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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2.15V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f24j11t-i-so

PIC18F46J11 FAMILY

28/44-Pin, Low-Power, High-Performance Microcontrollers

Power Management Features with nanoWatt XLP for Extreme Low Power:

- Deep Sleep mode: CPU off, Peripherals off, Currents Down to 13 nA and 850 nA with RTCC
 - Able to wake-up on external triggers, programmable WDT or RTCC alarm
 - Ultra Low-Power Wake-up (ULPWU)
- Sleep mode: CPU off, Peripherals off, SRAM on, Fast Wake-up, Currents Down to 105 nA Typical
- Idle: CPU off, Peripherals on, Currents Down to 2.3 μ A Typical
- Run: CPU on, Peripherals on, Currents Down to 6.2 μ A Typical
- Timer1 Oscillator/w RTCC: 1 μ A, 32 kHz Typical
- Watchdog Timer: 813 nA, 2V Typical

Special Microcontroller Features:

- 5.5V Tolerant Inputs (digital only pins)
- Low-Power, High-Speed CMOS Flash Technology
- C Compiler Optimized Architecture for Re-Entrant Code
- Priority Levels for Interrupts
- Self-Programmable under Software Control
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
 - Programmable period from 4 ms to 131s
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Operating Voltage Range of 2.0V to 3.6V
- On-Chip 2.5V Regulator
- Flash Program Memory of 10,000 Erase/Write Cycles Minimum and 20-Year Data Retention

Peripheral Highlights:

- Peripheral Pin Select:
 - Allows independent I/O mapping of many peripherals
 - Continuous hardware integrity checking and safety interlocks prevent unintentional configuration changes
- Hardware Real-Time Clock and Calendar (RTCC):
 - Provides clock, calendar and alarm functions
- High-Current Sink/Source 25 mA/25 mA (PORTB and PORTC)

Peripheral Highlights (Continued):

- Four Programmable External Interrupts
- Four Input Change Interrupts
- Two Enhanced Capture/Compare/PWM (ECCP) modules:
 - One, two or four PWM outputs
 - Selectable polarity
 - Programmable dead time
 - Auto-shutdown and auto-restart
 - Pulse steering control
- Two Master Synchronous Serial Port (MSSP) modules featuring:
 - 3-wire SPI (all 4 modes)
 - 1024-byte SPI Direct Memory Access (DMA) channel
 - I²C™ Master and Slave modes
- 8-Bit Parallel Master Port/Enhanced Parallel Slave Port
- Two-Rail – Rail Analog Comparators with Input Multiplexing
- 10-Bit, up to 13-Channel Analog-to-Digital (A/D) Converter module:
 - Auto-acquisition capability
 - Conversion available during Sleep
 - Self-Calibration
- High/Low-Voltage Detect module
- Charge Time Measurement Unit (CTMU):
 - Supports capacitive touch sensing for touch screens and capacitive switches
 - Provides a Precise Resolution Time Measurement for Both Flow Measurement and Simple Temperature Sensing
- Two Enhanced USART modules:
 - Supports RS-485, RS-232 and LIN/J2602
 - Auto-wake-up on Start bit
- Auto-Baud Detect

Flexible Oscillator Structure:

- 1% Accurate High-Precision Internal Oscillator
- Two External Clock modes, up to 48 MHz (12 MIPS)
- Low-Power 31 kHz Internal RC Oscillator
- Tunable Internal Oscillator (31 kHz to 8 MHz, $\pm 0.15\%$ Typical, $\pm 1\%$ Max).
- 4x PLL Option
- Secondary Oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor:
 - Allows for safe shutdown if any clock stops
- Two-Speed Oscillator Start-up
- Programmable Reference Clock Output Generator

4.0 LOW-POWER MODES

The PIC18F46J11 family devices can manage power consumption through clocking to the CPU and the peripherals. In general, reducing the clock frequency and the amount of circuitry being clocked reduces power consumption.

For managing power in an application, the primary modes of operation are:

- Run Mode
- Idle Mode
- Sleep Mode
- Deep Sleep Mode

Additionally, there is an Ultra Low-Power Wake-up (ULPWU) mode for generating an interrupt-on-change on RA0.

These modes define which portions of the device are clocked and at what speed.

- The Run and Idle modes can use any of the three available clock sources (primary, secondary or internal oscillator blocks).
- The Sleep mode does not use a clock source.

The ULPWU mode on RA0 allows a slow falling voltage to generate an interrupt-on-change on RA0 without excess current consumption. See **Section 4.7 “Ultra Low-Power Wake-up”**.

The power-managed modes include several power-saving features offered on previous PIC® devices, such as clock switching, ULPWU and Sleep mode. In addition, the PIC18F46J11 family devices add a new power-managed Deep Sleep mode.

4.1 Selecting Power-Managed Modes

Selecting a power-managed mode requires these decisions:

- Will the CPU be clocked?
- If so, which clock source will be used?

The IDLEN bit (OSCCON<7>) controls CPU clocking and the SCS<1:0> bits (OSCCON<1:0>) select the clock source. The individual modes, bit settings, clock sources and affected modules are summarized in Table 4-1.

4.1.1 CLOCK SOURCES

The SCS<1:0> bits allow the selection of one of three clock sources for power-managed modes. They are:

- Primary clock source – Defined by the FOSC<2:0> Configuration bits
- Timer1 clock – Provided by the secondary oscillator
- Postscaled internal clock – Derived from the internal oscillator block

4.1.2 ENTERING POWER-MANAGED MODES

Switching from one clock source to another begins by loading the OSCCON register. The SCS<1:0> bits select the clock source.

Changing these bits causes an immediate switch to the new clock source, assuming that it is running. The switch also may be subject to clock transition delays. These delays are discussed in **Section 4.1.3 “Clock Transitions and Status Indicators”** and subsequent sections.

Entry to the power-managed Idle or Sleep modes is triggered by the execution of a SLEEP instruction. The actual mode that results depends on the status of the IDLEN bit.

Depending on the current mode and the mode being switched to, a change to a power-managed mode does not always require setting all of these bits. Many transitions may be done by changing the oscillator select bits, the IDLEN bit or the DSEN bit prior to issuing a SLEEP instruction.

If the IDLEN and DSEN bits are already configured correctly, it may only be necessary to perform a SLEEP instruction to switch to the desired mode.

4.3 Sleep Mode

The power-managed Sleep mode is identical to the legacy Sleep mode offered in all other PIC devices. It is entered by clearing the IDLEN bit (the default state on device Reset) and executing the `SLEEP` instruction. This shuts down the selected oscillator (Figure 4-5). All clock source status bits are cleared.

Entering the Sleep mode from any other mode does not require a clock switch. This is because no clocks are needed once the controller has entered Sleep mode. If the WDT is selected, the INTRC source will continue to operate. If the Timer1 oscillator is enabled, it will also continue to run.

When a wake event occurs in Sleep mode (by interrupt, Reset or WDT time-out), the device will not be clocked until the clock source selected by the `SCS<1:0>` bits becomes ready (see Figure 4-6), or it will be clocked from the internal oscillator if either the Two-Speed Start-up or the FSCM is enabled (see **Section 26.0 “Special Features of the CPU”**). In either case, the OSTS bit is set when the primary clock is providing the device clocks. The IDLEN and SCS bits are not affected by the wake-up.

FIGURE 4-5: TRANSITION TIMING FOR ENTRY TO SLEEP MODE

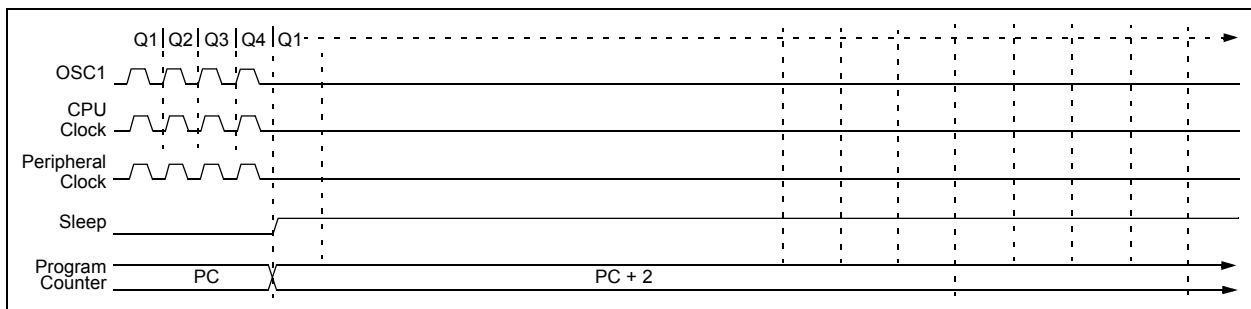
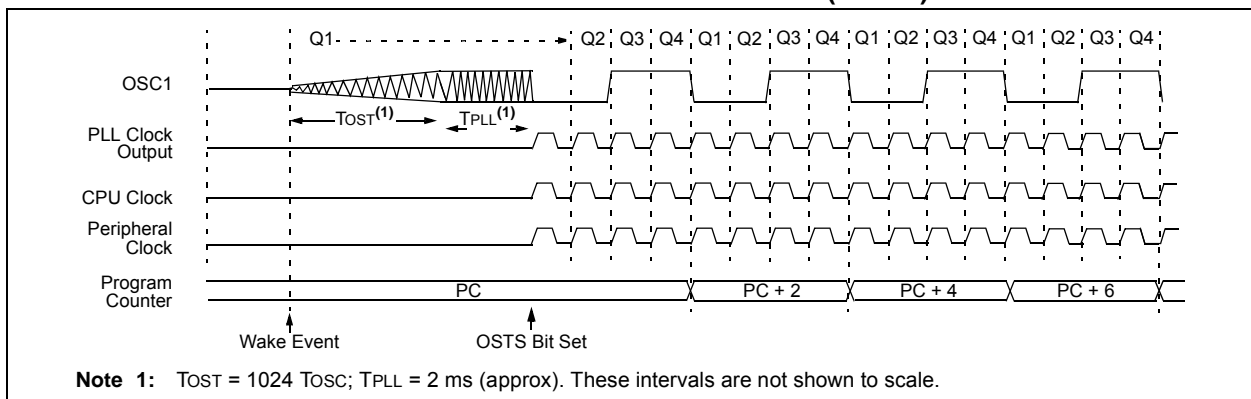


FIGURE 4-6: TRANSITION TIMING FOR WAKE FROM SLEEP (HSPLL)



4.7 Ultra Low-Power Wake-up

The Ultra Low-Power Wake-up (ULPWU) on RA0 allows a slow falling voltage to generate an interrupt without excess current consumption.

Follow these steps to use this feature:

1. Configure a remappable output pin to output the ULPOUT signal.
2. Map an INTx interrupt-on-change input function to the same pin as used for the ULPOUT output function. Alternatively, in step 1, configure ULPOUT to output onto a PORTB interrupt-on-change pin.
3. Charge the capacitor on RA0 by configuring the RA0 pin to an output and setting it to '1'.
4. Enable interrupt for the corresponding pin selected in step 2.
5. Stop charging the capacitor by configuring RA0 as an input.
6. Discharge the capacitor by setting the ULPEN and ULPSINK bits in the WDTCON register.
7. Configure Sleep mode.
8. Enter Sleep mode.

When the voltage on RA0 drops below V_{IL} , an interrupt will be generated, which will cause the device to wake-up and execute the next instruction.

This feature provides a low-power technique for periodically waking up the device from Sleep mode. The time-out is dependent on the discharge time of the RC circuit on RA0.

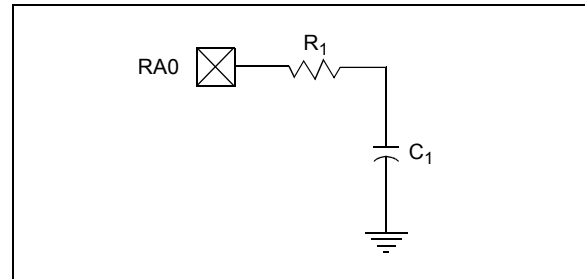
When the ULPWU module causes the device to wake-up from Sleep mode, the WDTCON<ULPLVL> bit is set. When the ULPWU module causes the device to wake-up from Deep Sleep, the DSULP (DSWAKEL<5>) bit is set. Software can check these bits upon wake-up to determine the wake-up source. Also in Sleep mode, only the remappable output function, ULPWU, will output this bit value to an RPN pin for externally detecting wake-up events.

See Example 4-1 for initializing the ULPWU module.

Note: For module-related bit definitions, see the WDTCON register in **Section 26.2 “Watchdog Timer (WDT)”** and the DSWAKEL register (Register 4-6).

A series resistor between RA0 and the external capacitor provides overcurrent protection for the RA0/AN0/C1INA/ULPWU/RP0 pin and can allow for software calibration of the time-out (see Figure 4-9).

FIGURE 4-9: SERIAL RESISTOR



A timer can be used to measure the charge time and discharge time of the capacitor. The charge time can then be adjusted to provide the desired interrupt delay. This technique will compensate for the affects of temperature, voltage and component accuracy. The peripheral can also be configured as a simple Programmable Low-Voltage Detect (LVD) or temperature sensor.

Note: For more information, refer to AN879, “Using the Microchip Ultra Low-Power Wake-up Module” application note (DS00879).

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REGISTER 10-9: RPINR4: PERIPHERAL PIN SELECT INPUT REGISTER 4 (BANKED EEAh)

U-0	U-0	U-0	R \overline{W} -1	R \overline{W} -1	R \overline{W} -1	R \overline{W} -1	R \overline{W} -1
—	—	—	T0CKR4	T0CKR3	T0CKR2	T0CKR1	T0CKR0
bit 7			bit 0				

Legend:	R/W = Readable, Writable if IOLOCK = 0
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **T0CKR<4:0>:** Timer0 External Clock Input (T0CKI) to the Corresponding RPn Pin bits

REGISTER 10-10: RPINR6: PERIPHERAL PIN SELECT INPUT REGISTER 6 (BANKED EECh)

U-0	U-0	U-0	R \overline{W} -1	R \overline{W} -1	R \overline{W} -1	R \overline{W} -1	R \overline{W} -1
—	—	—	T3CKR4	T3CKR3	T3CKR2	T3CKR1	T3CKR0
bit 7			bit 0				

Legend:	R/W = Readable, Writable if IOLOCK = 0
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **T3CKR<4:0>:** Timer 3 External Clock Input (T3CKI) to the Corresponding RPn Pin bits

REGISTER 10-11: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7 (BANKED EEDh)

U-0	U-0	U-0	R \overline{W} -1	R \overline{W} -1	R \overline{W} -1	R \overline{W} -1	R \overline{W} -1
—	—	—	IC1R4	IC1R3	IC1R2	IC1R1	IC1R0
bit 7			bit 0				

Legend:	R/W = Readable, Writable if IOLOCK = 0
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **IC1R<4:0>:** Assign Input Capture 1 (ECCP1) to the Corresponding RPn Pin bits

11.2.2 WRITE TO SLAVE PORT

When chip select is active and a write strobe occurs (PMCS = 1 and PMWR = 1), the data from PMD<7:0> is captured into the lower PMDIN1L register. The PMPIF and IBF flag bits are set when the write ends. The timing for the control signals in Write mode is displayed in Figure 11-3. The polarity of the control signals are configurable.

11.2.3 READ FROM SLAVE PORT

When chip select is active and a read strobe occurs (PMCS = 1 and PMRD = 1), the data from the PMDOUT1L register (PMDOUT1L<7:0>) is presented onto PMD<7:0>. Figure 11-4 provides the timing for the control signals in Read mode.

FIGURE 11-3: PARALLEL SLAVE PORT WRITE WAVEFORMS

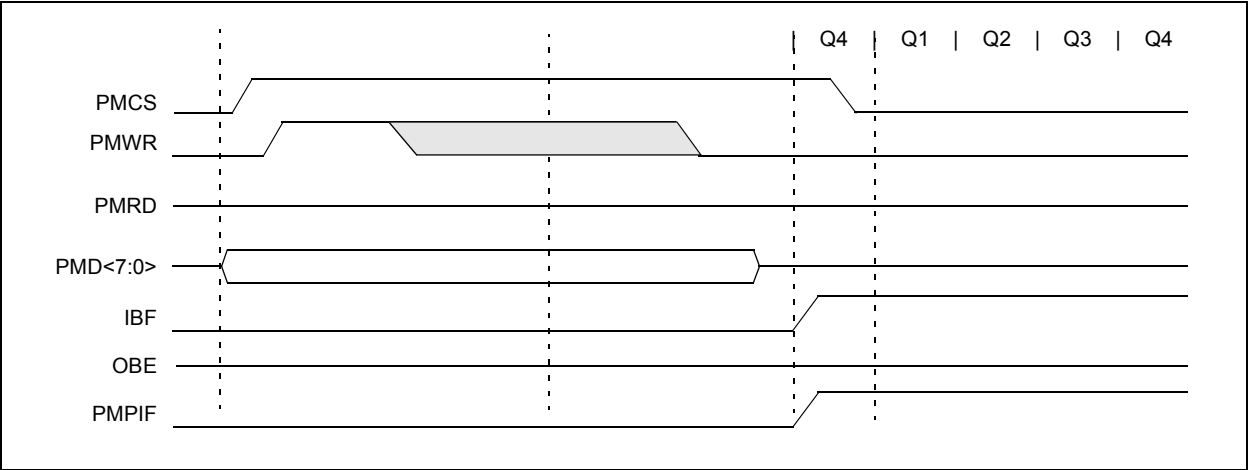
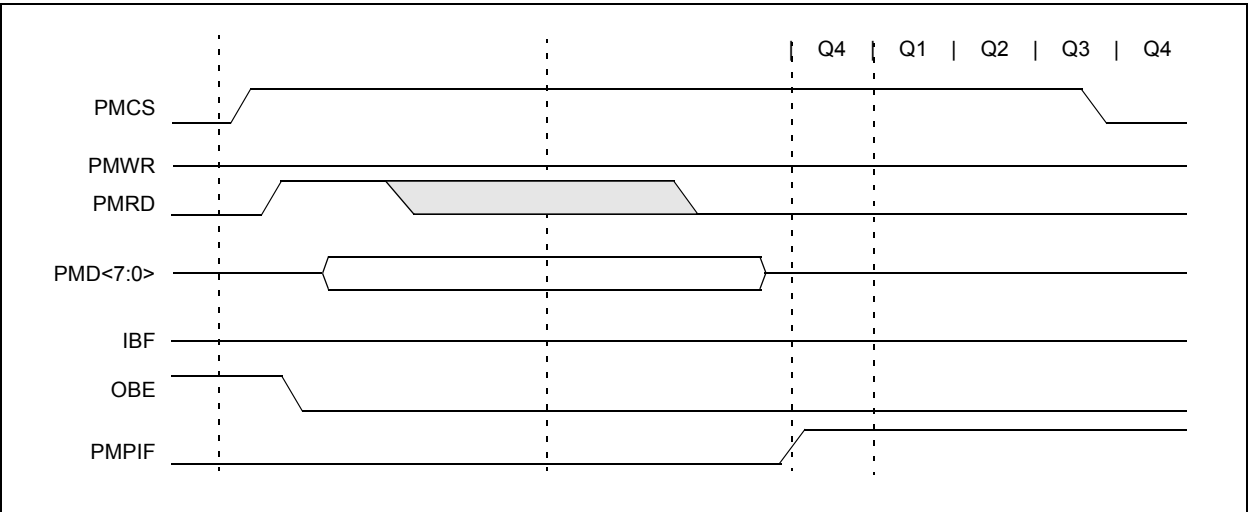


FIGURE 11-4: PARALLEL SLAVE PORT READ WAVEFORMS



PIC18F46J11 FAMILY

11.2.4 BUFFERED PARALLEL SLAVE PORT MODE

Buffered Parallel Slave Port mode is functionally identical to the legacy PSP mode with one exception, the implementation of 4-level read and write buffers. Buffered PSP mode is enabled by setting the INCM bits in the PMMODEH register. If the INCM<1:0> bits are set to '11', the PMP module will act as the Buffered PSP.

When the Buffered mode is active, the PMDIN1L, PMDIN1H, PMDIN2L and PMDIN2H registers become the write buffers and the PMDOUT1L, PMDOUT1H, PMDOUT2L and PMDOUT2H registers become the read buffers. Buffers are numbered 0 through 3, starting with the lower byte of PMDIN1L to PMDIN2H as the read buffers and PMDOUT1L to PMDOUT2H as the write buffers.

11.2.4.1 READ FROM SLAVE PORT

For read operations, the bytes will be sent out sequentially, starting with Buffer 0 (PMDOUT1L<7:0>) and ending with Buffer 3 (PMDOUT2H<7:0>) for every read strobe. The module maintains an internal pointer to keep track of which buffer is to be read. Each buffer has a corresponding read status bit, OBxE, in the PMSTATL register. This bit is cleared when a buffer contains data that has not been written to the bus, and is set when data is written to the bus. If the current buffer location being read from is empty, a buffer underflow is generated, and the Buffer Overflow flag bit, OBUF, is set. If all four OBxE status bits are set, then the Output Buffer Empty flag (OBE) will also be set.

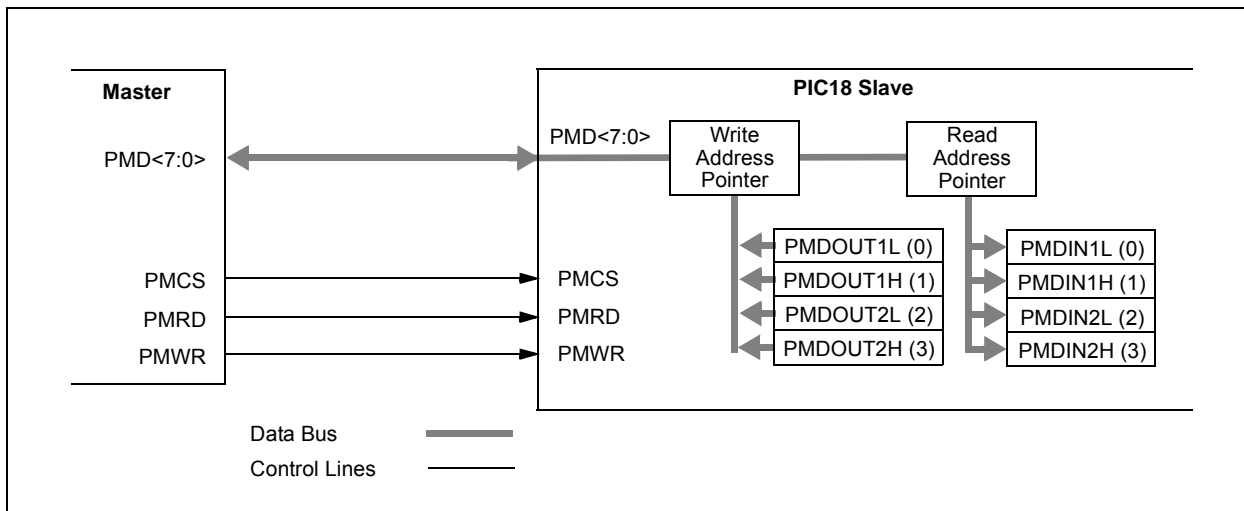
11.2.4.2 WRITE TO SLAVE PORT

For write operations, the data has to be stored sequentially, starting with Buffer 0 (PMDIN1L<7:0>) and ending with Buffer 3 (PMDIN2H<7:0>). As with read operations, the module maintains an internal pointer to the buffer that is to be written next.

The input buffers have their own write status bits, IBxF in the PMSTATH register. The bit is set when the buffer contains unread incoming data, and cleared when the data has been read. The flag bit is set on the write strobe. If a write occurs on a buffer when its associated IBxF bit is set, the Buffer Overflow flag, IBOV, is set; any incoming data in the buffer will be lost. If all four IBxF flags are set, the Input Buffer Full Flag (IBF) is set.

In Buffered Slave mode, the module can be configured to generate an interrupt on every read or write strobe (IRQM<1:0> = 01). It can be configured to generate an interrupt on a read from Read Buffer 3 or a write to Write Buffer 3, which is essentially an interrupt every fourth read or write strobe (RQM<1:0> = 11). When interrupting every fourth byte for input data, all input buffer registers should be read to clear the IBxF flags. If these flags are not cleared, then there is a risk of hitting an overflow condition.

FIGURE 11-5: PARALLEL MASTER/SLAVE CONNECTION BUFFERED EXAMPLE



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REGISTER 17-2: RTCCAL: RTCC CALIBRATION REGISTER (BANKED F3Eh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CAL<7:0>:** RTC Drift Calibration bits
01111111 = Maximum positive adjustment; adds 508 RTC clock pulses every minute
.
.
.
00000001 = Minimum positive adjustment; adds four RTC clock pulses every minute
00000000 = No adjustment
11111111 = Minimum negative adjustment; subtracts four RTC clock pulses every minute
.
.
.
10000000 = Maximum negative adjustment; subtracts 512 RTC clock pulses every minute

REGISTER 17-3: PADCFG1: PAD CONFIGURATION REGISTER (BANKED F3Ch)

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	RTSECSEL1 ⁽¹⁾	RTSECSEL0 ⁽¹⁾	PMPTTL
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-3 **Unimplemented:** Read as '0'
bit 2-1 **RTSECSEL<1:0>:** RTCC Seconds Clock Output Select bits⁽¹⁾
11 = Reserved, do not use
10 = RTCC source clock is selected for the RTCC pin (pin can be INTRC or T1OSC, depending on the RTCOSC (CONFIG3L<1>) setting)
01 = RTCC seconds clock is selected for the RTCC pin
00 = RTCC alarm pulse is selected for the RTCC pin
bit 0 **PMPTTL:** PMP Module TTL Input Buffer Select bit
1 = PMP module uses TTL input buffers
0 = PMP module uses Schmitt input buffers

Note 1: To enable the actual RTCC output, the RTCOE (RTCCFG<2>) bit must be set.

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19.4.6 USING THE SPI DMA MODULE

The following steps would typically be taken to enable and use the SPI DMA module:

1. Configure the I/O pins, which will be used by MSSP2.
 - a) Assign SCK2, SDO2, SDI2 and $\overline{SS}2$ to RPN pins as appropriate for the SPI mode which will be used. Only functions which will be used need to be assigned to a pin.
 - b) Initialize the associated LATx registers for the desired Idle SPI bus state.
 - c) If Open-Drain Output mode on SDO2 and SCK2 (Master mode) is desired, set ODCON3<1>.
 - d) Configure corresponding TRISx bits for each I/O pin used
2. Configure and enable MSSP2 for the desired SPI operating mode.
 - a) Select the desired operating mode (Master or Slave, SPI Mode 0, 1, 2 and 3) and configure the module by writing to the SSP2STAT and SSP2CON1 registers.
 - b) Enable MSSP2 by setting SSP2CON1<5> = 1.
3. Configure the SPI DMA engine.
 - a) Select the desired operating mode by writing the appropriate values to DMACON2 and DMACON1.
 - b) Initialize the TXADDRH/TXADDRL Pointer (Full-Duplex or Half-Duplex Transmit Only mode).
 - c) Initialize the RXADDRH/RXADDRL Pointer (Full-Duplex or Half-Duplex Receive Only mode).
 - d) Initialize the DMABCH/DMABCL Byte Count register with the number of bytes to be transferred in the next SPI DMA operation.
 - e) Set the DMAEN bit (DMACON1<0>).

In SPI Master modes, this will initiate a DMA transaction. In SPI Slave modes, this will complete the initialization process, and the module will now be ready to begin receiving and/or transmitting data to the master device once the master starts the transaction.

4. Detect the SSP2IF interrupt condition (PIR3<7>).
 - a) If the interrupt was configured to occur at the completion of the SPI DMA transaction, the DMAEN bit (DMACON1<0>) will be clear. User firmware may prepare the module for another transaction by repeating steps 3.b through 3.e.
 - b) If the interrupt was configured to occur prior to the completion of the SPI DMA transaction, the DMAEN bit may still be set, indicating the transaction is still in progress. User firmware would typically use this interrupt condition to begin preparing new data for the next DMA transaction. Firmware should not repeat steps 3.b. through 3.e. until the DMAEN bit is cleared by the hardware, indicating the transaction is complete.

Example 19-2 provides example code demonstrating the initialization process and the steps needed to use the SPI DMA module to perform a 512-byte Full-Duplex, Master mode transfer.

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19.5.10 I²C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address or the other half of a 10-bit address, is accomplished by simply writing a value to the SSPxBUF register. This action will set the Buffer Full flag bit, BF, and allow the BRG to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDAx pin after the falling edge of SCLx is asserted (see data hold time specification parameter 106). SCLx is held low for one BRG rollover count (TBRG). Data should be valid before SCLx is released high (see data setup time specification parameter 107). When the SCLx pin is released high, it is held that way for TBRG.

The data on the SDAx pin must remain stable for that duration and some hold time after the next falling edge of SCLx. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDAx. This allows the slave device being addressed to respond with an ACK bit during the ninth bit time if an address match occurred, or if data was received properly. The status of ACK is written into the ACKDT bit on the falling edge of the ninth clock.

If the master receives an Acknowledge, the Acknowledge Status bit, ACKSTAT, is cleared; if not, the bit is set. After the ninth clock, the SSPxIF bit is set and the master clock (BRG) is suspended until the next data byte is loaded into the SSPxBUF, leaving SCLx low and SDAx unchanged (Figure 19-23).

After the write to the SSPxBUF, each bit of the address will be shifted out on the falling edge of SCLx until all seven address bits and the R/W bit are completed. On the falling edge of the eighth clock, the master will deassert the SDAx pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDAx pin to see if the address was recognized by a slave. The status of the ACK bit is loaded into the ACKSTAT status bit (SSPxCON2<6>). Following the falling edge of the ninth clock transmission of the address, the SSPxIF flag is set, the BF flag is cleared and the BRG is turned off until another write to the SSPxBUF takes place, holding SCLx low and allowing SDAx to float.

19.5.10.1 BF Status Flag

In Transmit mode, the BF bit (SSPxSTAT<0>) is set when the CPU writes to SSPxBUF and is cleared when all eight bits are shifted out.

19.5.10.2 WCOL Status Flag

If the user writes the SSPxBUF when a transmit is already in progress (i.e., SSPxSR is still shifting out a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur) after 2 Tcy after the SSPxBUF write. If SSPxBUF is rewritten within 2 Tcy, the WCOL bit is set and SSPxBUF is updated. This may result in a corrupted transfer.

The user should verify that the WCOL bit is clear after each write to SSPxBUF to ensure the transfer is correct. In all cases, WCOL must be cleared in software.

19.5.10.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit (SSPxCON2<6>) is cleared when the slave has sent an Acknowledge (ACK = 0) and is set when the slave does not Acknowledge (ACK = 1). A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

19.5.11 I²C MASTER MODE RECEPTION

Master mode reception is enabled by programming the Receive Enable bit, RCEN (SSPxCON2<3>).

Note:	The MSSP module must be in an inactive state before the RCEN bit is set or the RCEN bit will be disregarded.
--------------	--

The BRG begins counting and on each rollover, the state of the SCLx pin changes (high-to-low/low-to-high) and data is shifted into the SSPxSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPxSR are loaded into the SSPxBUF, the BF flag bit is set, the SSPxIF flag bit is set and the BRG is suspended from counting, holding SCLx low. The MSSP is now in Idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable bit, ACKEN (SSPxCON2<4>).

19.5.11.1 BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPxBUF from SSPxSR. It is cleared when the SSPxBUF register is read.

19.5.11.2 SSPOV Status Flag

In receive operation, the SSPOV bit is set when 8 bits are received into the SSPxSR and the BF flag bit is already set from a previous reception.

19.5.11.3 WCOL Status Flag

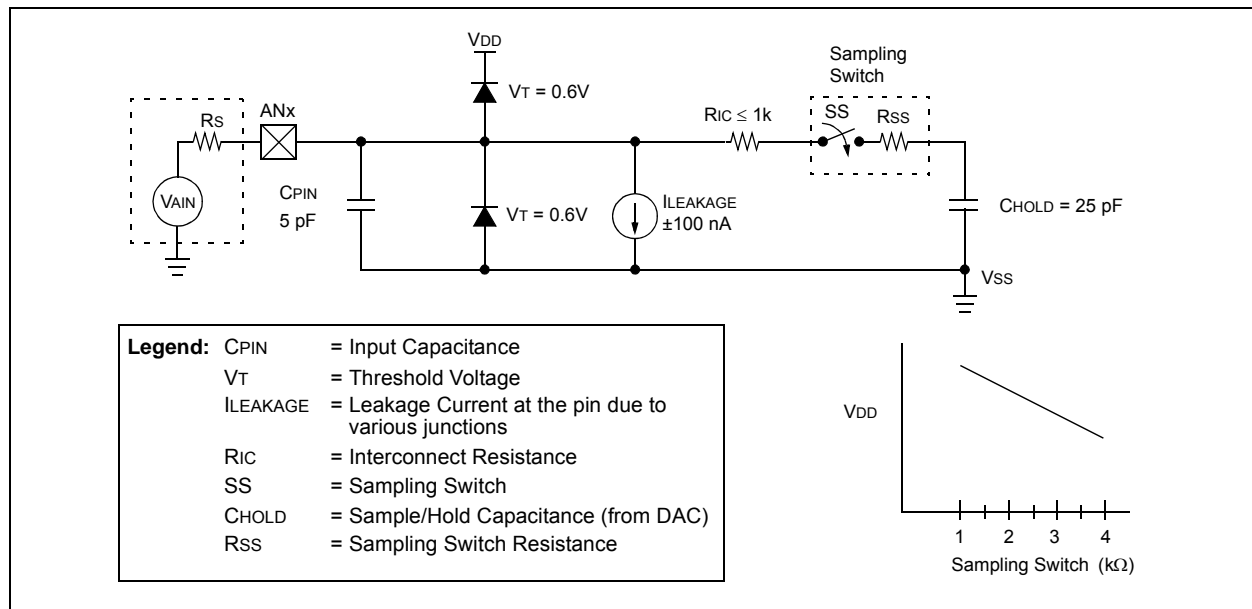
If users write the SSPxBUF when a receive is already in progress (i.e., SSPxSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see **Section 21.1 “A/D Acquisition Requirements”**. After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the $\overline{\text{GO/DONE}}$ bit and the actual start of the conversion.

The following steps should be followed to do an A/D conversion:

1. Configure the A/D module:
 - Configure the required ADC pins as analog pins using ANCON0, ANCON1
 - Set voltage reference using ADCON0
 - Select A/D input channel (ADCON0)
 - Select A/D acquisition time (ADCON1)
 - Select A/D conversion clock (ADCON1)
 - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
 - Clear ADIF bit
 - Set ADIE bit
 - Set GIE bit
3. Wait the required acquisition time (if required).
4. Start conversion:
 - Set $\overline{\text{GO/DONE}}$ bit (ADCON0<1>)
5. Wait for A/D conversion to complete, by either:
 - Polling for the $\overline{\text{GO/DONE}}$ bit to be cleared
 OR
 - Waiting for the A/D interrupt
6. Read A/D Result registers (ADRESH:ADRESL); clear bit, ADIF, if required.
7. For next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as T_{AD} . A minimum wait of 2 T_{AD} is required before next acquisition starts.

FIGURE 21-2: ANALOG INPUT MODEL



PIC18F46J11 FAMILY

22.7 Comparator Operation During Sleep

When a comparator is active and the device is placed in Sleep mode, the comparator remains active and the interrupt is functional if enabled. This interrupt will wake-up the device from Sleep mode when enabled. Each operational comparator will consume additional current. To minimize power consumption while in Sleep mode, turn off the comparators (CON = 0) before entering Sleep. If the device wakes up from Sleep, the contents of the CMxCON register are not affected.

22.8 Effects of a Reset

A device Reset forces the CMxCON registers to their Reset state. This forces both comparators and the voltage reference to the OFF state.

TABLE 22-3: REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	69
PIR2	OSCFIF	CM2IF	CM1IF	—	BCL1IF	LVDIF	TMR3IF	CCP2IF	72
PIE2	OSCFIE	CM2IE	CM1IE	—	BCL1IE	LVDIE	TMR3IE	CCP2IE	72
IPR2	OSCFIP	CM2IP	CM1IP	—	BCL1IP	LVDIP	TMR3IP	CCP2IP	72
CMxCON	CON	COE	CPOL	EVPOL1	EVPOL0	CREF	CCH1	CCH0	70
CVRCON	CVREN	CVROE	CVRR	CVRSS	CVR3	CVR2	CVR1	CVR0	74
CMSTAT	—	—	—	—	—	—	COUT2	COUT1	73
ANCON0	PCFG7 ⁽¹⁾	PCFG6 ⁽¹⁾	PCFG5 ⁽¹⁾	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	74
PORTA	RA7	RA6	RA5	—	RA3	RA2	RA1	RA0	72
TRISA	TRISA7	TRISA6	TRISA5	—	TRISA3	TRISA2	TRISA1	TRISA0	72

Legend: — = unimplemented, read as '0', r = reserved. Shaded cells are not related to comparator operation.

Note 1: These bits and/or registers are not implemented on 28-pin devices.

PIC18F46J11 FAMILY

ADDWFC

ADD W and Carry bit to f

Syntax: ADDWFC f {,d {,a}}

Operands: $0 \leq f \leq 255$
 $d \in [0,1]$
 $a \in [0,1]$

Operation: $(W) + (f) + (C) \rightarrow \text{dest}$

Status Affected: N, OV, C, DC, Z

Encoding:

0010	00da	ffff	ffff
------	------	------	------

Description: Add W, the Carry flag and data memory location 'f'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed in data memory location 'f'.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \leq 95$ (5Fh). See **Section 27.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: ADDWFC REG, 0, 1

Before Instruction

Carry bit = 1
REG = 02h
W = 4Dh

After Instruction

Carry bit = 0
REG = 02h
W = 50h

ANDLW

AND Literal with W

Syntax: ANDLW k

Operands: $0 \leq k \leq 255$

Operation: $(W) .\text{AND}. k \rightarrow W$

Status Affected: N, Z

Encoding:

0000	1011	kkkk	kkkk
------	------	------	------

Description: The contents of W are ANDed with the 8-bit literal 'k'. The result is placed in W.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write to W

Example: ANDLW 0x5F

Before Instruction

W = A3h

After Instruction

W = 03h

PIC18F46J11 FAMILY

BTFSC Bit Test File, Skip if Clear

Syntax:	BTFSC f, b {a}			
Operands:	$0 \leq f \leq 255$ $0 \leq b \leq 7$ $a \in [0,1]$			
Operation:	skip if ($f < b$) = 0			
Status Affected:	None			
Encoding:	1011	bbba	ffff	ffff
Description:	<p>If bit 'b' in register 'f' is '0', then the next instruction is skipped. If bit 'b' is '0', then the next instruction fetched during the current instruction execution is discarded and a NOP is executed instead, making this a two-cycle instruction.</p> <p>If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).</p> <p>If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \leq 95$ (5Fh). See Section 27.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.</p>			
Words:	1			
Cycles:	1(2)			
	Note: 3 cycles if skip and followed by a 2-word instruction.			

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:

HERE	BTFSC	FLAG, 1, 0
FALSE	:	
TRUE	:	

Before Instruction

PC = address (HERE)

After Instruction

If FLAG<1> = 0;
 PC = address (TRUE)
 If FLAG<1> = 1;
 PC = address (FALSE)

BTFSS Bit Test File, Skip if Set

Syntax:	BTFSS f, b {,a}				
Operands:	$0 \leq f \leq 255$ $0 \leq b < 7$ $a \in [0,1]$				
Operation:	skip if ($f < b$) = 1				
Status Affected:	None				
Encoding:	<table border="1"><tr><td>1010</td><td>bbba</td><td>ffff</td><td>ffff</td></tr></table>	1010	bbba	ffff	ffff
1010	bbba	ffff	ffff		
Description:	<p>If bit 'b' in register 'f' is '1', then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution is discarded and a NOP is executed instead, making this a two-cycle instruction.</p> <p>If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).</p> <p>If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \leq 95$ (5Fh). See Section 27.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.</p>				
Words:	1				
Cycles:	1(2) Note: 3 cycles if skip and followed by a 2-word instruction.				

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:

HERE	BTFSS	FLAG, 1, 0
FALSE	:	
TRUE	:	

Before Instruction

PC = address (HERE)

After Instruction

If FLAG<1> = 0;
 PC = address (FALSE)
 If FLAG<1> = 1;
 PC = address (TRUE)

PIC18F46J11 FAMILY

28.2 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

28.3 MPLAB C18 and MPLAB C30 C Compilers

The MPLAB C18 and MPLAB C30 Code Development Systems are complete ANSI C compilers for Microchip's PIC18 and PIC24 families of microcontrollers and the dsPIC30 and dsPIC33 family of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

28.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

28.5 MPLAB ASM30 Assembler, Linker and Librarian

MPLAB ASM30 Assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

28.6 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C18 and MPLAB C30 C Compilers, and the MPASM and MPLAB ASM30 Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

PIC18F46J11 FAMILY

29.2 DC Characteristics: Power-Down and Supply Current PIC18F46J11 Family (Industrial) (Continued)

PIC18LFXXJ11 Family		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial						
PIC18FXXJ11 Family		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial						
Param No.	Device	Typ	Max	Units	Conditions			
	Supply Current (I_{DD}) ⁽²⁾							
	PIC18LFXXJ11	1.9	3.6	mA	-40°C	$V_{DD} = 2.0\text{V},$ $V_{DDCORE} = 2.0\text{V}$	Fosc = 8 MHz, RC_RUN mode, Internal RC Oscillator	
		2.0	3.8	mA	$+25^{\circ}\text{C}$			
		2.0	3.8	mA	$+85^{\circ}\text{C}$			
	PIC18LFXXJ11	2.8	4.8	mA	-40°C	$V_{DD} = 2.5\text{V},$ $V_{DDCORE} = 2.5\text{V}$		
		2.8	4.8	mA	$+25^{\circ}\text{C}$			
		2.8	4.9	mA	$+85^{\circ}\text{C}$			
	PIC18FXXJ11	2.3	4.2	mA	-40°C	$V_{DD} = 2.15\text{V},$ $V_{DDCORE} = 10\text{ }\mu\text{F}$ Capacitor		
		2.3	4.2	mA	$+25^{\circ}\text{C}$			
		2.4	4.5	mA	$+85^{\circ}\text{C}$			
	PIC18FXXJ11	2.8	5.1	mA	-40°C	$V_{DD} = 3.3\text{V},$ $V_{DDCORE} = 10\text{ }\mu\text{F}$ Capacitor		
		2.8	5.1	mA	$+25^{\circ}\text{C}$			
		2.8	5.4	mA	$+85^{\circ}\text{C}$			
	PIC18LFXXJ11	1.9	9.4	μA	-40°C	$V_{DD} = 2.0\text{V},$ $V_{DDCORE} = 2.0\text{V}$		Fosc = 31 kHz, RC_IDLE mode, Internal RC Oscillator, INTSRC = 0
		2.3	9.4	μA	$+25^{\circ}\text{C}$			
		4.5	17.2	μA	$+85^{\circ}\text{C}$			
	PIC18LFXXJ11	2.4	10.5	μA	-40°C	$V_{DD} = 2.5\text{V},$ $V_{DDCORE} = 2.5\text{V}$		
		2.8	10.5	μA	$+25^{\circ}\text{C}$			
		5.4	19.5	μA	$+85^{\circ}\text{C}$			
	PIC18FXXJ11	33.3	75	μA	-40°C	$V_{DD} = 2.15\text{V},$ $V_{DDCORE} = 10\text{ }\mu\text{F}$ Capacitor		
		43.8	75	μA	$+25^{\circ}\text{C}$			
		55.3	92	μA	$+85^{\circ}\text{C}$			
	PIC18FXXJ11	36.1	82	μA	-40°C	$V_{DD} = 3.3\text{V},$ $V_{DDCORE} = 10\text{ }\mu\text{F}$ Capacitor		
		44.5	82	μA	$+25^{\circ}\text{C}$			
		56.3	105	μA	$+85^{\circ}\text{C}$			

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption. All features that add delta current are disabled (WDT, etc.). The test conditions for all I_{DD} measurements in active operation mode are:
 OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD/VSS;
 MCLR = VDD; WDT disabled unless otherwise specified.
- 3:** Low-Power Timer1 with standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to $+70^{\circ}\text{C}$. Extended temperature crystals are available at a much higher cost.

PIC18F46J11 FAMILY

29.2 DC Characteristics: Power-Down and Supply Current PIC18F46J11 Family (Industrial) (Continued)

PIC18LFXXJ11 Family		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
PIC18FXXJ11 Family		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
Param No.	Device	Typ	Max	Units	Conditions	
	PIC18LFXXJ11	5.2	6.5	mA	-40°C	FOSC = 16 MHz (PRI_RUN mode, 4 MHz Internal Oscillator with PLL
		5.1	6.4	mA	$+25^{\circ}\text{C}$	
		5.1	6.4	mA	$+85^{\circ}\text{C}$	
	PIC18FXXJ11	5.3	7.5	mA	-40°C	
		5.2	7.4	mA	$+25^{\circ}\text{C}$	
		5.2	7.4	mA	$+85^{\circ}\text{C}$	
	PIC18LFXXJ11	9.3	12.0	mA	-40°C	FOSC = 32 MHz, PRI_RUN mode, 8 MHz Internal Oscillator with PLL
		9.2	11.8	mA	$+25^{\circ}\text{C}$	
		9.0	11.8	mA	$+85^{\circ}\text{C}$	
	PIC18FXXJ11	9.7	17.5	mA	-40°C	
		9.6	17.2	mA	$+25^{\circ}\text{C}$	
		9.6	17.2	mA	$+85^{\circ}\text{C}$	
	PIC18LFXXJ11	12.4	13.5	mA	-40°C	FOSC = 48 MHz, PRI_RUN mode, 12 MHz External Oscillator with PLL
		12.2	13.5	mA	$+25^{\circ}\text{C}$	
		12.1	13.9	mA	$+85^{\circ}\text{C}$	
	PIC18FXXJ11	14.3	24.1	mA	-40°C	
		14.2	23.0	mA	$+25^{\circ}\text{C}$	
		14.2	23.0	mA	$+85^{\circ}\text{C}$	

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption. All features that add delta current are disabled (WDT, etc.). The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD/VSS;
MCLR = VDD; WDT disabled unless otherwise specified.
- 3:** Low-Power Timer1 with standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to $+70^{\circ}\text{C}$. Extended temperature crystals are available at a much higher cost.

PIC18F46J11 FAMILY

FIGURE 29-12: PARALLEL SLAVE PORT TIMING

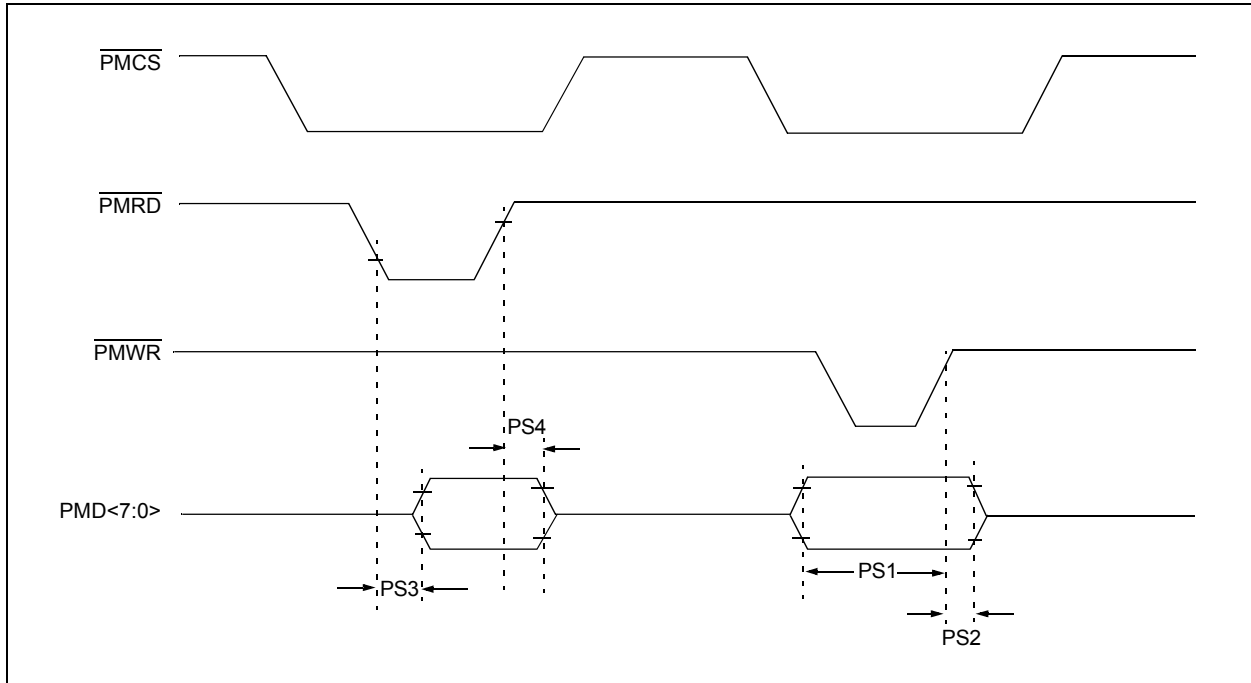


TABLE 29-19: PARALLEL SLAVE PORT REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial			
Param. No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
PS1	TdV2wrH	Data In Valid before $\overline{\text{PMWR}}$ or $\overline{\text{PMCS}}$ Inactive (setup time)	20	—	—	ns	
PS2	TwrH2dtI	$\overline{\text{PMWR}}$ or $\overline{\text{PMCS}}$ Inactive to Data-In Invalid (hold time)	20	—	—	ns	
PS3	TrdL2dtV	$\overline{\text{PMRD}}$ and $\overline{\text{PMCS}}$ Active to Data-Out Valid	—	—	80	ns	
PS4	TrdH2dtI	$\overline{\text{PMRD}}$ Inactive or $\overline{\text{PMCS}}$ Inactive to Data-Out Invalid	10	—	30	ns	

FIGURE 29-14: EXAMPLE SPI MASTER MODE TIMING (CKE = 1)

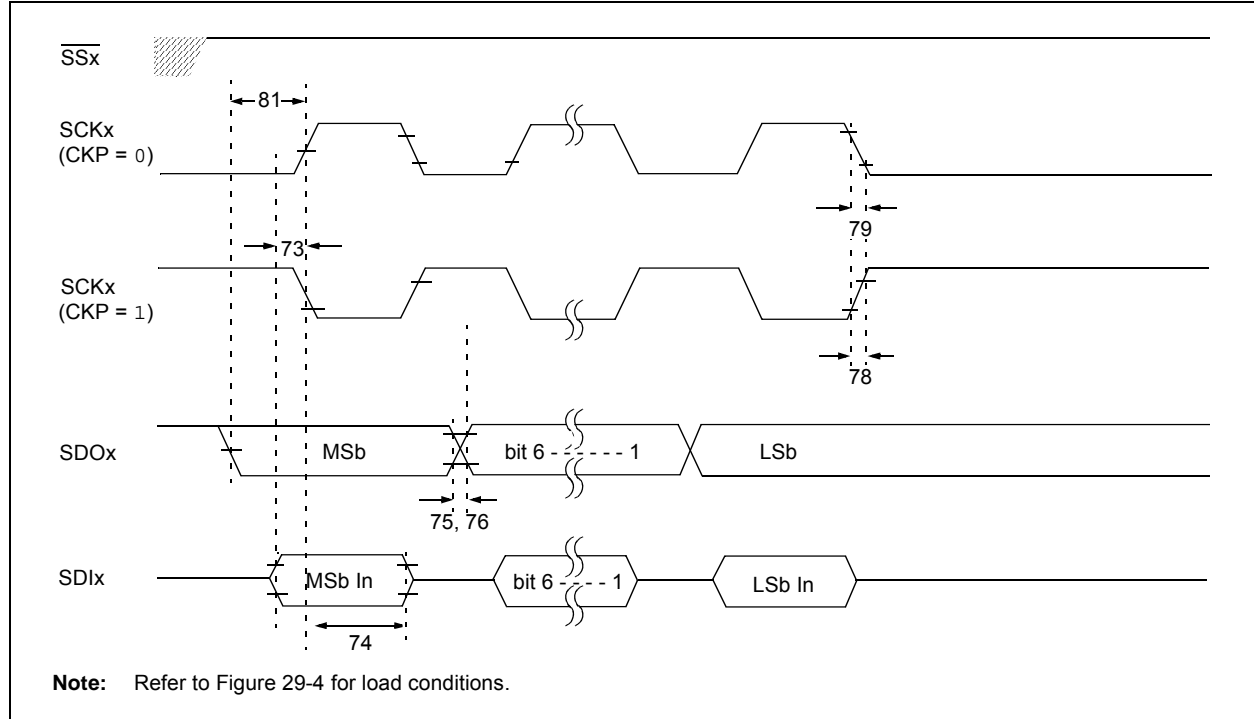


TABLE 29-21: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 1)

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
73	TdIV2scH, TdIV2scL	Setup Time of SDIx Data Input to SCKx Edge	35 100	—	ns ns	VDD = 3.3V, VDDCORE = 2.5V VDD = 2.15V, VDDCORE = 2.15V
74	Tsch2DiL, TscL2DiL	Hold Time of SDIx Data Input to SCKx Edge	30 83	—	ns ns	VDD = 3.3V, VDDCORE = 2.5V VDD = 2.15V
75	TdoR	SDOx Data Output Rise Time	—	25	ns	PORTB or PORTC
76	TdoF	SDOx Data Output Fall Time	—	25	ns	PORTB or PORTC
78	TscR	SCKx Output Rise Time (Master mode)	—	25	ns	PORTB or PORTC
79	TscF	SCKx Output Fall Time (Master mode)	—	25	ns	PORTB or PORTC
81	TdoV2sch, TdoV2scL	SDOx Data Output Setup to SCKx Edge	Tcy	—	ns	

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