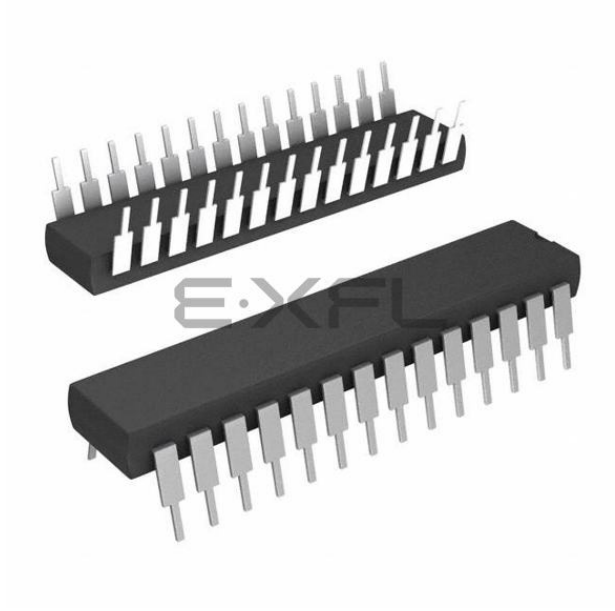


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf26j11-i-sp

NOTES:

TABLE 1-1: DEVICE FEATURES FOR THE PIC18F2XJ11 (28-PIN DEVICES)

Features	PIC18F24J11	PIC18F25J11	PIC18F26J11
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	16K	32K	64K
Program Memory (Instructions)	8,192	16,384	32,768
Data Memory (Bytes)	3.8K	3.8K	3.8K
Interrupt Sources	30		
I/O Ports	Ports A, B, C		
Timers	5		
Enhanced Capture/Compare/PWM Modules	2		
Serial Communications	MSSP (2), Enhanced USART (2)		
Parallel Communications (PMP/PSP)	No		
10-Bit Analog-to-Digital Module	10 Input Channels		
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST)		
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled		
Packages	28-Pin QFN, SOIC, SSOP and SPDIP (300 mil)		

TABLE 1-2: DEVICE FEATURES FOR THE PIC18F4XJ11 (44-PIN DEVICES)

Features	PIC18F44J11	PIC18F45J11	PIC18F46J11
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	16K	32K	64K
Program Memory (Instructions)	8,192	16,384	32,768
Data Memory (Bytes)	3.8K	3.8K	3.8K
Interrupt Sources	30		
I/O Ports	Ports A, B, C, D, E		
Timers	5		
Enhanced Capture/Compare/PWM Modules	2		
Serial Communications	MSSP (2), Enhanced USART (2)		
Parallel Communications (PMP/PSP)	Yes		
10-Bit Analog-to-Digital Module	13 Input Channels		
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST)		
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled		
Packages	44-Pin QFN and TQFP		

TABLE 1-4: PIC18F4XJ11 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	44-QFN	44-TQFP			
					PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/AN12/INT0/RP3	9	8			
RB0			I/O	DIG	Digital I/O.
AN12			I	Analog	Analog input 12.
INT0			I	ST	External interrupt 0.
RP3			I/O	DIG	Remappable peripheral pin 3.
RB1/AN10/PMBE/RTCC/RP4	10	9			
RB1			I/O	DIG	Digital I/O.
AN10			I	Analog	Analog input 10.
PMBE			O	DIG	Parallel Master Port byte enable.
RTCC			O	DIG	Real Time Clock Calendar output.
RP4			I/O	DIG	Remappable peripheral pin 4.
RB2/AN8/CTED1/PMA3/REFO/RP5	11	10			
RB2			I/O	DIG	Digital I/O.
AN8			I	Analog	Analog input 8.
CTED1			I	ST	CTMU edge 1 input.
PMA3			O	DIG	Parallel Master Port address.
REFO			O	DIG	Reference output clock.
RP5			I/O	DIG	Remappable peripheral pin 5.
RB3/AN9/CTED2/PMA2/RP6	12	11			
RB3			I/O	DIG	Digital I/O.
AN9			I	Analog	Analog input 9.
CTED2			I	ST	CTMU edge 2 input.
PMA2			O	DIG	Parallel Master Port address.
RP6			I/O	DIG	Remappable peripheral pin 6.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD}); DIG = Digital output

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

2.4 Voltage Regulator Pins (VCAP/ VDDCORE)

When the regulator is enabled ("F" devices), a low-ESR (< 5Ω) capacitor is required on the VCAP/VDDCORE pin to stabilize the voltage regulator output voltage. The VCAP/ VDDCORE pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specifications can be used.

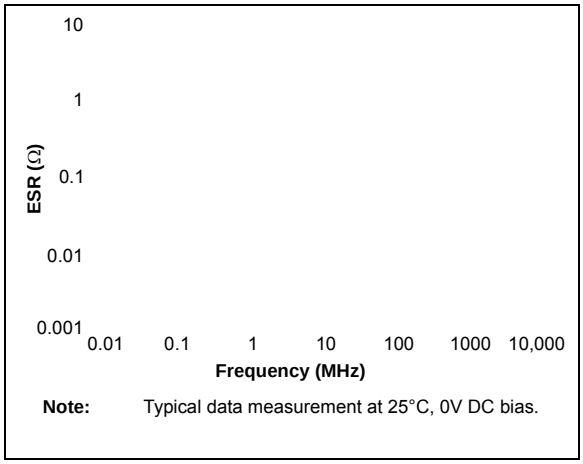
Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 28.0 "Electrical Characteristics"** for additional information.

When the regulator is disabled ("LF" devices), the VCAP/VDDCORE pin must be tied to a voltage supply at the VDDCORE level. Refer to **Section 28.0 "Electrical Characteristics"** for information on VDD and VDDCORE.

Note that the "LF" versions are provided with the voltage regulator permanently disabled; they must always be provided with a supply voltage on the VDDCORE pin.

FIGURE 2-3: FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at 25°C, 0V DC bias.

TABLE 2-1: SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to 125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to 85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to 125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to 85ºC
Murata	GRM32DR71C106KA01L	10 µF	±10%	16V	-55 to 125ºC
Murata	GRM31CR61C106KC31L	10 µF	±10%	16V	-55 to 85ºC

5.7 Reset State of Registers

Most registers are unaffected by a Reset. Their status is unknown on POR and unchanged by all other Resets. The other registers are forced to a "Reset state" depending on the type of Reset that occurred.

Most registers are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. Status bits from the RCON register ($\overline{CM}$, $\overline{RI}$, $\overline{TO}$, $\overline{PD}$, $\overline{POR}$ and $\overline{BOR}$) are set or cleared differently in different Reset situations, as indicated in Table 5-1. These bits are used in software to determine the nature of the Reset.

Table 5-2 describes the Reset states for all of the Special Function Registers. These are categorized by POR and BOR, $\overline{MCLR}$ and WDT Resets, and WDT wake-ups.

TABLE 5-1: STATUS BITS, THEIR SIGNIFICANCE AND THE INITIALIZATION CONDITION FOR RCON REGISTER

Condition	Program Counter(1)	RCON Register						STKPTR Register	
		$\overline{CM}$	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$	STKFUL	STKUNF
Power-on Reset	0000h	1	1	1	1	0	0	0	0
RESET instruction	0000h	u	0	u	u	u	u	u	u
Brown-out Reset	0000h	1	1	1	1	u	0	u	u
Configuration Mismatch Reset	0000h	0	u	u	u	u	u	u	u
$\overline{MCLR}$ Reset during power-managed Run modes	0000h	u	u	1	u	u	u	u	u
$\overline{MCLR}$ Reset during power-managed Idle modes and Sleep mode	0000h	u	u	1	0	u	u	u	u
$\overline{MCLR}$ Reset during full-power execution	0000h	u	u	u	u	u	u	u	u
Stack Full Reset (STVREN = 1)	0000h	u	u	u	u	u	u	1	u
Stack Underflow Reset (STVREN = 1)	0000h	u	u	u	u	u	u	u	1
Stack Underflow Error (not an actual Reset, STVREN = 0)	0000h	u	u	u	u	u	u	u	1
WDT time-out during full-power or power-managed Run modes	0000h	u	u	0	u	u	u	u	u
WDT time-out during power-managed Idle or Sleep modes	PC + 2	u	u	0	0	u	u	u	u
Interrupt exit from power-managed modes	PC + 2	u	u	u	0	u	u	u	u

Legend: u = unchanged

Note 1: When the wake-up is due to an interrupt and the GIEH or GIEL bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

TABLE 5-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset, Wake From Deep Sleep	$\overline{\text{MCLR}}$ Resets WDT Reset RESET Instruction Stack Resets CM Resets	Wake-up via WDT or Interrupt
PMDOUT2H(5)	—	PIC18F4XJ11	0000 0000	0000 0000	uuuu uuuu
PMDOUT2L(5)	—	PIC18F4XJ11	0000 0000	0000 0000	uuuu uuuu
PMDIN2H(5)	—	PIC18F4XJ11	0000 0000	0000 0000	uuuu uuuu
PMDIN2L(5)	—	PIC18F4XJ11	0000 0000	0000 0000	uuuu uuuu
PMEH(5)	—	PIC18F4XJ11	0000 0000	0000 0000	uuuu uuuu
PMEL(5)	—	PIC18F4XJ11	0000 0000	0000 0000	uuuu uuuu
PMSTATH(5)	—	PIC18F4XJ11	00-- 0000	00-- 0000	uu-- uuuu
PMSTATL(5)	—	PIC18F4XJ11	10-- 1111	10-- 1111	uu-- uuuu
CVRCON	PIC18F2XJ11	PIC18F4XJ11	0000 0000	0000 0000	uuuu uuuu
TCLKCON	PIC18F2XJ11	PIC18F4XJ11	---0 --00	---0 --uu	---u --uu
DSGPR1(6)	PIC18F2XJ11	PIC18F4XJ11	uuuu uuuu	uuuu uuuu	uuuu uuuu
DSGPR0(6)	PIC18F2XJ11	PIC18F4XJ11	uuuu uuuu	uuuu uuuu	uuuu uuuu
DSCONH(6)	PIC18F2XJ11	PIC18F4XJ11	0--- -000	0--- -uuu	u--- -uuu
DSCONL(6)	PIC18F2XJ11	PIC18F4XJ11	---- -000	---- -u00	---- -uuu
DSWAKEH(6)	PIC18F2XJ11	PIC18F4XJ11	---- ---0	---- ---0	---- ---u
DSWAKEL(6)	PIC18F2XJ11	PIC18F4XJ11	0-00 00-1	0-00 00-0	u-uu uu-u
ANCON1	PIC18F2XJ11	PIC18F4XJ11	00-0 0000	00-0 0000	uu-u uuuu
ANCON0	PIC18F2XJ11	PIC18F4XJ11	0000 0000	0000 0000	uuuu uuuu
ODCON1	PIC18F2XJ11	PIC18F4XJ11	---- --00	---- --uu	---- --uu
ODCON2	PIC18F2XJ11	PIC18F4XJ11	---- --00	---- --uu	---- --uu
ODCON3	PIC18F2XJ11	PIC18F4XJ11	---- --00	---- --uu	---- --uu
RTCCFG	PIC18F2XJ11	PIC18F4XJ11	0-00 0000	u-uu uuuu	u-uu uuuu
RTCCAL	PIC18F2XJ11	PIC18F4XJ11	0000 0000	uuuu uuuu	uuuu uuuu
REFOCON	PIC18F2XJ11	PIC18F4XJ11	0-00 0000	0-00 0000	u-uu uuuu
PADCFG1	PIC18F2XJ11	PIC18F4XJ11	---- -000	---- -000	---- -uuu
PPSCON	PIC18F2XJ11	PIC18F4XJ11	---- ---0	---- ---0	---- ---u
RPINR24	PIC18F2XJ11	PIC18F4XJ11	---1 1111	---1 1111	---u uuuu
RPINR23	PIC18F2XJ11	PIC18F4XJ11	---1 1111	---1 1111	---u uuuu
RPINR22	PIC18F2XJ11	PIC18F4XJ11	---1 1111	---1 1111	---u uuuu
RPINR21	PIC18F2XJ11	PIC18F4XJ11	---1 1111	---1 1111	---u uuuu
RPINR17	PIC18F2XJ11	PIC18F4XJ11	---1 1111	---1 1111	---u uuuu
RPINR16	PIC18F2XJ11	PIC18F4XJ11	---1 1111	---1 1111	---u uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition.

Note 1: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 5-1 for Reset value for specific condition.

5: Not implemented for PIC18F2XJ11 devices.

6: Not implemented on "LF" devices.

6.2.3 INSTRUCTIONS IN PROGRAM MEMORY

The program memory is addressed in bytes. Instructions are stored as 2 bytes or 4 bytes in program memory. The Least Significant Byte (LSB) of an instruction word is always stored in a program memory location with an even address (LSB = 0). To maintain alignment with instruction boundaries, the PC increments in steps of 2 and the LSB will always read '0' (see **Section 6.1.3 "Program Counter"**).

Figure 6-5 provides an example of how instruction words are stored in the program memory.

The CALL and GOTO instructions have the absolute program memory address embedded into the instruction. Since instructions are always stored on word boundaries, the data contained in the instruction is a word address. The word address is written to PC<20:1>, which accesses the desired byte address in program memory. Instruction #2 in Figure 6-5 displays how the instruction, GOTO 0006h, is encoded in the program memory. Program branch instructions, which encode a relative address offset, operate in the same manner. The offset value stored in a branch instruction represents the number of single-word instructions that the PC will be offset by. **Section 27.0 "Instruction Set Summary"** provides further details of the instruction set.

FIGURE 6-5: INSTRUCTIONS IN PROGRAM MEMORY

Program Memory Byte Locations →

			LSB = 1	LSB = 0	Word Address ↓
					000000h
					000002h
					000004h
					000006h
Instruction 1:	MOVLW	055h	0Fh	55h	000008h
Instruction 2:	GOTO	0006h	EFh	03h	00000Ah
			F0h	00h	00000Ch
Instruction 3:	MOVFF	123h, 456h	C1h	23h	00000Eh
			F4h	56h	000010h
					000012h
					000014h

6.2.4 TWO-WORD INSTRUCTIONS

The standard PIC18 instruction set has four two-word instructions: CALL, MOVFF, GOTO and LSFR. In all cases, the second word of the instructions always has '1111' as its four Most Significant bits (MSbs); the other 12 bits are literal data, usually a data memory address.

The use of '1111' in the 4 MSbs of an instruction specifies a special form of NOP. If the instruction is executed in proper sequence immediately after the first word, the data in the second word is accessed and used by the instruction sequence. If the first word is skipped for some reason, and the second word is executed by itself, a NOP is executed instead. This is necessary for cases when the two-word instruction is preceded by a conditional instruction that changes the PC. Example 6-4 illustrates how this works.

Note:	See **Section 6.5 "Program Memory and the Extended Instruction Set"** for information on two-word instructions in the extended instruction set.

EXAMPLE 6-4: TWO-WORD INSTRUCTIONS

CASE 1:

Object Code	Source Code		
0110 0110 0000 0000	TSTFSZ	REG1	; is RAM location 0?
1100 0001 0010 0011	MOVFF	REG1, REG2	; No, skip this word
1111 0100 0101 0110			; Execute this word as a NOP
0010 0100 0000 0000	ADDWF	REG3	; continue code

CASE 2:

Object Code	Source Code		
0110 0110 0000 0000	TSTFSZ	REG1	; is RAM location 0?
1100 0001 0010 0011	MOVFF	REG1, REG2	; Yes, execute this word
1111 0100 0101 0110			; 2nd word of instruction
0010 0100 0000 0000	ADDWF	REG3	; continue code

TABLE 6-3: NON-ACCESS BANK SPECIAL FUNCTION REGISTER MAP

Address	Name	Address	Name	Address	Name	Address	Name	Address	Name
F5Fh	PMCONH(1)	F3Fh	RTCCFG	F1Fh	—	EFFh	PPSCON	EDFh	—
F5Eh	PMCONL(1)	F3Eh	RTCCAL	F1Eh	—	EFEh	RPINR24	EDEh	RPOR24(1)
F5Dh	PMMODEH(1)	F3Dh	REFOCON	F1Dh	—	EFDh	RPINR23	EDDh	RPOR23(1)
F5Ch	PMMODEL(1)	F3Ch	PADCFG1	F1Ch	—	EFCh	RPINR22	EDCh	RPOR22(1)
F5Bh	PMDOUT2H(1)	F3Bh	—	F1Bh	—	EFBh	RPINR21	EDBh	RPOR21(1)
F5Ah	PMDOUT2L(1)	F3Ah	—	F1Ah	—	EFAh	—	EDAh	RPOR20(1)
F59h	PMDIN2H(1)	F39h	—	F19h	—	EF9h	—	ED9h	RPOR19(1)
F58h	PMDIN2L(1)	F38h	—	F18h	—	EF8h	—	ED8h	RPOR18
F57h	PMEH(1)	F37h	—	F17h	—	EF7h	RPINR17	ED7h	RPOR17
F56h	PMEL(1)	F36h	—	F16h	—	EF6h	RPINR16	ED6h	RPOR16
F55h	PMSTATH(1)	F35h	—	F15h	—	EF5h	—	ED5h	RPOR15
F54h	PMSTATL(1)	F34h	—	F14h	—	EF4h	—	ED4h	RPOR14
F53h	CVRCON	F33h	—	F13h	—	EF3h	—	ED3h	RPOR13
F52h	TCLKCON	F32h	—	F12h	—	EF2h	—	ED2h	RPOR12
F51h	—	F31h	—	F11h	—	EF1h	—	ED1h	RPOR11
F50h	—	F30h	—	F10h	—	EF0h	—	ED0h	RPOR10
F4Fh	DSGPR1(2)	F2Fh	—	F0Fh	—	EEFh	—	ECFh	RPOR9
F4Eh	DSGPR0(2)	F2Eh	—	F0Eh	—	EEEh	RPINR8	ECEh	RPOR8
F4Dh	DSCONH(2)	F2Dh	—	F0Dh	—	EEDh	RPINR7	ECDh	RPOR7
F4Ch	DSCONL(2)	F2Ch	—	F0Ch	—	EECh	RPINR6	ECCh	RPOR6
F4Bh	DSWAKEH(2)	F2Bh	—	F0Bh	—	EEBh	—	ECBh	RPOR5
F4Ah	DSWAKEL(2)	F2Ah	—	F0Ah	—	EEAh	RPINR4	ECAh	RPOR4
F49h	ANCON1	F29h	—	F09h	—	EE9h	RPINR3	EC9h	RPOR3
F48h	ANCON0	F28h	—	F08h	—	EE8h	RPINR2	EC8h	RPOR2
F47h	—	F27h	—	F07h	—	EE7h	RPINR1	EC7h	RPOR1
F46h	—	F26h	—	F06h	—	EE6h	—	EC6h	RPOR0
F45h	—	F25h	—	F05h	—	EE5h	—	EC5h	—
F44h	—	F24h	—	F04h	—	EE4h	—	EC4h	—
F43h	—	F23h	—	F03h	—	EE3h	—	EC3h	—
F42h	ODCON1	F22h	—	F02h	—	EE2h	—	EC2h	—
F41h	ODCON2	F21h	—	F01h	—	EE1h	—	EC1h	—
F40h	ODCON3	F20h	—	F00h	—	EE0h	—	EC0h	—

Note 1: This register is not available on 28-pin devices.
2: Deep Sleep registers are not available on LF devices.

TABLE 6-4: REGISTER FILE SUMMARY (PIC18F46J11 FAMILY)

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on Page:
TOSU	—	—	—	Top-of-Stack Upper Byte (TOS<20:16>)					---0 0000	69, 81
TOSH	Top-of-Stack High Byte (TOS<15:8>)								0000 0000	69, 79
TOSL	Top-of-Stack Low Byte (TOS<7:0>)								0000 0000	69, 79
STKPTR	STKFUL	STKUNF	—	SP4	SP3	SP2	SP1	SP0	00-0 0000	69, 80
PCLATU	—	—	bit 21(1)	Holding Register for PC<20:16>					---0 0000	69, 79
PCLATH	Holding Register for PC<15:8>								0000 0000	69, 79
PCL	PC Low Byte (PC<7:0>)								0000 0000	69, 79
TBLPTRU	—	—	bit 21	Program Memory Table Pointer Upper Byte (TBLPTR<20:16>)					--00 0000	69, 112
TBLPTRH	Program Memory Table Pointer High Byte (TBLPTR<15:8>)								0000 0000	69, 112
TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								0000 0000	69, 112
TABLAT	Program Memory Table Latch								0000 0000	69, 112
PRODH	Product Register High Byte								xxxx xxxx	69, 69
PRODL	Product Register Low Byte								xxxx xxxx	69, 113
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	69, 117
INTCON2	$\overline{\text{RBPU}}$	INTEDG0	INTEDG1	INTEDG2	INTEDG3	TMR0IP	INT3IP	RBIP	1111 1111	69, 118
INTCON3	INT2IP	INT1IP	INT3IE	INT2IE	INT1IE	INT3IF	INT2IF	INT1IF	1100 0000	69, 119
INDF0	Uses contents of FSR0 to address data memory – value of FSR0 not changed (not a physical register)								**N/A**	69, 98
POSTINC0	Uses contents of FSR0 to address data memory – value of FSR0 post-incremented (not a physical register)								**N/A**	69, 99
POSTDEC0	Uses contents of FSR0 to address data memory – value of FSR0 post-decremented (not a physical register)								**N/A**	69, 99
PREINC0	Uses contents of FSR0 to address data memory – value of FSR0 pre-incremented (not a physical register)								**N/A**	69, 99
PLUSW0	Uses contents of FSR0 to address data memory – value of FSR0 pre-incremented (not a physical register) – value of FSR0 offset by W								**N/A**	69, 99
FSR0H	—	—	—	—	Indirect Data Memory Address Pointer 0 High Byte				---- 0000	69, 98
FSR0L	Indirect Data Memory Address Pointer 0 Low Byte								xxxx xxxx	69, 98
WREG	Working Register								xxxx xxxx	69, 81
INDF1	Uses contents of FSR1 to address data memory – value of FSR1 not changed (not a physical register)								**N/A**	69, 98
POSTINC1	Uses contents of FSR1 to address data memory – value of FSR1 post-incremented (not a physical register)								**N/A**	69, 99
POSTDEC1	Uses contents of FSR1 to address data memory – value of FSR1 post-decremented (not a physical register)								**N/A**	69, 99
PREINC1	Uses contents of FSR1 to address data memory – value of FSR1 pre-incremented (not a physical register)								**N/A**	69, 99
PLUSW1	Uses contents of FSR1 to address data memory – value of FSR1 pre-incremented (not a physical register) – value of FSR1 offset by W								**N/A**	69, 99
FSR1H	—	—	—	—	Indirect Data Memory Address Pointer 1 High Byte				---- 0000	69, 98
FSR1L	Indirect Data Memory Address Pointer 1 Low Byte								xxxx xxxx	69, 98
BSR	—	—	—	—	Bank Select Register				---- 0000	69, 84
INDF2	Uses contents of FSR2 to address data memory – value of FSR2 not changed (not a physical register)								**N/A**	69, 98
POSTINC2	Uses contents of FSR2 to address data memory – value of FSR2 post-incremented (not a physical register)								**N/A**	70, 99
POSTDEC2	Uses contents of FSR2 to address data memory – value of FSR2 post-decremented (not a physical register)								**N/A**	70, 99
PREINC2	Uses contents of FSR2 to address data memory – value of FSR2 pre-incremented (not a physical register)								**N/A**	70, 99
PLUSW2	Uses contents of FSR2 to address data memory – value of FSR2 pre-incremented (not a physical register) – value of FSR2 offset by W								**N/A**	70, 99
FSR2H	—	—	—	—	Indirect Data Memory Address Pointer 2 High Byte				---- 0000	70, 98
FSR2L	Indirect Data Memory Address Pointer 2 Low Byte								xxxx xxxx	70, 98

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition, r = reserved. **Bold** indicates shared access SFRs.

Note 1: Bit 21 of the PC is only available in Serial Programming (SP) modes.

2: Reset value is '0' when Two-Speed Start-up is enabled and '1' if disabled.

3: The SSPxMSK registers are only accessible when SSPxCON2<3:0> = 1001.

4: Alternate names and definitions for these bits when the MSSP module is operating in I^2C™ Slave mode. See **Section 19.5.3.2 "Address Masking Modes"** for details.

5: These bits and/or registers are only available in 44-pin devices; otherwise, they are unimplemented and read as '0'. Reset values are shown for 44-pin devices.

6: The PMADDRH/PMDOUT1H and PMADDRL/PMDOUT1L register pairs share the same physical registers and addresses, but have different functions determined by the module's operating mode. See **Section 11.1.2 "Data Registers"** for more information.

13.0 TIMER1 MODULE

The Timer1 timer/counter module incorporates these features:

- Software selectable operation as a 16-bit timer or counter
- Readable and writable 8-bit registers (TMR1H and TMR1L)
- Selectable clock source (internal or external) with device clock or Timer1 oscillator internal options
- Interrupt-on-overflow
- Reset on ECCP Special Event Trigger
- Device clock status flag (T1RUN)
- Timer with gated control

Figure 13-1 displays a simplified block diagram of the Timer1 module.

The module incorporates its own low-power oscillator to provide an additional clocking option. The Timer1 oscillator can also be used as a low-power clock source for the microcontroller in power-managed operation.

Timer1 is controlled through the T1CON Control register (Register 13-1). It also contains the Timer1 oscillator Enable bit (T1OSCEN). Timer1 can be enabled or disabled by setting or clearing control bit, TMR1ON (T1CON<0>).

The FOSC clock source (TMR1CS<1:0> = 01) should not be used with the ECCP capture/compare features. If the timer will be used with the capture or compare features, always select one of the other timer clocking options.

REGISTER 13-1: T1CON: TIMER1 CONTROL REGISTER (ACCESS FCDh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	RD16	TMR1ON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **TMR1CS<1:0>:** Timer1 Clock Source Select bits
10 = Timer1 clock source is T1OSC or T1CKI pin
01 = Timer1 clock source is system clock (FOSC)(1)
00 = Timer1 clock source is instruction clock (FOSC/4)

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3 **T1OSCEN:** Timer1 Crystal Oscillator Enable bit
1 = Timer1 oscillator circuit enabled
0 = Timer1 oscillator circuit disabled
The oscillator inverter and feedback resistor are turned off to eliminate power drain.

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 External Clock Input Synchronization Select bit
TMR1CS<1:0> = 10:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
TMR1CS<1:0> = 0x:
This bit is ignored. Timer1 uses the internal clock when TMR1CS<1:0> = 0x.

bit 1 **RD16:** 16-Bit Read/Write Mode Enable bit
1 = Enables register read/write of Timer1 in one 16-bit operation
0 = Enables register read/write of Timer1 in two 8-bit operations

bit 0 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

Note 1: The FOSC clock source should not be selected if the timer will be used with the ECCP capture/compare features.

FIGURE 13-7: TIMER1 GATE SINGLE PULSE AND TOGGLE COMBINED MODE

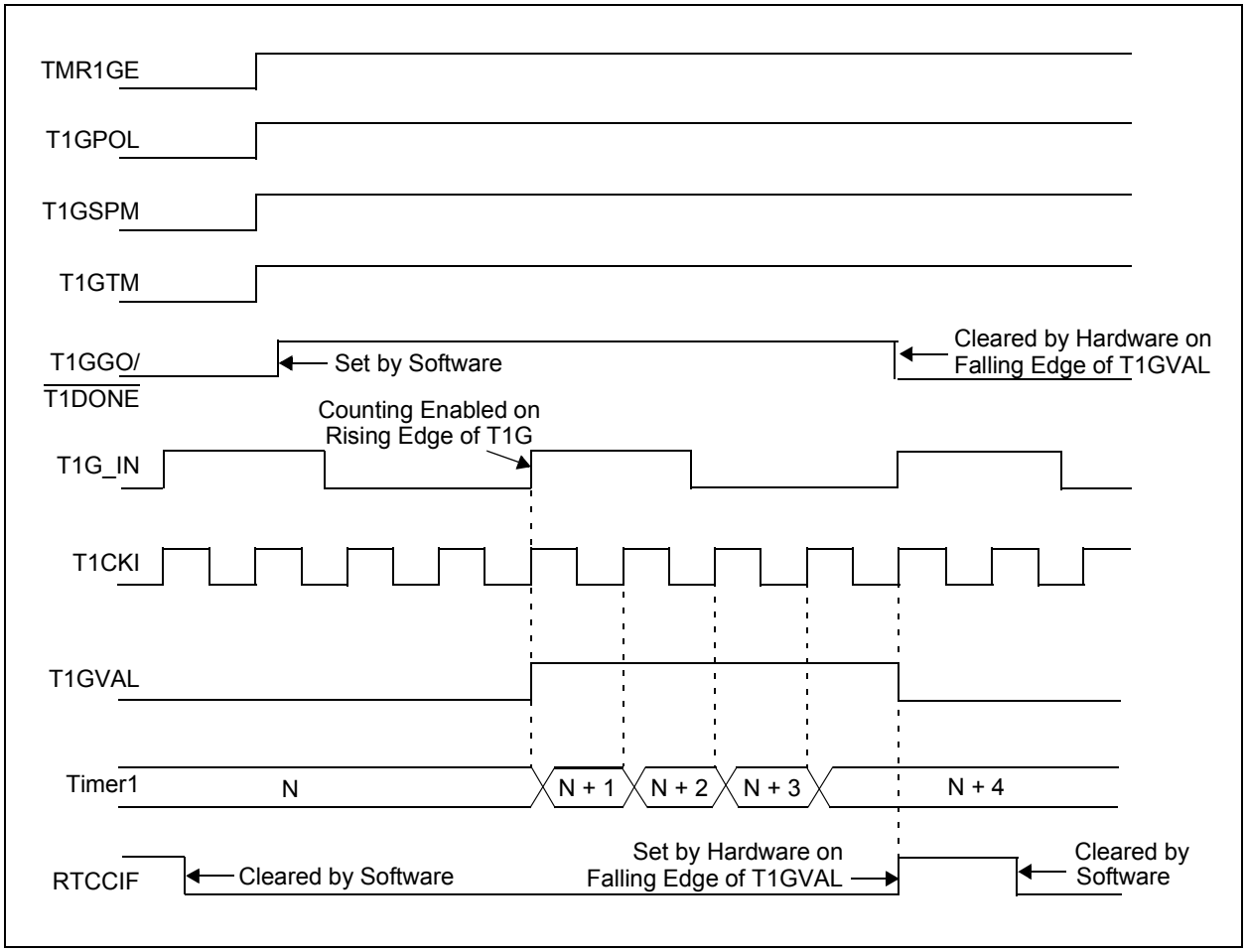


TABLE 13-5: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	90
PIR1	PMPIF(1)	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	92
PIE1	PMPIE(1)	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	92
IPR1	PMPIP(1)	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	92
TMR1L	Timer1 Register Low Byte								91
TMR1H	Timer1 Register High Byte								91
T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	RD16	TMR1ON	91
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{T1DONE}}$	T1GVAL	T1GSS1	T1GSS0	92
TCLKCON	—	—	—	T1RUN	—	—	T3CCP2	T3CCP1	94

Legend: Shaded cells are not used by the Timer1 module.

Note 1: These bits are only available in 44-pin devices.

REGISTER 18-1: CCPxCON: ECCPx CONTROL (ACCESS FBAh/FB4h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PxM1	PxM0	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **PxM<1:0>:** Enhanced PWM Output Configuration bits

If CCPxM<3:2> = 00, 01, 10:

xx = PxA assigned as capture/compare input/output; PxB, PxC and PxD assigned as port pins

If CCPxM<3:2> = 11:

00 = Single output: PxA, PxB, PxC and PxD controlled by steering (see **Section 18.5.7 "Pulse Steering Mode"**)

01 = Full-bridge output forward: PxD modulated; PxA active; PxB, PxC inactive

10 = Half-bridge output: PxA, PxB modulated with dead-band control; PxC and PxD assigned as port pins

11 = Full-bridge output reverse: PxB modulated; PxC active; PxA and PxD inactive

bit 5-4 **DCxB<1:0>**: PWM Duty Cycle bit 1 and bit 0

Capture mode:
Unused.

Compare mode:
Unused.

PWM mode:
These bits are the two LSbs of the 10-bit PWM duty cycle. The eight MSbs of the duty cycle are found in CCPRxL.

bit 3-0 **CCPxM<3:0>**: ECCPx Mode Select bits

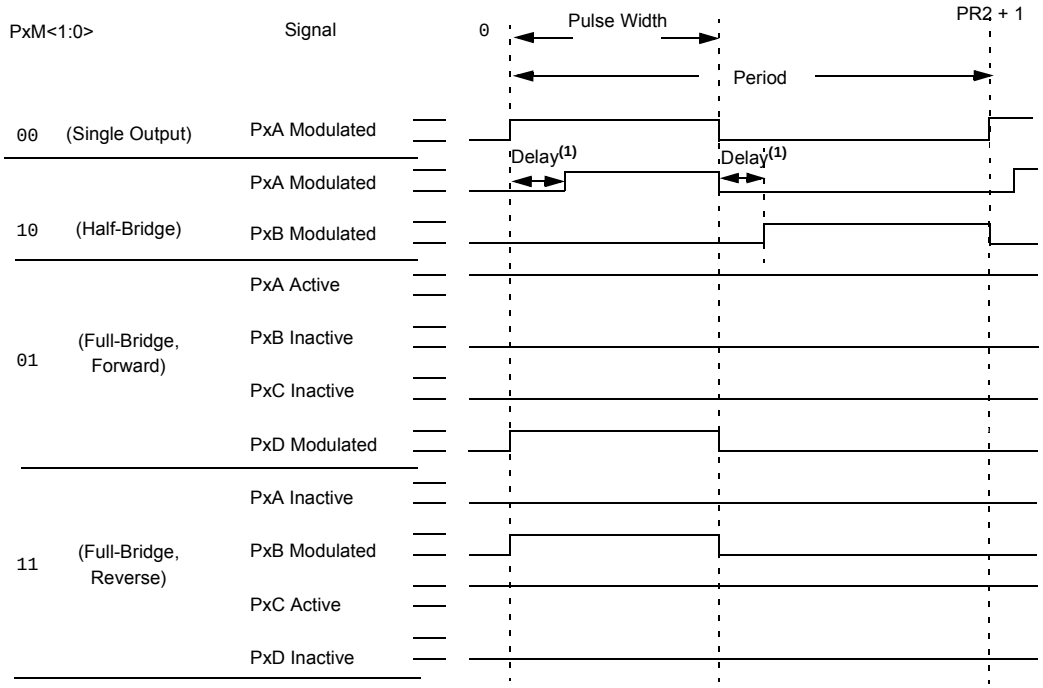
0000 = Capture/Compare/PWM off (resets ECCPx module)
0001 = Reserved
0010 = Compare mode, toggle output on match
0011 = Capture mode
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, initialize ECCPx pin low, set output on compare match (set CCPxIF)
1001 = Compare mode, initialize ECCPx pin high, clear output on compare match (set CCPxIF)
1010 = Compare mode, generate software interrupt only, ECCPx pin reverts to I/O state
1011 = Compare mode, trigger special event (ECCPx resets TMR1 or TMR3, starts A/D conversion, sets CCxIF bit)
1100 = PWM mode; PxA and PxC active-high; PxB and PxD active-high
1101 = PWM mode; PxA and PxC active-high; PxB and PxD active-low
1110 = PWM mode; PxA and PxC active-low; PxB and PxD active-high
1111 = PWM mode; PxA and PxC active-low; PxB and PxD active-low

TABLE 18-4: EXAMPLE PIN ASSIGNMENTS FOR VARIOUS PWM ENHANCED MODES

ECCP Mode	PxM<1:0>	PxA	PxB	PxC	PxD
Single	00	Yes(1)	Yes(1)	Yes(1)	Yes(1)
Half-Bridge	10	Yes	Yes	No	No
Full-Bridge, Forward	01	Yes	Yes	Yes	Yes
Full-Bridge, Reverse	11	Yes	Yes	Yes	Yes

Note 1: Outputs are enabled by pulse steering in Single mode (see Register 18-4).

FIGURE 18-6: EXAMPLE PWM (ENHANCED MODE) OUTPUT RELATIONSHIPS (ACTIVE-HIGH STATE)



Relationships:

- Period = 4 * Tosc * (PR2 + 1) * (TMR2 Prescale Value)
- Pulse Width = Tosc * (CCPRxL<7:0>:CCPxCON<5:4>) * (TMR2 Prescale Value)
- Delay = 4 * Tosc * (ECCPxDEL<6:0>)

Note 1: Dead-band delay is programmed using the ECCPxDEL register (**Section 18.5.6 "Programmable Dead-Band Delay Mode"**).

REGISTER 19-7: SSPxCON2: MSSPx CONTROL REGISTER 2 –I²C™ MASTER MODE (ACCESS FC5h/F71h)

R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GCEN(3)	ACKSTAT	ACKDT(1)	ACKEN(2)	RCEN(2)	PEN(2)	RSEN(2)	SEN(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **GCEN:** General Call Enable bit (Slave mode only)(3)
1 = Enable interrupt when a general call address (0000h) is received in the SSPxSR
0 = General call address disabled

bit 6 **ACKSTAT:** Acknowledge Status bit (Master Transmit mode only)
1 = Acknowledge was not received from slave
0 = Acknowledge was received from slave

bit 5 **ACKDT:** Acknowledge Data bit (Master Receive mode only)(1)
1 = Not Acknowledge
0 = Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit(2)
1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit; automatically cleared by hardware
0 = Acknowledge sequence Idle

bit 3 **RCEN:** Receive Enable bit (Master Receive mode only)(2)
1 = Enables Receive mode for I²C
0 = Receive Idle

bit 2 **PEN:** Stop Condition Enable bit(2)
1 = Initiates Stop condition on SDAx and SCLx pins; automatically cleared by hardware
0 = Stop condition Idle

bit 1 **RSEN:** Repeated Start Condition Enable bit(2)
1 = Initiates Repeated Start condition on SDAx and SCLx pins; automatically cleared by hardware
0 = Repeated Start condition Idle

bit 0 **SEN:** Start Condition Enable bit(2)
1 = Initiates Start condition on SDAx and SCLx pins; automatically cleared by hardware
0 = Start condition Idle

Note 1: Value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.
2: If the I²C module is active, these bits may not be set (no spooling) and the SSPxBUF may not be written (or writes to the SSPxBUF are disabled).
3: This bit is not implemented in I²C Master mode.

REGISTER 20-3: BAUDCONx: BAUD RATE CONTROL REGISTER (ACCESS F7Eh/F7Ch)

R/W-0	R-1	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ABDOVF:** Auto-Baud Acquisition Rollover Status bit
1 = A BRG rollover has occurred during Auto-Baud Rate Detect mode (must be cleared in software)
0 = No BRG rollover has occurred

bit 6 **RCIDL:** Receive Operation Idle Status bit
1 = Receive operation is Idle
0 = Receive operation is active

bit 5 **RXDTP:** Data/Receive Polarity Select bit
Asynchronous mode:
1 = Receive data (RXx) is inverted (active-low)
0 = Receive data (RXx) is not inverted (active-high)
Synchronous mode:
1 = Data (DTx) is inverted (active-low)
0 = Data (DTx) is not inverted (active-high)

bit 4 **TXCKP:** Synchronous Clock Polarity Select bit
Asynchronous mode:
1 = Idle state for transmit (TXx) is a low level
0 = Idle state for transmit (TXx) is a high level
Synchronous mode:
1 = Idle state for clock (CKx) is a high level
0 = Idle state for clock (CKx) is a low level

bit 3 **BRG16:** 16-Bit Baud Rate Register Enable bit
1 = 16-bit Baud Rate Generator – SPBRGHx and SPBRGx
0 = 8-bit Baud Rate Generator – SPBRGx only (Compatible mode), SPBRGHx value ignored

bit 2 **Unimplemented:** Read as '0'

bit 1 **WUE:** Wake-up Enable bit
Asynchronous mode:
1 = EUSART will continue to sample the RXx pin – interrupt generated on falling edge; bit cleared in hardware on following rising edge
0 = RXx pin not monitored or rising edge detected
Synchronous mode:
Unused in this mode.

bit 0 **ABDEN:** Auto-Baud Detect Enable bit
Asynchronous mode:
1 = Enable baud rate measurement on the next character; requires reception of a Sync field (55h); cleared in hardware upon completion
0 = Baud rate measurement disabled or completed
Synchronous mode:
Unused in this mode.

25.1 CTMU Operation

The CTMU works by using a fixed current source to charge a circuit. The type of circuit depends on the type of measurement being made. In the case of charge measurement, the current is fixed, and the amount of time the current is applied to the circuit is fixed. The amount of voltage read by the A/D is then a measurement of the capacitance of the circuit. In the case of time measurement, the current, as well as the capacitance of the circuit, is fixed. In this case, the voltage read by the A/D is then representative of the amount of time elapsed from the time the current source starts and stops charging the circuit.

If the CTMU is being used as a time delay, both capacitance and current source are fixed, as well as the voltage supplied to the comparator circuit. The delay of a signal is determined by the amount of time it takes the voltage to charge to the comparator threshold voltage.

25.1.1 THEORY OF OPERATION

The operation of the CTMU is based on the equation for charge:

$$I = C \cdot \frac{dV}{dT}$$

More simply, the amount of charge measured in coulombs in a circuit is defined as current in amperes (I) multiplied by the amount of time in seconds that the current flows (t). Charge is also defined as the capacitance in farads (C) multiplied by the voltage of the circuit (V). It follows that:

$$I \cdot t = C \cdot V.$$

The CTMU module provides a constant, known current source. The A/D Converter is used to measure (V) in the equation, leaving two unknowns: capacitance (C) and time (t). The above equation can be used to calculate capacitance or time, by either the relationship using the known fixed capacitance of the circuit:

$$t = (C \cdot V)/I$$

or by:

$$C = (I \cdot t)/V$$

using a fixed time that the current source is applied to the circuit.

25.1.2 CURRENT SOURCE

At the heart of the CTMU is a precision current source, designed to provide a constant reference for measurements. The level of current is user-selectable across three ranges or a total of two orders of magnitude, with the ability to trim the output in ±2% increments (nominal). The current range is selected by the IRNG<1:0> bits (CTMUICON<1:0>), with a value of '01' representing the lowest range.

Current trim is provided by the ITRIM<5:0> bits (CTMUICON<7:2>). These six bits allow trimming of the current source in steps of approximately 2% per step. Note that half of the range adjusts the current source positively and the other half reduces the current source. A value of '000000' is the neutral position (no change). A value of '100001' is the maximum negative adjustment (approximately -62%) and '011111' is the maximum positive adjustment (approximately +62%).

25.1.3 EDGE SELECTION AND CONTROL

CTMU measurements are controlled by edge events occurring on the module's two input channels. Each channel, referred to as Edge 1 and Edge 2, can be configured to receive input pulses from one of the edge input pins (CTED1 and CTED2) or ECCPx Special Event Triggers. The input channels are level-sensitive, responding to the instantaneous level on the channel rather than a transition between levels. The inputs are selected using the EDG1SEL and EDG2SEL bit pairs (CTMUCONL<3:2 and 6:5>).

In addition to source, each channel can be configured for event polarity using the EDGE2POL and EDGE1POL bits (CTMUCONL<7,4>). The input channels can also be filtered for an edge event sequence (Edge 1 occurring before Edge 2) by setting the EDGSEQEN bit (CTMUCONH<2>).

25.1.4 EDGE STATUS

The CTMUCONL register also contains two status bits: EDG2STAT and EDG1STAT (CTMUCONL<1:0>). Their primary function is to show if an edge response has occurred on the corresponding channel. The CTMU automatically sets a particular bit when an edge response is detected on its channel. The level-sensitive nature of the input channels also means that the status bits become set immediately if the channel's configuration is changed and is the same as the channel's current state.

The module uses the edge status bits to control the current source output to external analog modules (such as the A/D Converter). Current is only supplied to external modules when only one (but not both) of the status bits is set, and shuts current off when both bits are either set or cleared. This allows the CTMU to measure current only during the interval between edges. After both status bits are set, it is necessary to clear them before another measurement is taken. Both bits should be cleared simultaneously, if possible, to avoid re-enabling the CTMU current source.

In addition to being set by the CTMU hardware, the edge status bits can also be set by software. This is also the user's application to manually enable or disable the current source. Setting either one (but not both) of the bits enables the current source. Setting or clearing both bits at once disables the source.

TSTFSZ **Test f, Skip if 0**

Syntax: TSTFSZ f {,a}

Operands: $0 \le f \le 255$
$a \in [0,1]$

Operation: skip if f = 0

Status Affected: None

Encoding:

0110	011a	ffff	ffff

Description: If 'f' = 0, the next instruction fetched during the current instruction execution is discarded and a NOP is executed, making this a two-cycle instruction.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 27.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1(2)
Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:
```
HERE    TSTFSZ  CNT, 1
NZERO   :
ZERO    :
```
Before Instruction
PC = Address (HERE)
After Instruction
If CNT = 00h,
PC = Address (ZERO)
If CNT ≠ 00h,
PC = Address (NZERO)

XORLW **Exclusive OR Literal with W**

Syntax: XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → W

Status Affected: N, Z

Encoding:

0000	1010	kkkk	kkkk

Description: The contents of W are XORed with the 8-bit literal 'k'. The result is placed in W.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write to W

Example:
```
XORLW   0xAF
```
Before Instruction
W = B5h
After Instruction
W = 1Ah

29.2 DC Characteristics: Power-Down and Supply Current PIC18F46J11 Family (Industrial) (Continued)

PIC18LFXXJ11 Family		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18FXXJ11 Family		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (IDD)(2)						
	PIC18LFXXJ11	5.2	14.2	µA	-40°C	VDD = 2.0V, VDDCORE = 2.0V	FOSC = 31 kHz, **RC_RUN** mode, Internal RC Oscillator, INTSRC = 0
		6.2	14.2	µA	+25°C		
		8.6	19.0	µA	+85°C		
	PIC18LFXXJ11	7.6	16.5	µA	-40°C	VDD = 2.5V, VDDCORE = 2.5V	
		8.5	16.5	µA	+25°C		
		11.3	22.4	µA	+85°C		
	PIC18FXXJ11	37	77	µA	-40°C	VDD = 2.15V, VDDCORE = 10 µF Capacitor	
		48	77	µA	+25°C		
		60	93	µA	+85°C		
	PIC18FXXJ11	52	84	µA	-40°C	VDD = 3.3V, VDDCORE = 10 µF Capacitor	
		61	84	µA	+25°C		
		70	108	µA	+85°C		
	PIC18LFXXJ11	1.1	1.5	mA	-40°C	VDD = 2.0V, VDDCORE = 2.0V	FOSC = 4 MHz, **RC_RUN** mode, Internal RC Oscillator
		1.1	1.5	mA	+25°C		
		1.2	1.6	mA	+85°C		
	PIC18LFXXJ11	1.5	1.7	mA	-40°C	VDD = 2.5V, VDDCORE = 2.5V	
		1.6	1.7	mA	+25°C		
		1.6	1.9	mA	+85°C		
	PIC18FXXJ11	1.3	2.6	mA	-40°C	VDD = 2.15V, VDDCORE = 10 µF Capacitor	
		1.4	2.6	mA	+25°C		
		1.4	2.8	mA	+85°C		
	PIC18FXXJ11	1.6	2.9	mA	-40°C	VDD = 3.3V, VDDCORE = 10 µF Capacitor	
		1.6	2.9	mA	+25°C		
		1.6	3.0	mA	+85°C		

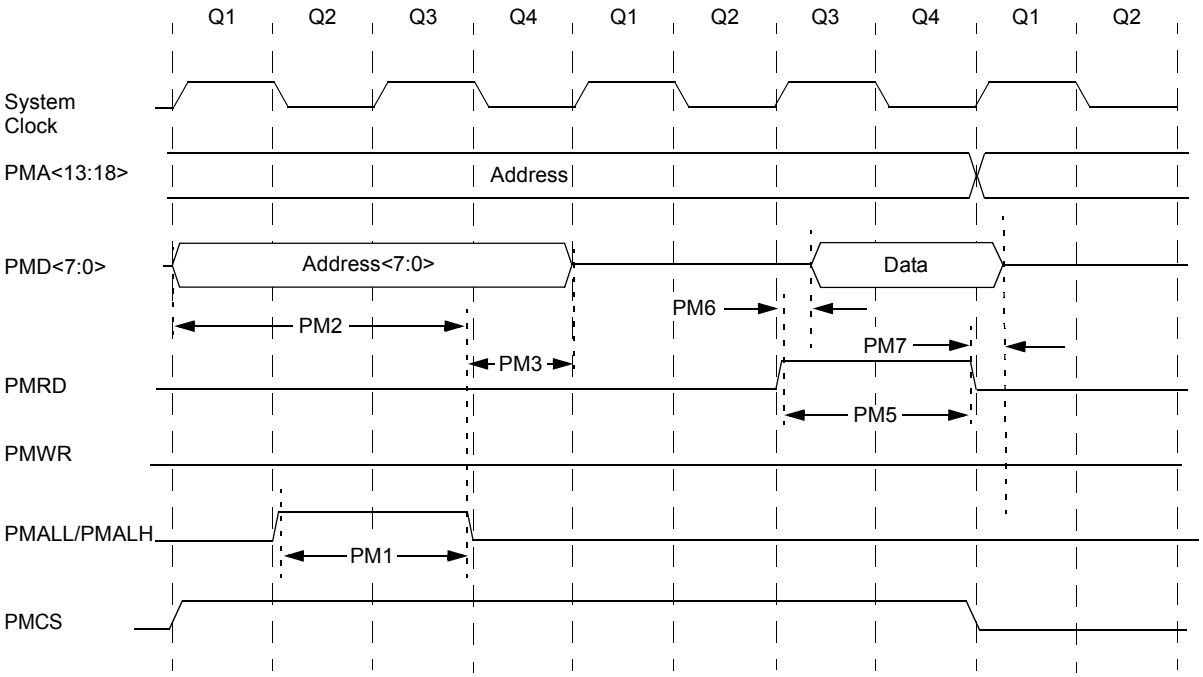
Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption. All features that add delta current are disabled (WDT, etc.). The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD/VSS;
$\overline{MCLR}$ = VDD; WDT disabled unless otherwise specified.

3: Low-Power Timer1 with standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

FIGURE 29-10: PARALLEL MASTER PORT READ TIMING DIAGRAM



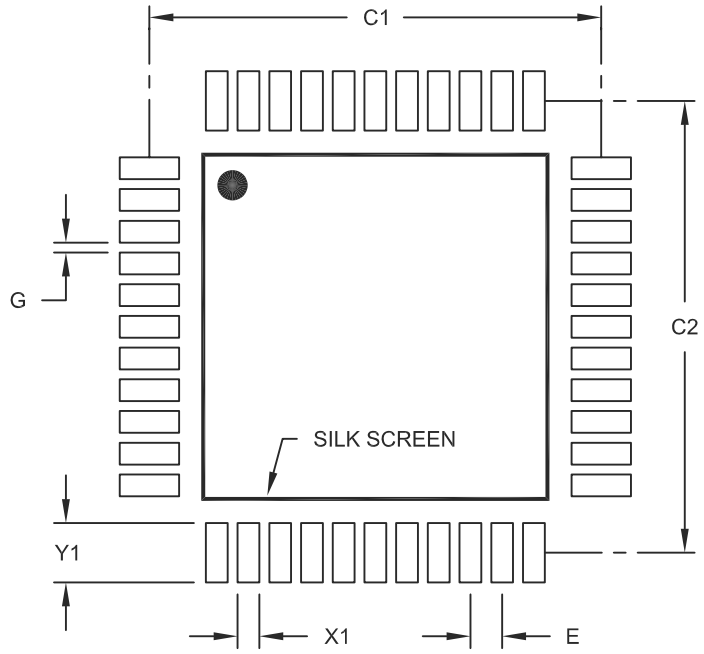
Operating Conditions: 2.0V < V_{DD} < 3.6V, -40°C < T_A < +85°C unless otherwise stated.

TABLE 29-17: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

Param. No	Symbol	Characteristics	Min	Typ	Max	Units
PM1		PMALL/PMALH Pulse Width	—	0.5 T_{CY}	—	ns
PM2		Address Out Valid to PMALL/PMALH Invalid (address setup time)	—	0.75 T_{CY}	—	ns
PM3		PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	0.25 T_{CY}	—	ns
PM5		PMRD Pulse Width	—	0.5 T_{CY}	—	ns
PM6		PMRD or PMENB Active to Data In Valid (data setup time)	—	—	—	ns
PM7		PMRD or PMENB Inactive to Data In Invalid (data hold time)	—	—	—	ns

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076A