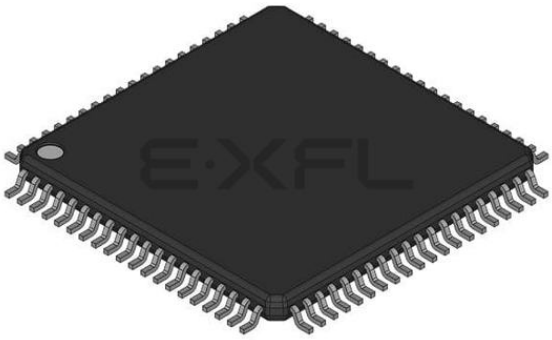

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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.75V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12e256cfue

List of Chapters

1.4.36 PS1 / TXD0 — Port S I/O Pin 1

PS1 is a general purpose input or output. When the Serial Communications Interface 0 (SCI0) transmitter is enabled the PS1 pin is configured as the transmit pin, TXD0, of SCI0. While in reset and immediately out of reset the PS1 pin is configured as a high impedance input pin. Consult Chapter 3, “Port Integration Module (PIM9E256V1) Block Description” and Chapter 8, “Serial Communication Interface (SCIV4) Block Description” for information about pin configurations.

1.4.37 PS0 / RXD0 — Port S I/O Pin 0

PS0 is a general purpose input or output. When the Serial Communications Interface 0 (SCI0) receiver is enabled the PS0 pin is configured as the receive pin RXD0 of SCI0. While in reset and immediately out of reset the PS0 pin is configured as a high impedance input pin. Consult Chapter 3, “Port Integration Module (PIM9E256V1) Block Description” and Chapter 8, “Serial Communication Interface (SCIV4) Block Description” for information about pin configurations.

1.4.38 PT[7:4] / IOC1[7:4]— Port T I/O Pins [7:4]

PT[7:4] are general purpose input or output pins. When the Timer system 1 (TIM1) is enabled they can also be configured as the TIM1 input capture or output compare pins IOC1[7-4]. While in reset and immediately out of reset the PT[7:4] pins are configured as a high impedance input pins. Consult Chapter 3, “Port Integration Module (PIM9E256V1) Block Description” and Chapter 13, “Timer (S12TIM16B4CV1) Block Description” for information about pin configurations.

1.4.39 PT[3:0] / IOC0[7:4]— Port T I/O Pins [3:0]

PT[3:0] are general purpose input or output pins. When the Timer system 0 (TIM0) is enabled they can also be configured as the TIM0 input capture or output compare pins IOC0[7-4]. While in reset and immediately out of reset the PT[3:0] pins are configured as a high impedance input pins. Consult Chapter 3, “Port Integration Module (PIM9E256V1) Block Description” and Chapter 13, “Timer (S12TIM16B4CV1) Block Description” for information about pin configurations.

1.4.40 PU[7:6] — Port U I/O Pins [7:6]

PU[7:6] are general purpose input or output pins. While in reset and immediately out of reset the PU[7:6] pins are configured as a high impedance input pins. Consult Chapter 3, “Port Integration Module (PIM9E256V1) Block Description” for information about pin configurations. PU[7:6] are not available in the 80 pin package version.

1.4.41 PU[5:4] / PW1[5:4] — Port U I/O Pins [5:4]

PU[5:4] are general purpose input or output pins. When the Pulse Width Modulator (PWM) is enabled the PU[5:4] output pins, individually or as a pair, can be configured as PW1[5:4] outputs. While in reset and immediately out of reset the PU[5:4] pins are configured as a high impedance input pins. Consult Chapter 3, “Port Integration Module (PIM9E256V1) Block Description” and Chapter 12, “Pulse-Width

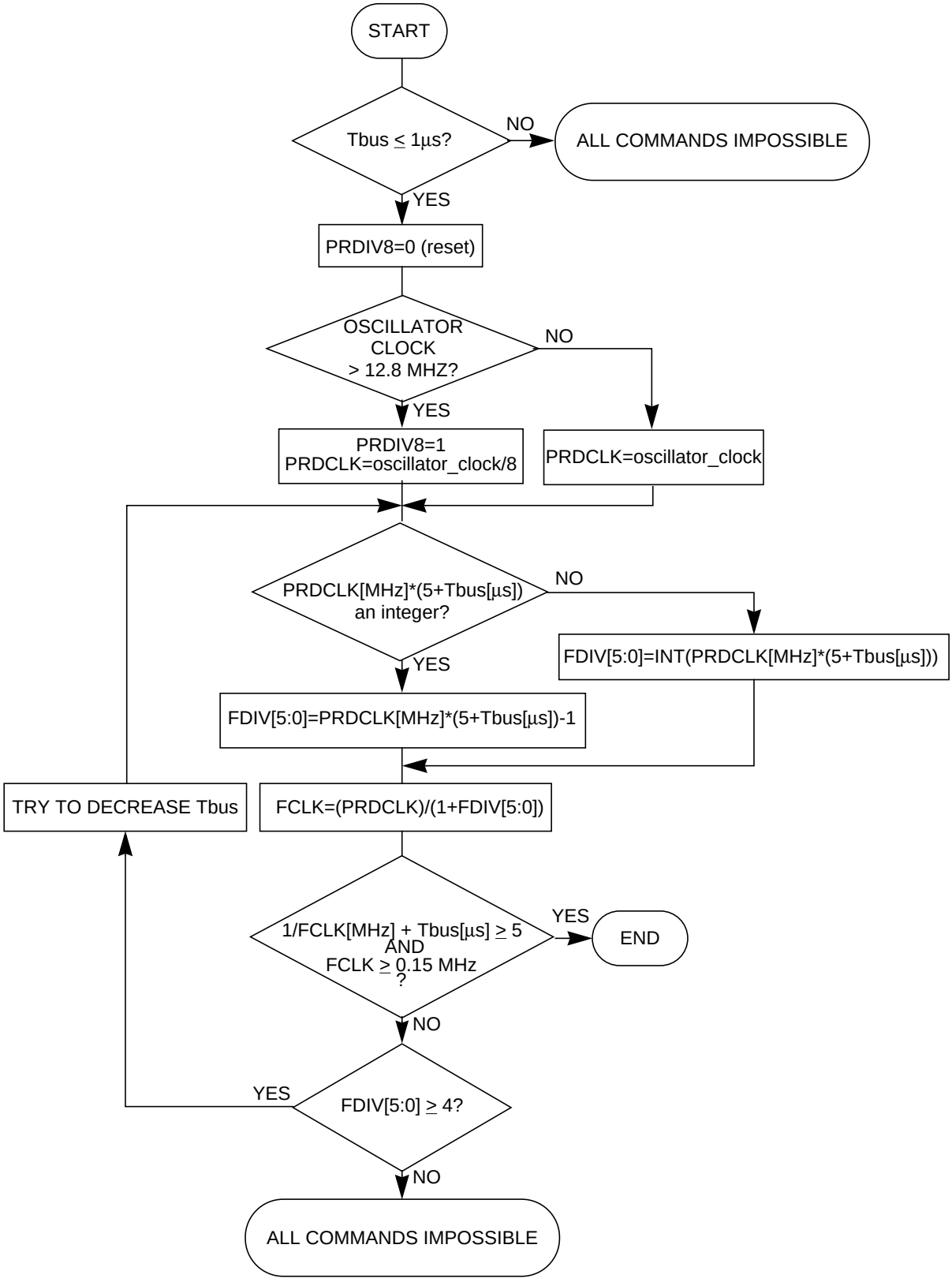

Figure 2-22. Determination Procedure for PRDIV8 and FDIV Bits

3.3.1.2 Port AD Input Register (PTIAD)

Module Base + 0x0032

	7	6	5	4	3	2	1	0
R	PTIAD15	PTIAD14	PTIAD13	PTIAD12	PTIAD11	PTIAD10	PTIAD9	PTIAD8
W								
Reset	1	1	1	1	1	1	1	1

Module Base + 0x0033

	7	6	5	4	3	2	1	0
R	PTIAD7	PTIAD6	PTIAD5	PTIAD4	PTIAD3	PTIAD2	PTIAD1	PTIAD0
W								
Reset	1	1	1	1	1	1	1	1

= Reserved or Unimplemented

Figure 3-3. Port AD Input Register (PTIAD)

Read: Anytime. Write: Never; writes to these registers have no effect.

If the ATDDIEN0(1) bit of the associated I/O pin is set to 0 (digital input buffer is disabled), a read returns a 1. If the ATDDIEN0(1) bit of the associated I/O pin is set to 1 (digital input buffer is enabled), a read returns the status of the associated pin.

3.3.4 Port Q

Port Q is associated with the Pulse Width Modulator (PMF) modules. Each pin is assigned according to the following priority: PMF > general-purpose I/O.

When a current status or fault function is enabled, the corresponding pin becomes an input. PQ[3:0] are connected to FAULT[3:0] inputs and PQ[6:4] are connected to $\overline{IS}$[2:0] inputs of the PMF module. Refer to the PMF block description chapter for information on enabling and disabling these PMF functions.

During reset, port Q pins are configured as high-impedance inputs.

3.3.4.1 Port Q I/O Register (PTQ)

Module Base + 0x0020

	7	6	5	4	3	2	1	0
R	0	PTQ5	PTQ5	PTQ4	PTQ3	PTQ2	PTQ1	PTQ0
W								
PMF:		$\overline{IS2}$	$\overline{IS1}$	$\overline{IS0}$	FAULT3	FAULT2	FAULT1	FAULT0
Reset	0	0	0	0	0	0	0	0

= Reserved or Unimplemented

Figure 3-23. Port Q I/O Register (PTQ)

Read: Anytime. Write: Anytime.

If the associated data direction bit (DDRQx) is set to 1 (output), a read returns the value of the I/O register bit. If the associated data direction bit (DDRQx) is set to 0 (input), a read returns the value of the pin.

3.3.4.2 Port Q Input Register (PTIQ)

Module Base + 0x0021

	7	6	5	4	3	2	1	0
R	0	PTIQ6	PTIQ5	PTIQ4	PTIQ3	PTIQ2	PTIQ1	PTIQ0
W								
Reset	0	u	u	u	u	u	u	u

= Reserved or Unimplemented u = Unaffected by reset

Figure 3-24. Port Q Input Register (PTIQ)

Read: Anytime. Write: Never, writes to this register have no effect.

This register always reads back the status of the associated pins.

3.3.7.4 Port U Reduced Drive Register (RDRU)

Module Base + 0x002B

	7	6	5	4	3	2	1	0
R W	RDRU7	RDRU6	RDRU5	RDRU4	RDRU3	RDRU2	RDRU1	RDRU0
Reset	0	0	0	0	0	0	0	0

Figure 3-45. Port U Reduced Drive Register (RDRU)

Read: Anytime. Write: Anytime.

This register configures the drive strength of configured output pins as either full or reduced. If a pin is configured as input, the corresponding Reduced Drive Register bit has no effect.

Table 3-32. RDRT Field Descriptions

Field	Description
7:0 RDRU[7:0]	**Reduced Drive Port U** 0 Full drive strength at output. 1 Associated pin drives at about 1/3 of the full drive strength.

3.3.7.5 Port U Pull Device Enable Register (PERU)

Module Base + 0x002C

	7	6	5	4	3	2	1	0
R W	PERU7	PERU6	PERU5	PERU4	PERU3	PERU2	PERU1	PERU0
Reset	0	0	0	0	0	0	0	0

Figure 3-46. Port T Pull Device Enable Register (PERT)

Read: Anytime. Write: Anytime.

This register configures whether a pull-up or a pull-down device is activated on configured input pins. If a pin is configured as output, the corresponding Pull Device Enable Register bit has no effect.

Table 3-33. PERT Field Descriptions

Field	Description
7:0 PERU[7:0]	**Pull Device Enable Port U** 0 Pull-up or pull-down device is disabled. 1 Pull-up or pull-down device is enabled.

6.3.2.12 ATD Input Enable Register 0 (ATDDIEN0)

Module Base + 0x000C

	7	6	5	4	3	2	1	0
R W	IEN15	IEN14	IEN13	IEN12	IEN11	IEN10	IEN9	IEN8
Reset	0	0	0	0	0	0	0	0

Figure 6-14. ATD Input Enable Register 0 (ATDDIEN0)

Read: Anytime

Write: anytime

Table 6-23. ATDDIEN0 Field Descriptions

Field	Description
7:0 IEN[15:8]	**ATD Digital Input Enable on Channel Bits** — This bit controls the digital input buffer from the analog input pin (ANx) to PTADx data register. 0 Disable digital input buffer to PTADx 1 Enable digital input buffer to PTADx. **Note:** Setting this bit will enable the corresponding digital input buffer continuously. If this bit is set while simultaneously using it as an analog port, there is potentially increased power consumption because the digital input buffer maybe in the linear region.

6.3.2.13 ATD Input Enable Register 1 (ATDDIEN1)

Module Base + 0x000D

	7	6	5	4	3	2	1	0
R W	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
Reset	0	0	0	0	0	0	0	0

Figure 6-15. ATD Input Enable Register 1 (ATDDIEN1)

Read: Anytime

Write: Anytime

Table 6-24. ATDDIEN1 Field Descriptions

Field	Description
7:0 IEN[7:0]	**ATD Digital Input Enable on Channel Bits** — This bit controls the digital input buffer from the analog input pin (ANx) to PTADx data register. 0 Disable digital input buffer to PTADx 1 Enable digital input buffer to PTADx. **Note:** Setting this bit will enable the corresponding digital input buffer continuously. If this bit is set while simultaneously using it as an analog port, there is potentially increased power consumption because the digital input buffer maybe in the linear region.

indicating that the received byte can be read. If the receive interrupt enable bit, RIE, in SCI control register 2 (SCICR2) is also set, the RDRF flag generates an RDRF interrupt request.

8.5.5.3 Data Sampling

The receiver samples the RXD pin at the RT clock rate. The RT clock is an internal signal with a frequency 16 times the baud rate. To adjust for baud rate mismatch, the RT clock (see Figure 8-15) is re-synchronized:

- After every start bit
- After the receiver detects a data bit change from logic 1 to logic 0 (after the majority of data bit samples at RT8, RT9, and RT10 returns a valid logic 1 and the majority of the next RT8, RT9, and RT10 samples returns a valid logic 0)

To locate the start bit, data recovery logic does an asynchronous search for a logic 0 preceded by three logic 1s. When the falling edge of a possible start bit occurs, the RT clock begins to count to 16.

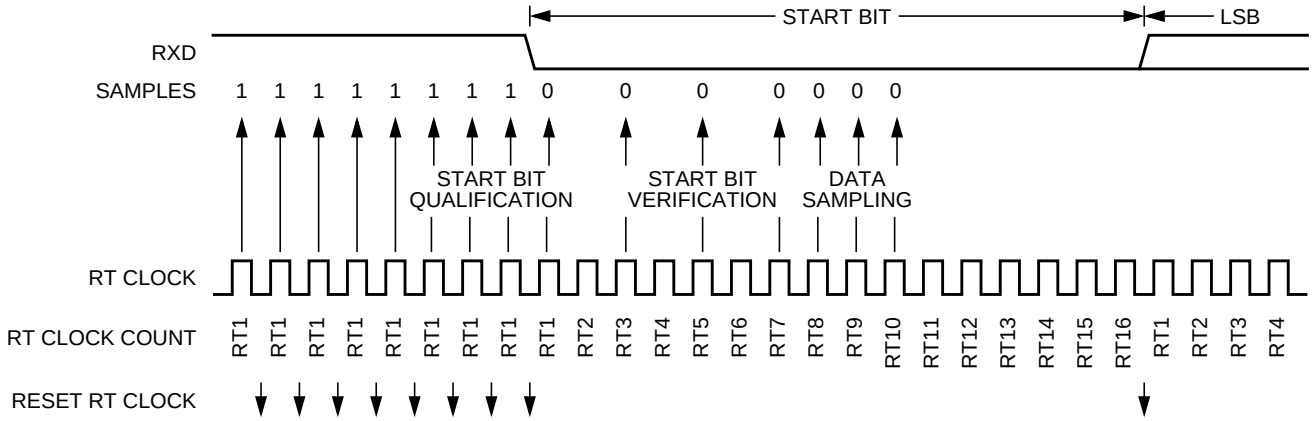

Figure 8-15. Receiver Data Sampling

To verify the start bit and to detect noise, data recovery logic takes samples at RT3, RT5, and RT7. Table 8-15 summarizes the results of the start bit verification samples.

Table 8-15. Start Bit Verification

RT3, RT5, and RT7 Samples	Start Bit Verification	Noise Flag
000	Yes	0
001	Yes	1
010	Yes	1
011	No	0
100	Yes	1
101	No	0
110	No	0
111	No	0

If start bit verification is not successful, the RT clock is reset and a new search for a start bit begins.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
$000E	PMFDTMS	R	0	0	DT5	DT4	DT3	DT2	DT1	DT0
		W								
$000F	PMFCCTL	R	0	0	ISENS		0	IPOLC	IPOLB	IPOLA
		W								
$0010	PMFVAL0	R	PMFVAL0							
		W								
$0011	PMFVAL0	R	PMFVAL0							
		W								
$0012	PMFVAL1	R	PMFVAL1							
		W								
$0013	PMFVAL1	R	PMFVAL1							
		W								
$0014	PMFVAL2	R	PMFVAL2							
		W								
$0015	PMFVAL2	R	PMFVAL2							
		W								
$0016	PMFVAL3	R	PMFVAL3							
		W								
$0017	PMFVAL3	R	PMFVAL3							
		W								
$0018	PMFVAL4	R	PMFVAL4							
		W								
$0019	PMFVAL4	R	PMFVAL4							
		W								
$001A	PMFVAL5	R	PMFVAL5							
		W								
$001B	PMFVAL5	R	PMFVAL5							
		W								
$001C–$001F	Reserved	R								
		W								
$0020	PMFENCA	R	PWMENA	0	0	0	0	0	LDOKA	PWMRIEA
		W								
$0021	PMFFQCA	R	LDFQA				HALFA	PRSCA		PWMRFA
		W								

= Unimplemented or Reserved

Figure 11-3. Quick Reference to PMF Registers (Sheet 2 of 4)

The 12-bit value written to this register is the number of PWM clock cycles in complementary channel operation. A reset sets the PWM deadtime register to a default value of 0x0FFF, selecting a deadtime of 4096-PWM clock cycles minus one bus clock cycle.

NOTE

Deadtime is affected by changes to the prescaler value. The deadtime duration is determined as follows: DT = P × PMFDTMC – 1, where DT is deadtime, P is the prescaler value, PMFDTMC is the programmed value of dead time. For example: if the prescaler is programmed for a divide-by-two and the PMFDTMC is set to five, then P = 2 and the deadtime value is equal to DT = 2 × 5 – 1 = 9 IPbus clock cycles. A special case exists when the P = 1, then DT = PMFDTMC.

11.4 Functional Description

11.4.1 Block Diagram

A block diagram of the PMF is shown in Figure 11-1**.** The MTG bit allows the use of multiple PWM generators (A, B, and C) or just a single generator (A). PWM0 and PWM1 constitute Pair A, PWM2 and PWM3 constitute Pair B, and PWM4 and PWM5 constitute Pair C.

11.4.2 Prescaler

To permit lower PWM frequencies, the prescaler produces the PWM clock frequency by dividing the bus clock frequency by one, two, four, and eight. Each PWM generator has its own prescaler divisor. Each prescaler is buffered and will not be used by its PWM generator until the corresponding Load OK bit is set and a new PWM reload cycle begins.

11.4.3 PWM Generator

Each PWM generator contains a 15-bit up/down PWM counter producing output signals with software-selectables:

- Alignment — The logic state of each pair EDGE bit determines whether the PWM pair outputs are edge-aligned or center-aligned
- Period — The value written to each pair PWM counter modulo register is used to determine the PWM pair period. The period can also be varied by using the prescaler
- With edge-aligned output, the modulus is the period of the PWM output in clock cycles
- With center-aligned output, the modulus is one-half of the PWM output period in clock cycles
- Pulse width — The number written to the PWM value register determines the pulse width duty cycle of the PWM output in clock cycles
  - — With center-aligned output, the pulse width is twice the value written to the PWM value register
  - — With edge-aligned output, the pulse width is the value written to the PWM value register

Table 12-5. PWMPRCLK Field Descriptions

Field	Description
6:5 PCKB[2:0]	**Prescaler Select for Clock B** — Clock B is 1 of two clock sources which can be used for channels 2 or 3. These three bits determine the rate of clock B, as shown in Table 12-6.
2:0 PCKA[2:0]	**Prescaler Select for Clock A** — Clock A is 1 of two clock sources which can be used for channels 0, 1, 4, or 5. These three bits determine the rate of clock A, as shown in Table 12-7.

Table 12-6. Clock B Prescaler Selects

PCKB2	PCKB1	PCKB0	Value of Clock B
0	0	0	Bus Clock
0	0	1	Bus Clock / 2
0	1	0	Bus Clock / 4
0	1	1	Bus Clock / 8
1	0	0	Bus Clock / 16
1	0	1	Bus Clock / 32
1	1	0	Bus Clock / 64
1	1	1	Bus Clock / 128

Table 12-7. Clock A Prescaler Selects

PCKA2	PCKA1	PCKA0	Value of Clock A
0	0	0	Bus Clock
0	0	1	Bus Clock / 2
0	1	0	Bus Clock / 4
0	1	1	Bus Clock / 8
1	0	0	Bus Clock / 16
1	0	1	Bus Clock / 32
1	1	0	Bus Clock / 64
1	1	1	Bus Clock / 128

12.3.2.5 PWM Center Align Enable Register (PWMCAE)

The PWMCAE register contains six control bits for the selection of center aligned outputs or left aligned outputs for each PWM channel. If the CAEx bit is set to a 1, the corresponding PWM output will be center aligned. If the CAEx bit is cleared, the corresponding PWM output will be left aligned. Reference Section 12.4.2.5, “Left Aligned Outputs,” and Section 12.4.2.6, “Center Aligned Outputs,” for a more detailed description of the PWM output modes.

NOTE

Reads of this register return the most recent value written. Reads do not necessarily return the value of the currently active duty due to the double buffering scheme.

Reference Section 12.4.2.3, “PWM Period and Duty,” for more information.

NOTE

Depending on the polarity bit, the duty registers will contain the count of either the high time or the low time. If the polarity bit is 1, the output starts high and then goes low when the duty count is reached, so the duty registers contain a count of the high time. If the polarity bit is 0, the output starts low and then goes high when the duty count is reached, so the duty registers contain a count of the low time.

To calculate the output duty cycle (high time as a % of period) for a particular channel:

- Polarity = 0 (PPOLx = 0)
  Duty cycle = [(PWMPERx PWMDTYx)/PWMPERx] * 100%
- Polarity = 1 (PPOLx = 1)
  Duty cycle = [PWMDTYx / PWMPERx] * 100%
- For boundary case programming values, please refer to Section 12.4.2.8, “PWM Boundary Cases.”

Module Base + 0x0018

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	1	1	1	1	1	1	1	1

Figure 12-27. PWM Channel Duty Registers (PWMDTY0)

Module Base + 0x0019

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	1	1	1	1	1	1	1	1

Figure 12-28. PWM Channel Duty Registers (PWMDTY1)

Module Base + 0x001A

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	1	1	1	1	1	1	1	1

Figure 12-29. PWM Channel Duty Registers (PWMDTY2)

13.3.3.9 Timer Control Register 3 (TCTL3)

Module Base + 0x000A

	7	6	5	4	3	2	1	0
R W	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
Reset	0	0	0	0	0	0	0	0

Figure 13-11. Timer Control Register 3 (TCTL3)

Read or write anytime.

Table 13-10. TCTL3 Field Descriptions

Field	Description
7, 5, 3, 1 EDG[7:4]B 6, 4, 2, 0 EDG[7:4]A	**Input Capture Edge Control** — These four pairs of control bits configure the input capture edge detector circuits. See Table 13-11.

Table 13-11. Edge Detector Circuit Configuration

EDGnB	EDGnA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge (rising or falling)

13.3.3.10 Timer Interrupt Enable Register (TIE)

Module Base + 0x000C

	7	6	5	4	3	2	1	0
R	C7I	C6I	C5I	C4I	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 13-12. Timer Interrupt Enable Register (TIE)

Read or write anytime.

Table 13-12. TIE Field Descriptions

Field	Description
7–4 C[7:4]I	**Input Capture/Output Compare Interrupt Enable.** 0 Disables corresponding Interrupt flag (CnF of TFLG1 register) from causing a hardware interrupt 1 Enables corresponding Interrupt flag (CnF of TFLG1 register) to cause a hardware interrupt

14.1.3 Block Diagram

Figure 14-1 shows the function principle of VREG3V3V2 by means of a block diagram. The regulator core REG consists of two parallel sub-blocks, REG1 and REG2, providing two independent output voltages.

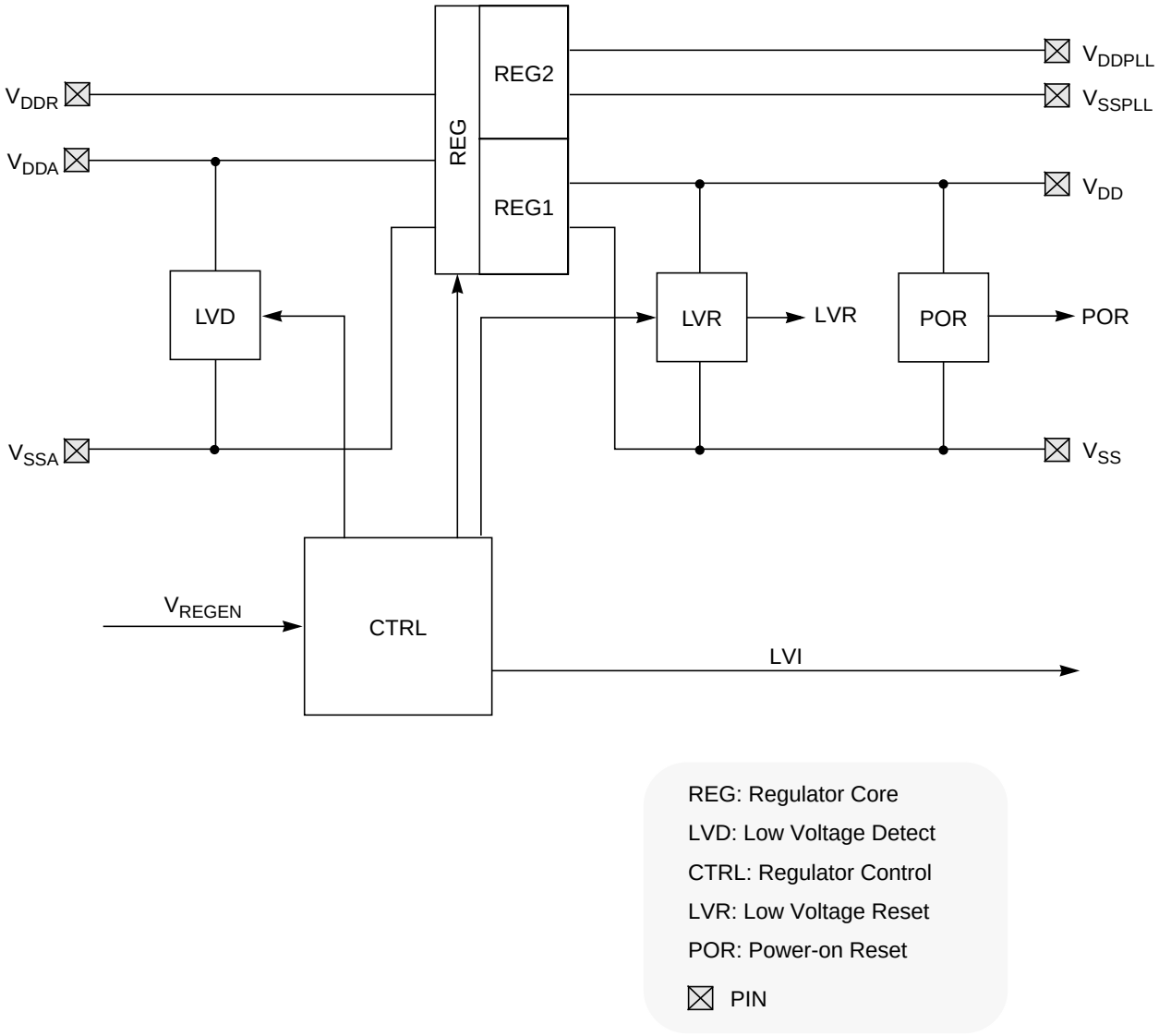

Figure 14-1. VREG3V3 Block Diagram

14.5 Resets

This subsection describes how VREG3V3V2 controls the reset of the MCU.The reset values of registers and signals are provided in Section 14.3, “Memory Map and Register Definition”. Possible reset sources are listed in Table 14-4.

Table 14-4. VREG3V3V2 — Reset Sources

Reset Source	Local Enable
Power-on reset	Always active
Low-voltage reset	Available only in full-performance mode

14.5.1 Power-On Reset

During chip power-up the digital core may not work if its supply voltage V_{DD} is below the POR deassertion level (V_{PORD}). Therefore, signal POR which forces the other blocks of the device into reset is kept high until V_{DD} exceeds V_{PORD}. Then POR becomes low and the reset generator of the device continues the start-up sequence. The power-on reset is active in all operation modes of VREG3V3V2.

14.5.2 Low-Voltage Reset

For details on low-voltage reset see Section 14.4.6, “LVR — Low-Voltage Reset”.

14.6 Interrupts

This subsection describes all interrupts originated by VREG3V3V2.

The interrupt vectors requested by VREG3V3V2 are listed in Table 14-5. Vector addresses and interrupt priorities are defined at MCU level.

Table 14-5. VREG3V3V2 — Interrupt Vectors

Interrupt Source	Local Enable
Low Voltage Interrupt (LVI)	LVIE = 1; Available only in full-performance mode

14.6.1 LVI — Low-Voltage Interrupt

In FPM VREG3V3V2 monitors the input voltage V_{DDA}. Whenever V_{DDA} drops below level V_{LVIA} the status bit LVDS is set to 1. Vice versa, LVDS is reset to 0 when V_{DDA} rises above level V_{LVID}. An interrupt, indicated by flag LVIF = 1, is triggered by any change of the status bit LVDS if interrupt enable bit LVIE = 1.

NOTE

On entering the reduced-power mode, the LVIF is not cleared by the VREG3V3V2.

Table 16-12. DBGCC Field Descriptions

Field	Description
15:0	**Comparator C Compare Bits** — The comparator C compare bits control whether comparator C will compare the address bus bits [15:0] to a logic 1 or logic 0. See Table 16-13. 0 Compare corresponding address bit to a logic 0 1 Compare corresponding address bit to a logic 1 **Note:** This register will be cleared automatically when the DBG module is armed in LOOP1 mode.

Table 16-13. Comparator C Compares

PAGSEL	EXTCMP Compare	High-Byte Compare
x0	No compare	DBGCCH[7:0] = AB[15:8]
x1	EXTCMP[5:0] = XAB[21:16]	DBGCCH[7:0] = XAB[15:14],AB[13:8]

16.3.2.7 Debug Control Register 2 (DBGC2)

Module Base + 0x0028
Starting address location affected by INITRG register setting.

	7	6	5	4	3	2	1	0
R W	BKABEN[1]	FULL	BDM	TAGAB	BKCEN[2]	TAGC[2]	RWCEN[2]	RWC[2]
Reset	0	0	0	0	0	0	0	0

1 When BKABEN is set (BKP mode), all bits in DBGC2 are available. When BKABEN is cleared and DBG is used in DBG mode, bits FULL and TAGAB have no meaning.

2 These bits can be used in BKP mode and DBG mode (when capture mode is not set in LOOP1) to provide a third breakpoint.

Figure 16-13. Debug Control Register 2 (DBGC2)

Table 16-14. DBGC2 Field Descriptions

Field	Description
7 BKABEN	**Breakpoint Using Comparator A and B Enable** — This bit enables the breakpoint capability using comparator A and B, when set (BKP mode) the DBGEN bit in DBGC1 cannot be set. 0 Breakpoint module off 1 Breakpoint module on
6 FULL	**Full Breakpoint Mode Enable** — This bit controls whether the breakpoint module is in dual mode or full mode. In full mode, comparator A is used to match address and comparator B is used to match data. See Section 16.4.1.2, “Full Breakpoint Mode,” for more details. 0 Dual address mode enabled 1 Full breakpoint mode enabled
5 BDM	**Background Debug Mode Enable** — This bit determines if the breakpoint causes the system to enter background debug mode (BDM) or initiate a software interrupt (SWI). 0 Go to software interrupt on a break request 1 Go to BDM on a break request

16.3.2.9 Debug Comparator A Extended Register (DBGCAX)

Module Base + 0x002A
Starting address location affected by INITRG register setting.

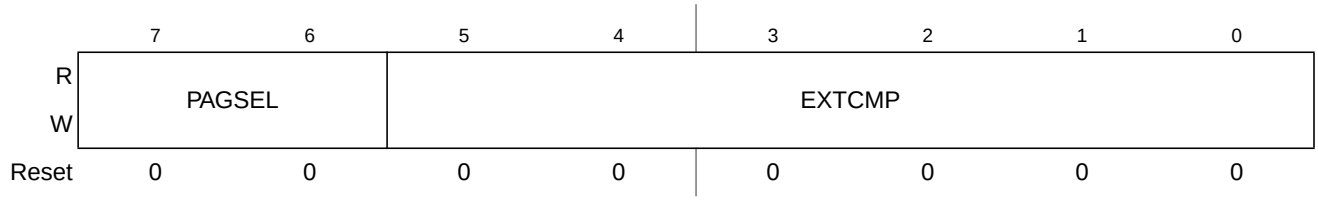

Figure 16-15. Debug Comparator A Extended Register (DBGCAX)

Table 16-19. DBGCAX Field Descriptions

Field	Description
7:6 PAGSEL	**Page Selector Field** — If DBGEN is set in DBGC1, then PAGSEL selects the type of paging as shown in Table 16-20. DPAGE and EPAGE are not yet implemented so the value in bit 7 will be ignored (i.e., PAGSEL values of 10 and 11 will be interpreted as values of 00 and 01, respectively). In BKP mode, PAGSEL has no meaning and EXTCMP[5:0] are compared to address bits [19:14] if the address is in the FLASH/ROM memory space.
5:0 EXTCMP	**Comparator A Extended Compare Bits** — The EXTCMP bits are used as comparison address bits as shown in Table 16-20 along with the appropriate PPAGE, DPAGE, or EPAGE signal from the core.

Table 16-20. Comparator A or B Compares

Mode		EXTCMP Compare	High-Byte Compare
BKP[1]	Not FLASH/ROM access	No compare	DBGCxH[7:0] = AB[15:8]
	FLASH/ROM access	EXTCMP[5:0] = XAB[19:14]	DBGCxH[5:0] = AB[13:8]
DBG[2]	PAGSEL = 00	No compare	DBGCxH[7:0] = AB[15:8]
	PAGSEL = 01	EXTCMP[5:0] = XAB[21:16]	DBGCxH[7:0] = XAB[15:14], AB[13:8]

1 See Figure 16-16.

2 See Figure 16-10 (note that while this figure provides extended comparisons for comparator C, the figure also pertains to comparators A and B in DBG mode only).

vector spaces, expansion windows, and on-chip memory are mapped so that their address ranges do not overlap. The MMC will make only one select signal active at any given time. This activation is based upon the priority outlined in Table 19-15. If two or more blocks share the same address space, only the select signal for the block with the highest priority will become active. An example of this is if the registers and the RAM are mapped to the same space, the registers will have priority over the RAM and the portion of RAM mapped in this shared space will not be accessible. The expansion windows have the lowest priority. This means that registers, vectors, and on-chip memory are always visible to a program regardless of the values in the page select registers.

Table 19-15. Select Signal Priority

Priority	Address Space
Highest	BDM (internal to core) firmware or register space
...	Internal register space
...	RAM memory block
...	EEPROM memory block
...	On-chip FLASH or ROM
Lowest	Remaining external space

In expanded modes, all address space not used by internal resources is by default external memory space. The data registers and data direction registers for ports A and B are removed from the on-chip memory map and become external accesses. If the EME bit in the MODE register (see MEBI block description chapter) is set, the data and data direction registers for port E are also removed from the on-chip memory map and become external accesses.

In special peripheral mode, the first 16 registers associated with bus expansion are removed from the on-chip memory map (PORTA, PORTB, DDRA, DDRB, PORTE, DDRE, PEAR, MODE, PUCR, RDRIV, and the EBI reserved registers).

In emulation modes, if the EMK bit in the MODE register (see MEBI block description chapter) is set, the data and data direction registers for port K are removed from the on-chip memory map and become external accesses.

19.4.2.2 Emulation Chip Select Signal

When the EMK bit in the MODE register (see MEBI block description chapter) is set, port K bit 7 is used as an active-low emulation chip select signal, $\overline{\text{ECS}}$. This signal is active when the system is in emulation mode, the EMK bit is set and the FLASH or ROM space is being addressed subject to the conditions outlined in Section 19.4.3.2, “Extended Address (XAB19:14) and ECS Signal Functionality.” When the EMK bit is clear, this pin is used for general purpose I/O.

19.4.2.3 External Chip Select Signal

When the EMK bit in the MODE register (see MEBI block description chapter) is set, port K bit 6 is used as an active-low external chip select signal, $\overline{\text{XCS}}$. This signal is active only when the $\overline{\text{ECS}}$ signal described above is not active and when the system is addressing the external address space. Accesses to

A.6 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

The ATD is specified and tested for both the 3.3V and 5V range. For ranges between 3.3V and 5V the ATD accuracy is generally the same as in the 3.3V range but is not tested in this range in production test.

A.6.1 ATD Operating Characteristics — 5V Range

The Table A-19 shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:
VSSA ≤ VRL ≤ VIN ≤ VRH ≤ VDDA. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-19. 5V ATD Operating Characteristics

Conditions are shown in Table A-4 unless otherwise noted. Supply Voltage 5V-10% <= VDDA <=5V+10%							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reference Potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA/2}$	 — —	 $V_{DDA/2}$ V_{DDA}	 V V
2	C	Differential Reference Voltage[1]	V_{RH}–V_{RL}	4.75	5.0	5.25	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5	—	2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK} Conv, Time at 4.0MHz[3] ATD Clock f_{ATDCLK}	 N_{CONV10} T_{CONV10} T_{CONV10}	 14 7 3.5	 — — —	 28 14 7	 Cycles µs µs
5	D	ATD 8-Bit Conversion Period Clock Cycles[1] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV8} T_{CONV8}	 12 6	 — —	 26 13	 Cycles µs
6	D	Stop Recovery Time (V_{DDA} = 5.0 Volts)	t_{SR}	—	—	20	µs
7	P	Reference Supply current	I_{REF}	—	—	0.375	mA

1 Full accuracy is not guaranteed when differential voltage is less than 4.75V

2 The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

3 Reduced accuracy see Table A-22 and Table A-23.

A.6.2 ATD Operating Characteristics — 3.3V Range

The Table A-20 shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:
VSSA ≤ VRL ≤ VIN ≤ VRH ≤ VDDA. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

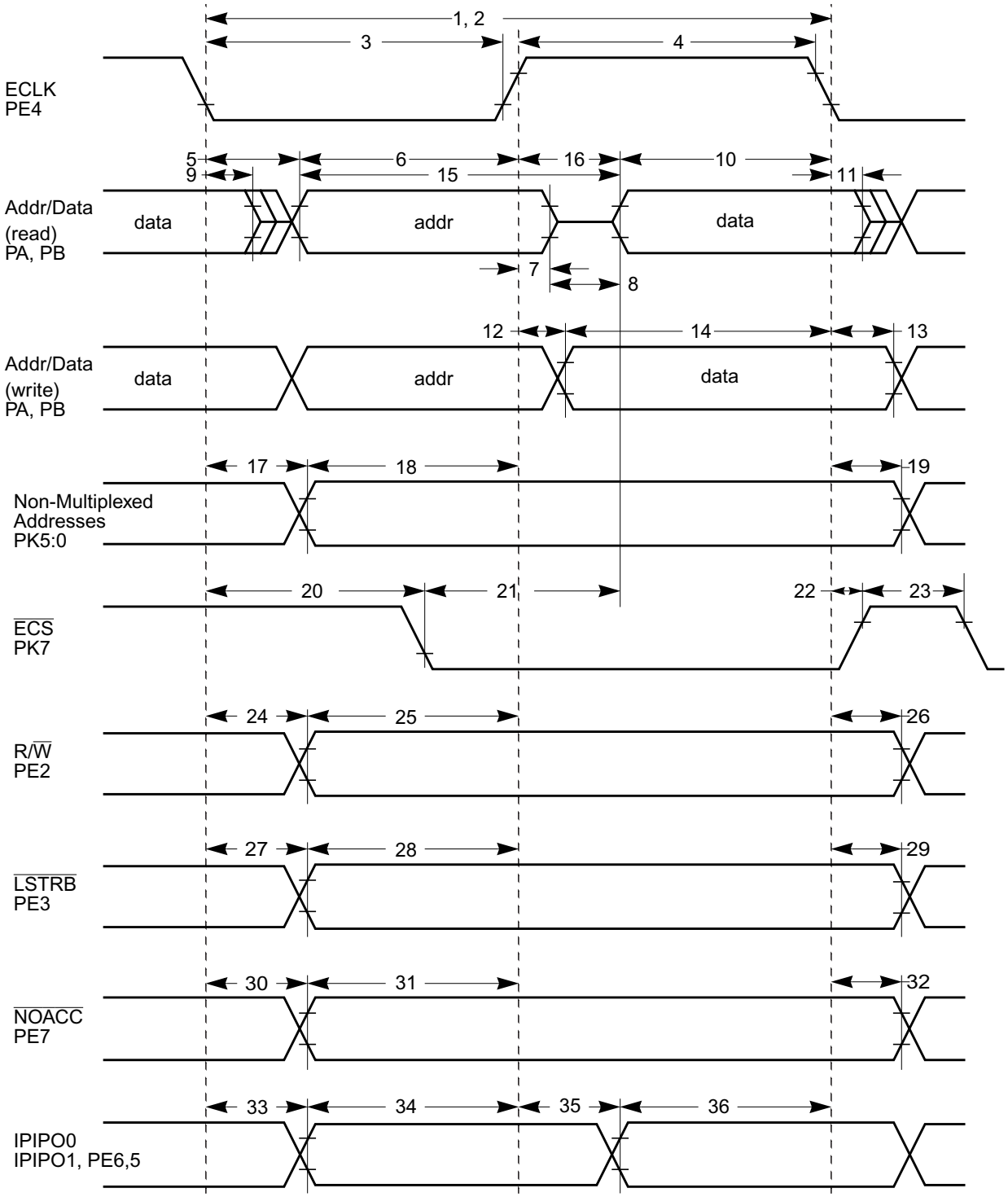

Figure A-10. General External Bus Timing