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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | HCS12 |
| Core Size | 16-Bit |
| Speed | 25MHz |
| Connectivity | EBI/EMI, I²C, SCI, SPI |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 91 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.35V ~ 2.75V |
| Data Converters | A/D 16x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 112-LQFP |
| Supplier Device Package | 112-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s12e256cpve |

## 0x0040 – 0x006F TIM0 (Timer 16 Bit 4 Channels) (Sheet 4 of 4)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x006C | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x006D | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x006E | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x006F | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |

## 0x0070 – 0x007F Reserved

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0070–0x007F | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |

## 0x0080 – 0x00AF ATD (Analog to Digital Converter 10 Bit 16 Channel) (Sheet 1 of 3)

| Address | Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0080 | ATDCTL0 | R | 0 | 0 | 0 | 0 | WRAP3[1] | WRAP2[1] | WRAP1[1] | WRAP0[1] |
| | | W | | | | | | | | |
| 0x0081 | ATDCTL1 | R | ETRIGSEL[2] | 0 | 0 | 0 | ETRIGCH3[2] | ETRIGCH2[2] | ETRIGCH1[2] | ETRIGCH0[2] |
| | | W | | | | | | | | |
| 0x0082 | ATDCTL2 | R | ADPU | AFFC | AWAI | ETRIGLE | ETRIGP | ETRIG | ASCIE | ASCIF |
| | | W | | | | | | | | |
| 0x0083 | ATDCTL3 | R | 0 | S8C | S4C | S2C | S1C | FIFO | FRZ1 | FRZ0 |
| | | W | | | | | | | | |
| 0x0084 | ATDCTL4 | R | SRES8 | SMP1 | SMP0 | PRS4 | PRS3 | PRS2 | PRS1 | PRS0 |
| | | W | | | | | | | | |
| 0x0085 | ATDCTL5 | R | DJM | DSGN | SCAN | MULT | 0 | CC | CB | CA |
| | | W | | | | | | | | |
| 0x0086 | ATDSTAT0 | R | SCF | 0 | ETORF | FIFOR | 0 | CC2 | CC1 | CC0 |
| | | W | | | | | | | | |
| 0x0087 | Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x0088 | ATDTEST0 | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | W | | | | | | | | |
| 0x0089 | ATDTEST1 | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SC |
| | | W | | | | | | | | |
| 0x008A | ATDSTAT0 | R | CCF15 | CCF14 | CCF13 | CCF12 | CCF11 | CCF10 | CCF9 | CCF8 |
| | | W | | | | | | | | |

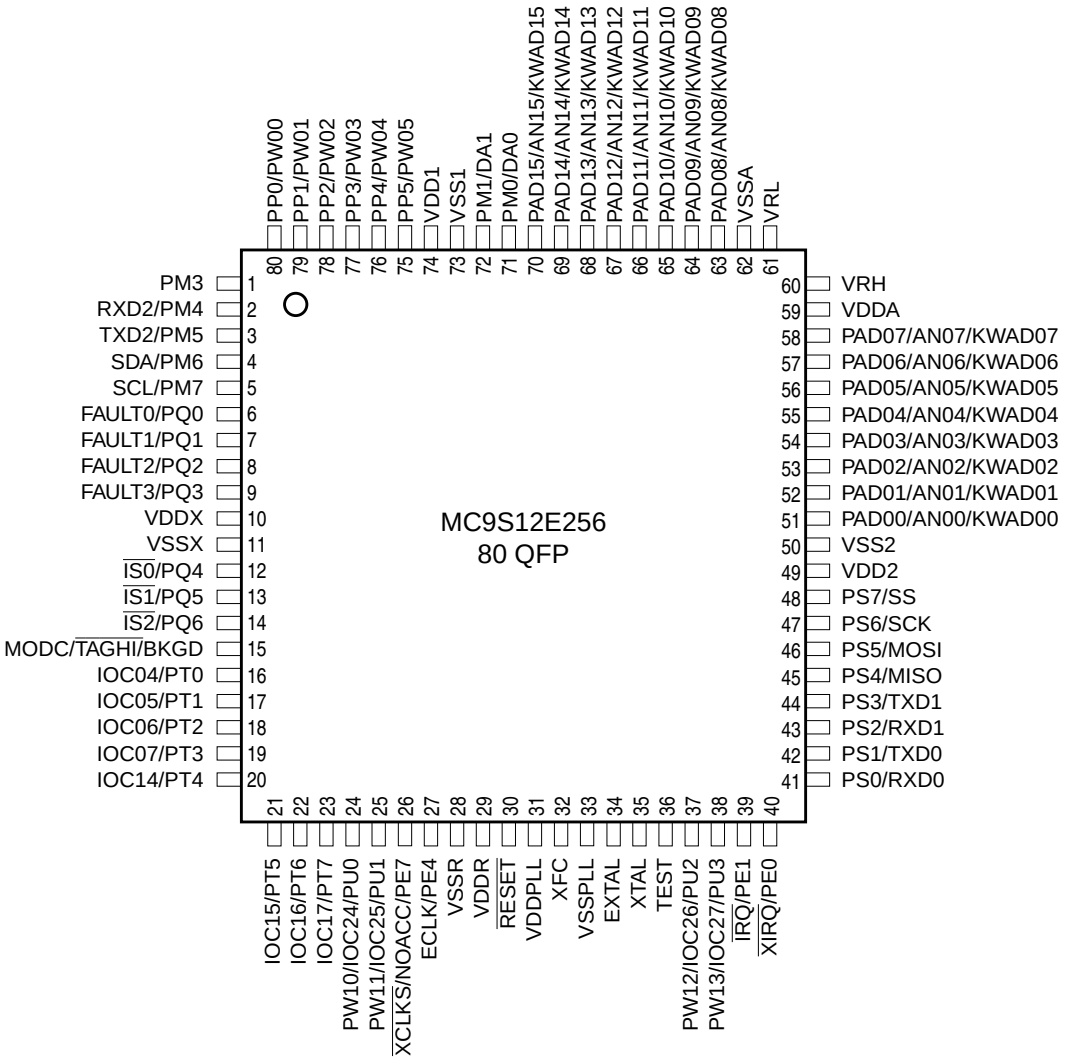


**Figure 1-4. Pin Assignments for 80-QFP**

an external program (again through BDM commands). Note that if the part goes through a reset before the security bits are reprogrammed to the unsecure state, the part will be secured again.

## 1.8 Low Power Modes

The microcontroller features three main low power modes. Consult the respective block description chapter for information on the module behavior in Stop, Pseudo Stop, and Wait Mode. An important source of information about the clock system is Chapter 4, “Clocks and Reset Generator (CRGV4) Block Description”.

### 1.8.1 Stop

Executing the CPU STOP instruction stops all clocks and the oscillator thus putting the chip in fully static mode. Wake up from this mode can be done via reset or external interrupts.

### 1.8.2 Pseudo Stop

This mode is entered by executing the CPU STOP instruction. In this mode the oscillator is still running and the Real Time Interrupt (RTI) or Watchdog (COP) sub module can stay active. Other peripherals are turned off. This mode consumes more current than the full STOP mode, but the wake up time from this mode is significantly shorter.

### 1.8.3 Wait

This mode is entered by executing the CPU WAI instruction. In this mode the CPU will not execute instructions. The internal CPU signals (address and data bus) will be fully static. All peripherals stay active. For further power consumption the peripherals can individually turn off their local clocks.

### 1.8.4 Run

Although this is not a low power mode, unused peripheral modules should not be enabled in order to save power.

## 1.9 Resets and Interrupts

Consult the Exception Processing section of the CPU12 Reference Manual for information on resets and interrupts. System resets can be generated through external control of the $\overline{\text{RESET}}$ pin, through the clock and reset generator module CRG or through the low voltage reset (LVR) generator of the voltage regulator module. Refer to Chapter 4, “Clocks and Reset Generator (CRGV4) Block Description” and Chapter 14, “Dual Output Voltage Regulator (VREG3V3V2) Block Description” for detailed information on reset generation.

### 1.9.1 Vectors

Table 1-9 lists interrupt sources and vectors in default order of priority.

### 1.9.2.2 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module block description chapters for register reset states. Refer to Chapter 18, “Multiplexed External Bus Interface (MEBIV3)” for mode dependent pin configuration of port A, B and E out of reset.

Refer to Chapter 3, “Port Integration Module (PIM9E256V1) Block Description” for reset configurations of all peripheral module ports.

Refer to Table 1-1 for locations of the memories depending on the operating mode after reset.

The RAM array is not automatically initialized out of reset.

## 1.10 Recommended Printed Circuit Board Layout

The Printed Circuit Board (PCB) must be carefully laid out to ensure proper operation of the voltage regulator as well as the MCU itself. The following rules must be observed:

- Every supply pair must be decoupled by a ceramic capacitor connected as near as possible to the corresponding pins (C1–C6).
- Central point of the ground star should be the VSSR pin.
- Use low ohmic low inductance connections between VSS1, VSS2 and VSSR.
- VSSPLL must be directly connected to VSSR.
- Keep traces of VSSPLL, EXTAL and XTAL as short as possible and occupied board area for C7, C8, C11 and Q1 as small as possible.
- Do not place other signals or supplies underneath area occupied by C7, C8, C10 and Q1 and the connection area to the MCU.
- Central power input should be fed in at the VDDA/VSSA pins.

**Table 1-11. Recommended Decoupling Capacitor Choice**

| Component | Purpose | Type | Value |
|---|---|---|---|
| C1 | VDD1 filter cap | Ceramic X7R | 100–220nF |
| C2 | VDD2 filter cap (80 QFP only) | Ceramic X7R | 100–220nF |
| C3 | VDDA filter cap | Ceramic X7R | 100nF |
| C4 | VDDR filter cap | X7R/tantalum | >=100nF |
| C5 | VDDPLL filter cap | Ceramic X7R | 100nF |
| C6 | VDDX filter cap | X7R/tantalum | >=100nF |
| C7 | OSC load cap | See PLL specification chapter | |
| C8 | OSC load cap | | |
| C9 | PLL loop filter cap | | |
| C10 | PLL loop filter cap | | |
| C11 | DC cutoff cap | | |
| R1 | PLL loop filter res | | |
| Q1 | Quartz | | |

### 3.3.1.5 Port AD Pull Device Enable Register (PERAD)

Module Base + 0x0038

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PERAD15 | PERAD14 | PERAD13 | PERAD12 | PERAD11 | PERAD10 | PERAD9 | PERAD8 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Module Base + 0x0039

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | PERAD7 | PERAD6 | PERAD5 | PERAD4 | PERAD3 | PERAD2 | PERAD1 | PERAD0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 3-6. Port AD Pull Device Enable Register (PERAD)**

Read: Anytime. Write: Anytime.

This register configures whether a pull-up or a pull-down device is activated on configured input pins. If a pin is configured as output, the corresponding Pull Device Enable Register bit has no effect.

**Table 3-5. PERAD Field Descriptions**

| Field | Description |
|---|---|
| 15:0<br>PERAD[15:0] | **Pull Device Enable Port AD**<br>0 Pull-up or pull-down device is disabled.<br>1 Pull-up or pull-down device is enabled. |

### 3.3.3 Port P

Port P is associated with the Pulse Width Modulator (PMF) modules. Each pin is assigned according to the following priority: PMF > general-purpose I/O.

When a PMF channel is enabled, the corresponding pin becomes a PWM output. Refer to the PMF block description chapter for information on enabling and disabling the PWM channels.

During reset, port P pins are configured as high-impedance inputs.

#### 3.3.3.1 Port P I/O Register (PTP)

Module Base + 0x0018

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | PTP5 | PTP4 | PTP3 | PTP2 | PTP1 | PTP0 |
| W | | | | | | | | |
| PMF: | | | PW05 | PW04 | PW03 | PW02 | PW01 | PW00 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Reserved or Unimplemented

**Figure 3-17. Port P I/O Register (PTP)**

Read: Anytime. Write: Anytime.

If the associated data direction bit (DDRPx) is set to 1 (output), a read returns the value of the I/O register bit. If the associated data direction bit (DDRPx) is set to 0 (input), a read returns the value of the pin.

The PMF function takes precedence over the general-purpose I/O function if the associated PWM channel is enabled. The PWM channels 5-0 are outputs if the respective channels are enabled.

#### 3.3.3.2 Port P Input Register (PTIP)

Module Base + 0x0019

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | PTIP5 | PTIP4 | PTIP3 | PTIP2 | PTIP1 | PTIP0 |
| W | | | | | | | | |
| Reset | 0 | 0 | u | u | u | u | u | u |

= Reserved or Unimplemented  u = Unaffected by reset

**Figure 3-18. Port P Input Register (PTIP)**

Read: Anytime. Write: Never, writes to this register have no effect.

This register always reads back the status of the associated pins.

### 3.3.6.3 Port T Data Direction Register (DDRT)

Module Base + 0x0002

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | DDRT7 | DDRT6 | DDRT5 | DDRT4 | DDRT3 | DDRT2 | DDRT1 | DDRT0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 3-38. Port T Data Direction Register (DDRT)**

Read: Anytime. Write: Anytime.

This register configures port pins PT[7:0] as either input or output.

If the TIM0(1) module is enabled, each port pin configured for output compare is forced to be an output and the associated Data Direction Register bit has no effect. If the associated timer output compare is disabled, the corresponding DDRTx bit reverts to control the I/O direction of the associated pin.

If the TIM0(1) module is enabled, each port pin configured as an input capture has the corresponding DDRTx bit controlling the I/O direction of the associated pin.

**Table 3-27. DDRT Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>DDRT[7:0] | **Data Direction Port T**<br>0 Associated pin is configured as input.<br>1 Associated pin is configured as output. |

### 3.3.6.4 Port T Reduced Drive Register (RDRT)

Module Base + 0x0003

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | RDRT7 | RDRT6 | RDRT5 | RDRT4 | RDRT3 | RDRT2 | RDRT1 | RDRT0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 3-39. Port T Reduced Drive Register (RDRT)**

Read: Anytime. Write: Anytime.

This register configures the drive strength of configured output pins as either full or reduced. If a pin is configured as input, the corresponding Reduced Drive Register bit has no effect.

**Table 3-28. RDRT Field Descriptions**

| Field | Description |
|---|---|
| 7:0<br>RDRT[7:0] | **Reduced Drive Port T**<br>0 Full drive strength at output.<br>1 Associated pin drives at about 1/3 of the full drive strength. |

### 4.3.2.10 Reserved Register (FORBYP)

**NOTE**

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special modes can alter the CRG's functionality.

Module Base + 0x0009

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 4-13. Reserved Register (FORBYP)**

Read: always read 0x0000 except in special modes

Write: only in special modes

### 4.3.2.11 Reserved Register (CTCTL)

**NOTE**

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special test modes can alter the CRG's functionality.

Module Base + 0x000A

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 4-14. Reserved Register (CTCTL)**

Read: always read 0x0080 except in special modes

Write: only in special modes

# 11.3 Memory Map and Registers

## 11.3.1 Module Memory Map

A summary of the registers associated with the PMF module is shown in Figure 11-3. Detailed descriptions of the registers and bits are given in the subsections that follow.

| Address | Name | | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $0000 | PMFCFG0 | R<br>W | WP | MTG | EDGEC | EDGEB | EDGEA | INDEPC | INDEPB | INDEPA |
| $0001 | PMFCFG1 | R<br>W | ENHA | 0 | BOTNEGC | TOPNEGC | BOTNEGB | TOPNEGB | BOTNEGA | TOPNEGA |
| $0002 | PMFCFG2 | R<br>W | 0 | 0 | MSK5 | MSK4 | MSK3 | MSK2 | MSK1 | MSK0 |
| $0003 | PMFCFG3 | R<br>W | PMFWAI | PMFFRZ | 0 | VLMODE | | SWAPC | SWAPB | SWAPA |
| $0004 | PMFFCTL | R<br>W | FMODE3 | FIE3 | FMODE2 | FIE2 | FMODE1 | FIE1 | FMODE0 | FIE0 |
| $0005 | PMFFPIN | R<br>W | 0 | FPINE3 | 0 | FPINE2 | 0 | FPINE1 | 0 | FPINE0 |
| $0006 | PMFFSTA | R<br>W | 0 | FFLAG3 | 0 | FFLAG2 | 0 | FFLAG1 | 0 | FFLAG0 |
| $0007 | PMFQSMP | R<br>W | QSMP3 | | QSMP2 | | QSMP1 | | QSMP0 | |
| $0008 | PMFDMPA | R<br>W | DMP13 | DMP12 | DMP11 | DMP10 | DMP03 | DMP02 | DMP01 | DMP00 |
| $0009 | PMFDMPB | R<br>W | DMP33 | DMP32 | DMP31 | DMP30 | DMP23 | DMP22 | DMP21 | DMP20 |
| $000A | PMFDMPC | R<br>W | DMP53 | DMP52 | DMP51 | DMP50 | DMP43 | DMP42 | DMP41 | DMP53 |
| $000B | Reserved | R<br>W | | | | | | | | |
| $000C | PMFOUTC | R<br>W | 0 | 0 | OUTCTL5 | OUTCTL4 | OUTCTL3 | OUTCTL2 | OUTCTL1 | OUTCTL0 |
| $000D | PMFOUTB | R<br>W | 0 | 0 | OUT5 | OUT4 | OUT3 | OUT2 | OUT1 | OUT0 |

= Unimplemented or Reserved

**Figure 11-3. Quick Reference to PMF Registers (Sheet 1 of 4)**

**Table 11-3. PMFCFG0 Field Descriptions (continued)**

| Field | Description |
|---|---|
| 6<br>MTG | **Multiple Timebase Generators** — This bit determines the number of timebase counters used. Once set, MTG can be cleared only by reset.<br>If MTG is set, PWM generators B and C and registers $0028 – $0037 are available. The three generators have their own variable frequencies and are not synchronized.<br>If MTG is cleared, PMF registers from $0028 – $0037 can not be written and read zeroes, and bits EDGEC and EDGEB are ignored. Pair A, Pair B and Pair C PWMs are synchronized to PWM generator A and use registers from $0020 – $0027.<br>0 Single timebase generator.<br>1 Multiple timebase generators. |
| 5<br>EDGEC | **Edge-Aligned or Center-Aligned PWM for Pair C** — This bit determines whether PWM4 and PWM5 channels will use edge-aligned or center-aligned waveforms. This bit has no effect if MTG bit is cleared. This bit cannot be modified after the WP bit is set.<br>0 PWM4 and PWM5 are center-aligned PWMs<br>1 PWM4 and PWM5 are edge-aligned PWMs |
| 4<br>EDGEB | **Edge-Aligned or Center-Aligned PWM for Pair B** — This bit determines whether PWM2 and PWM3 channels will use edge-aligned or center-aligned waveforms. This bit has no effect if MTG bit is cleared. This bit cannot be modified after the WP bit is set.<br>0 PWM2 and PWM3 are center-aligned PWMs<br>1 PWM2 and PWM3 are edge-aligned PWMs |
| 3<br>EDGEA | **Edge-Aligned or Center-Aligned PWM for Pair A**— This bit determines whether PWM0 and PWM1 channels will use edge-aligned or center-aligned waveforms. It determines waveforms for Pair B and Pair C if the MTG bit is cleared. This bit cannot be modified after the WP bit is set.<br>0 PWM0 and PWM1 are center-aligned PWMs<br>1 PWM0 and PWM1 are edge-aligned PWMs |
| 2<br>INDEPC | **Independent or Complimentary Operation for Pair C**— This bit determines if the PWM channels 4 and 5 will be independent PWMs or complementary PWMs. This bit cannot be modified after the WP bit is set.<br>0 PWM4 and PWM5 are complementary PWM pair<br>1 PWM4 and PWM5 are independent PWMs |
| 1<br>INDEPB | **Independent or Complimentary Operation for Pair B**— This bit determines if the PWM channels 2 and 3 will be independent PWMs or complementary PWMs. This bit cannot be modified after the WP bit is set.<br>0 PWM2 and PWM3 are complementary PWM pair<br>1 PWM2 and PWM3 are independent PWMs |
| 0<br>INDEPA | **Independent or Complimentary Operation for Pair A**— This bit determines if the PWM channels 0 and 1 will be independent PWMs or complementary PWMs. This bit cannot be modified after the WP bit is set.<br>0 PWM0 and PWM1 are complementary PWM pair<br>1 PWM0 and PWM1 are independent PWMs |

## 11.3.2.2 PMF Configure 1 Register (PMFCFG1)

Address: $0001

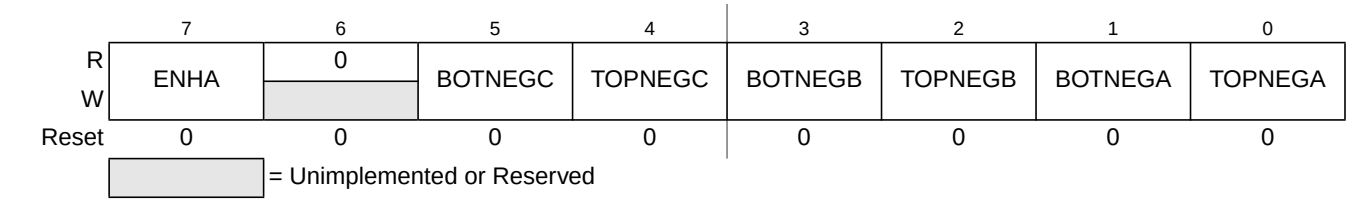


**Figure 11-5. PMF Configure 1 Register (PMFCFG1)**

### 11.3.2.24 PMF Deadtime A Register (PMFDTMA)

Address: $0026

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | PMFDTMA | | | | | | | | | | | |
| W | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

= Unimplemented or Reserved

**Figure 11-30. PMF Deadtime A Register (PMFDTMA)**

Read anytime. This register cannot be modified after the WP bit is set.

The 12-bit value written to this register is the number of PWM clock cycles in complementary channel operation. A reset sets the PWM deadtime register to a default value of 0x0FFF, selecting a deadtime of 4096-PWM clock cycles minus one bus clock cycle.

**NOTE**

Deadtime is affected by changes to the prescaler value. The deadtime duration is determined as follows: DT = P × PMFDTMA – 1, where DT is deadtime, P is the prescaler value, PMFDTMA is the programmed value of dead time. For example: if the prescaler is programmed for a divide-by-two and the PMFDTMA is set to five, then P = 2 and the deadtime value is equal to DT = 2 × 5 – 1 = 9 IPbus clock cycles. A special case exists when the P = 1, then DT = PMFDTMA.

### 11.3.2.25 PMF Enable Control B Register (PMFENCB)

Address: $0028

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | PWMENB | 0 | 0 | 0 | 0 | 0 | LDOKB | PWMRIEB |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 11-31. PMF Enable Control B Register (PMFENCB)**

Read anytime and write only if MTG is set.

**Table 11-29. PMFENCB Field Descriptions**

| Field | Description |
|---|---|
| 7<br>PWMENB | **PWM Generator B Enable** — If MTG is clear, this bit reads zero and cannot be written.<br>If MTG is set, this bit when set enables the PWM generator B and the PWM2 and PWM3 pins. When PWMENB is clear, PWM generator B is disabled, and the PWM2 and PWM3 pins are in their inactive states unless the OUTCTL2 and OUTCTL3 bits are set.<br>0 PWM generator B and PWM2–3 pins disabled unless the respective OUTCTL bit is set.<br>1 PWM generator B and PWM2–3 pins enabled. |

### 11.3.2.28 PMF Counter Modulo B Register (PMFMODB)

Address: $002C

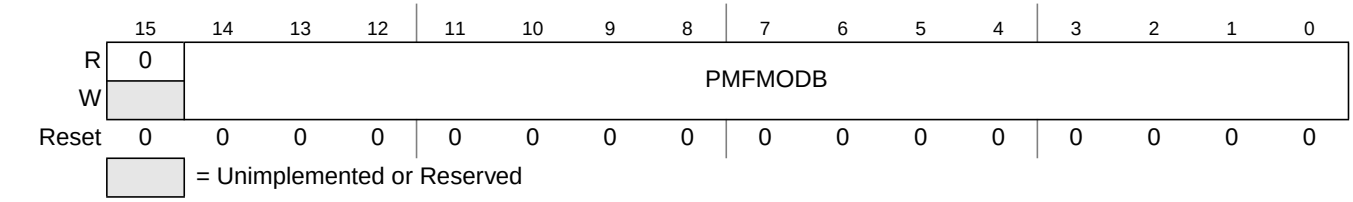


**Figure 11-34. PMF Counter Modulo B Register (PMFMODB)**

Read anytime and write only if MTG is set.

The 15-bit unsigned value written to this register is the PWM period in PWM clock periods. Do not write a modulus value of zero.

**NOTE**

The PWM counter modulo register is buffered. The value written does not take effect until the LDOKB bit is set and the next PWM load cycle begins. Reading PMFMODB reads the value in the buffer. It is not necessarily the value the PWM generator B is currently using.

### 11.3.2.29 PMF Deadtime B Register (PMFDTMB)

Address: $002E

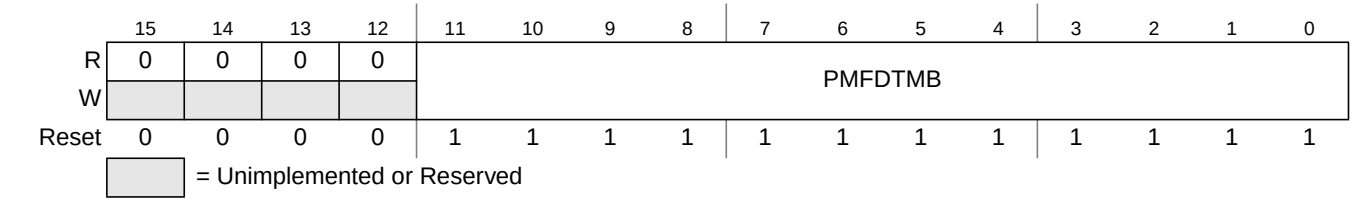


**Figure 11-35. PMF Deadtime B Register (PMFDTMB)**

Read anytime and write only if MTG is set. This register cannot be modified after the WP bit is set.

The 12-bit value written to this register is the number of PWM clock cycles in complementary channel operation. A reset sets the PWM deadtime register to a default value of 0x0FFF, selecting a deadtime of 4096-PWM clock cycles minus one bus clock cycle.

**NOTE**

Deadtime is affected by changes to the prescaler value. The deadtime duration is determined as follows: DT = P × PMFDTMB – 1, where DT is deadtime, P is the prescaler value, PMFDTMB is the programmed value of dead time. For example: if the prescaler is programmed for a divide-by-two and the PMFDTMB is set to five, then P = 2 and the deadtime value is equal to DT = 2 × 5 – 1 = 9 IPbus clock cycles. A special case exists when the P = 1, then DT = PMFDTMB.

The 12-bit value written to this register is the number of PWM clock cycles in complementary channel operation. A reset sets the PWM deadtime register to a default value of 0x0FFF, selecting a deadtime of 4096-PWM clock cycles minus one bus clock cycle.

**NOTE**

Deadtime is affected by changes to the prescaler value. The deadtime duration is determined as follows: DT = P × PMFDTMC – 1, where DT is deadtime, P is the prescaler value, PMFDTMC is the programmed value of dead time. For example: if the prescaler is programmed for a divide-by-two and the PMFDTMC is set to five, then P = 2 and the deadtime value is equal to DT = 2 × 5 – 1 = 9 IPbus clock cycles. A special case exists when the P = 1, then DT = PMFDTMC.

## 11.4 Functional Description

### 11.4.1 Block Diagram

A block diagram of the PMF is shown in Figure 11-1**.** The MTG bit allows the use of multiple PWM generators (A, B, and C) or just a single generator (A). PWM0 and PWM1 constitute Pair A, PWM2 and PWM3 constitute Pair B, and PWM4 and PWM5 constitute Pair C.

### 11.4.2 Prescaler

To permit lower PWM frequencies, the prescaler produces the PWM clock frequency by dividing the bus clock frequency by one, two, four, and eight. Each PWM generator has its own prescaler divisor. Each prescaler is buffered and will not be used by its PWM generator until the corresponding Load OK bit is set and a new PWM reload cycle begins.

### 11.4.3 PWM Generator

Each PWM generator contains a 15-bit up/down PWM counter producing output signals with software-selectables:

- Alignment — The logic state of each pair EDGE bit determines whether the PWM pair outputs are edge-aligned or center-aligned
- Period — The value written to each pair PWM counter modulo register is used to determine the PWM pair period. The period can also be varied by using the prescaler
- With edge-aligned output, the modulus is the period of the PWM output in clock cycles
- With center-aligned output, the modulus is one-half of the PWM output period in clock cycles
- Pulse width — The number written to the PWM value register determines the pulse width duty cycle of the PWM output in clock cycles
  - — With center-aligned output, the pulse width is twice the value written to the PWM value register
  - — With edge-aligned output, the pulse width is the value written to the PWM value register

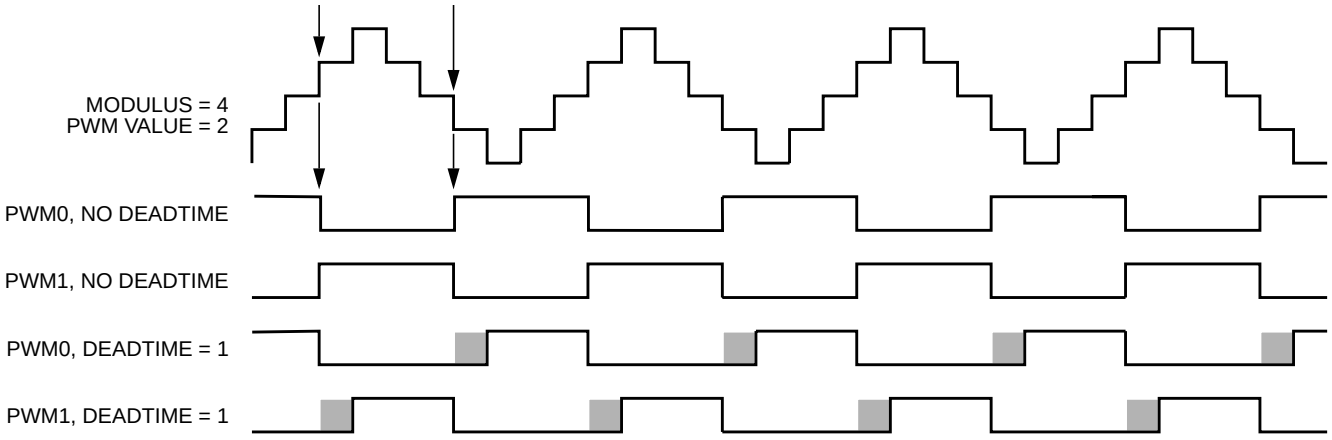


**Figure 11-50. Deadtime Insertion, Center Alignment**

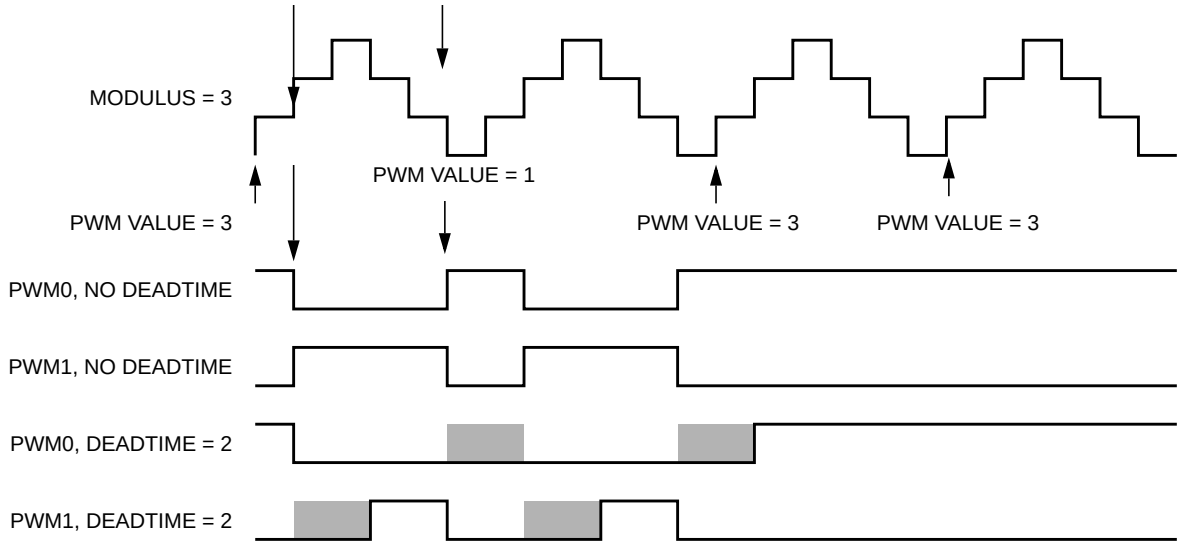


**Figure 11-51. Deadtime at Duty Cycle Boundaries**

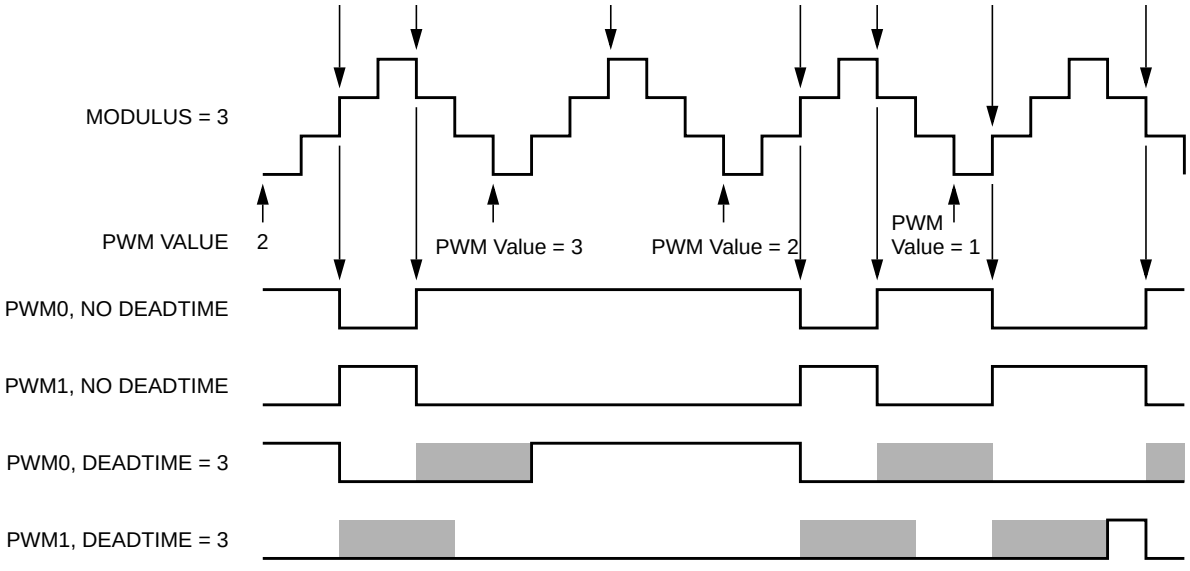


**Figure 11-52. Deadtime and Small Pulse Widths**

Shown below is the output waveform generated.

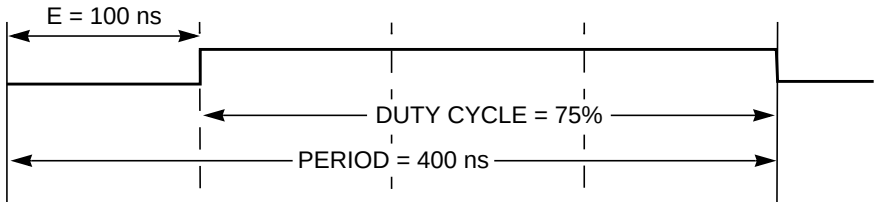


**Figure 12-37. PWM Left Aligned Output Example Waveform**

### 12.4.2.6 Center Aligned Outputs

For center aligned output mode selection, set the CAEx bit (CAEx = 1) in the PWMCAE register and the corresponding PWM output will be center aligned.

The 8-bit counter operates as an up/down counter in this mode and is set to up whenever the counter is equal to 0x0000. The counter compares to two registers, a duty register and a period register as shown in the block diagram in Figure 12-35. When the PWM counter matches the duty register the output flip-flop changes state causing the PWM waveform to also change state. A match between the PWM counter and the period register changes the counter direction from an up-count to a down-count. When the PWM counter decrements and matches the duty register again, the output flip-flop changes state causing the PWM output to also change state. When the PWM counter decrements and reaches 0, the counter direction changes from a down-count back to an up-count and a load from the double buffer period and duty registers to the associated registers is performed as described in Section 12.4.2.3, “PWM Period and Duty.” The counter counts from 0 up to the value in the period register and then back down to 0. Thus the effective period is PWMPERx*2.

**NOTE**

Changing the PWM output mode from left aligned output to center aligned output (or vice versa) while channels are operating can cause irregularities in the PWM output. It is recommended to program the output mode before enabling the PWM channel.

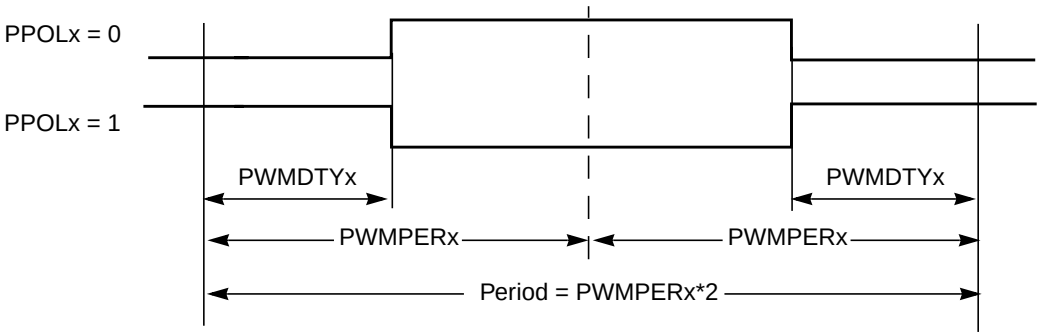


**Figure 12-38. PWM Center Aligned Output Waveform**

### 15.4.9 SYNC — Request Timed Reference Pulse

The SYNC command is unlike other BDM commands because the host does not necessarily know the correct communication speed to use for BDM communications until after it has analyzed the response to the SYNC command. To issue a SYNC command, the host should perform the following steps:

1. Drive the BKGD pin low for at least 128 cycles at the lowest possible BDM serial communication frequency (the lowest serial communication frequency is determined by the crystal oscillator or the clock chosen by CLKSW.)
2. Drive BKGD high for a brief speedup pulse to get a fast rise time (this speedup pulse is typically one cycle of the host clock.)
3. Remove all drive to the BKGD pin so it reverts to high impedance.
4. Listen to the BKGD pin for the sync response pulse.

Upon detecting the SYNC request from the host, the target performs the following steps:

1. Discards any incomplete command received or bit retrieved.
2. Waits for BKGD to return to a logic 1.
3. Delays 16 cycles to allow the host to stop driving the high speedup pulse.
4. Drives BKGD low for 128 cycles at the current BDM serial communication frequency.
5. Drives a one-cycle high speedup pulse to force a fast rise time on BKGD.
6. Removes all drive to the BKGD pin so it reverts to high impedance.

The host measures the low time of this 128 cycle SYNC response pulse and determines the correct speed for subsequent BDM communications. Typically, the host can determine the correct communication speed within a few percent of the actual target speed and the communication protocol can easily tolerate speed errors of several percent.

As soon as the SYNC request is detected by the target, any partially received command or bit retrieved is discarded. This is referred to as a soft-reset, equivalent to a time-out in the serial communication. After the SYNC response, the target will consider the next falling edge (issued by the host) as the start of a new BDM command or the start of new SYNC request.

Another use of the SYNC command pulse is to abort a pending ACK pulse. The behavior is exactly the same as in a regular SYNC command. Note that one of the possible causes for a command to not be acknowledged by the target is a host-target synchronization problem. In this case, the command may not have been understood by the target and so an ACK response pulse will not be issued.

### 15.4.10 Instruction Tracing

When a TRACE1 command is issued to the BDM in active BDM, the CPU exits the standard BDM firmware and executes a single instruction in the user code. As soon as this has occurred, the CPU is forced to return to the standard BDM firmware and the BDM is active and ready to receive a new command. If the TRACE1 command is issued again, the next user instruction will be executed. This facilitates stepping or tracing through the user code one instruction at a time.

## 17.2 External Signal Description

Most interfacing with the interrupt sub-block is done within the core. However, the interrupt does receive direct input from the multiplexed external bus interface (MEBI) sub-block of the core for the $\overline{\text{IRQ}}$ and $\overline{\text{XIRQ}}$ pin data.

## 17.3 Memory Map and Register Definition

Detailed descriptions of the registers and associated bits are given in the subsections that follow.

### 17.3.1 Module Memory Map

**Table 17-1. INT Memory Map**

| Address Offset | Use | Access |
|---|---|---|
| 0x0015 | Interrupt Test Control Register (ITCR) | R/W |
| 0x0016 | Interrupt Test Registers (ITEST) | R/W |
| 0x001F | Highest Priority Interrupt (Optional) (HPRIO) | R/W |

### 17.3.2 Register Descriptions

#### 17.3.2.1 Interrupt Test Control Register

Module Base + 0x0015
Starting address location affected by INITRG register setting.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | WRTINT | ADR3 | ADR2 | ADR1 | ADR0 |
| W | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

= Unimplemented or Reserved

**Figure 17-2. Interrupt Test Control Register (ITCR)**

Read: See individual bit descriptions

Write: See individual bit descriptions

## 19.3.2 Register Descriptions

| Name | | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x0010 INITRM | R | RAM15 | RAM14 | RAM13 | RAM12 | RAM11 | 0 | 0 | RAMHAL |
| | W | | | | | | | | |
| 0x0011 INITRG | R | 0 | REG14 | REG13 | REG12 | REG11 | 0 | 0 | 0 |
| | W | | | | | | | | |
| 0x0012 INITEE | R | EE15 | EE14 | EE13 | EE12 | EE11 | 0 | 0 | EEON |
| | W | | | | | | | | |
| 0x0013 MISC | R | 0 | 0 | 0 | 0 | EXSTR1 | EXSTR0 | ROMHM | ROMON |
| | W | | | | | | | | |
| 0x0014 MTSTO | R | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | W | | | | | | | | |
| 0x0017 MTST1 | R | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
| | W | | | | | | | | |
| 0x001C MEMSIZ0 | R | REG_SW0 | 0 | EEP_SW1 | EEP_SW0 | 0 | RAM_SW2 | RAM_SW1 | RAM_SW0 |
| | W | | | | | | | | |
| 0x001D MEMSIZ1 | R | ROM_SW1 | ROM_SW0 | 0 | 0 | 0 | 0 | PAG_SW1 | PAG_SW0 |
| | W | | | | | | | | |
| 0x0030 PPAGE | R | 0 | 0 | PIX5 | PIX4 | PIX3 | PIX2 | PIX1 | PIX0 |
| | W | | | | | | | | |
| 0x0031 Reserved | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | W | | | | | | | | |

= Unimplemented

**Figure 19-2. MMC Register Summary**

The loop bandwidth $f_C$ should be chosen to fulfill the Gardner's stability criteria by at least a factor of 10, typical values are 50. $\zeta = 0.9$ ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{ref}}{\pi \cdot \left(\zeta + \sqrt{1 + \zeta^2}\right)} \cdot \frac{1}{10} \rightarrow f_C < \frac{f_{ref}}{4 \cdot 10}; (\zeta = 0.9)$$

$f_C < 25kHz$

And finally the frequency relationship is defined as

$$n = \frac{f_{VCO}}{f_{ref}} = 2 \cdot (synr + 1) \quad = 50$$

With the above values the resistance can be calculated. The example is shown for a loop bandwidth $f_C$=10kHz:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_C}{K_\Phi} \quad = 2*\pi*50*10kHz/(316.7Hz/\Omega)=9.9k\Omega=\sim 10k\Omega$$

The capacitance $C_s$ can now be calculated as:

$$C_s = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} \approx \frac{0.516}{f_C \cdot R}; (\zeta = 0.9) \quad = 5.19nF =\sim 4.7nF$$

The capacitance $C_p$ should be chosen in the range of:

$$C_s/20 \leq C_p \leq C_s/10 \quad C_p = 470pF$$

### A.3.3.2 Jitter Information

The basic functionality of the PLL is shown in Figure A-2. With each transition of the clock $f_{cmp}$, the deviation from the reference clock $f_{ref}$ is measured and input voltage to the VCO is adjusted accordingly.The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in Figure A-3.

**Table A-20. 3.3V ATD Operating Characteristics**

| Conditions are shown in Table A-4 unless otherwise noted; Supply Voltage 3.3V-10% <= $V_{DDA}$ <= 3.3V+10% | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Num** | **C** | **Rating** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
| 1 | D | Reference Potential<br>Low<br>High | <br>$V_{RL}$<br>$V_{RH}$ | <br>$V_{SSA}$<br>$V_{DDA}/2$ | <br>—<br>— | <br>$V_{DDA}/2$<br>$V_{DDA}$ | <br>V<br>V |
| 2 | C | Differential Reference Voltage | $V_{RH}$-$V_{RL}$ | 3.0 | 3.3 | 3.6 | V |
| 3 | D | ATD Clock Frequency | $f_{ATDCLK}$ | 0.5 | — | 2.0 | MHz |
| 4 | D | ATD 10-Bit Conversion Period<br>Clock Cycles[1]<br>Conv, Time at 2.0MHz ATD Clock $f_{ATDCLK}$<br>Conv, Time at 4.0MHz[2] ATD Clock $f_{ATDCLK}$ | <br>$N_{CONV10}$<br>$T_{CONV10}$<br>$T_{CONV10}$ | <br>14<br>7<br>3.5 | <br>—<br>—<br>— | <br>28<br>14<br>7 | <br>Cycles<br>µs<br>µs |
| 5 | D | ATD 8-Bit Conversion Period<br>Clock Cycles[1]<br>Conv, Time at 2.0MHz ATD Clock $f_{ATDCLK}$ | <br>$N_{CONV8}$<br>$T_{CONV8}$ | <br>12<br>6 | <br>—<br>— | <br>26<br>13 | <br>Cycles<br>µs |
| 6 | D | Recovery Time ($V_{DDA}$=3.3 Volts) | $t_{REC}$ | — | — | 20 | µs |
| 7 | P | Reference Supply current | $I_{REF}$ | — | — | 0.250 | mA |

1 The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

2 Reduced accuracy see Table A-22 and Table A-23.

## A.6.3 Factors Influencing Accuracy

Three factors — source resistance, source capacitance and current injection — have an influence on the accuracy of the ATD.

### A.6.3.1 Source Resistance

Due to the input pin leakage current as specified in Table A-6 and Table A-7 in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance $R_S$ specifies results in an error of less than 1/2 LSB (2.5mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance are allowed.

### A.6.3.2 Source Capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage ≤ 1LSB, then the external filter capacitor, $C_f \geq 1024 * (C_{INS} - C_{INN})$.

### A.6.3.3 Current Injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of 0x3FF (0xFF in 8-bit mode) for analog inputs greater than VRH and 0x000 for values less than VRL unless the current is higher than specified as disruptive conditions.