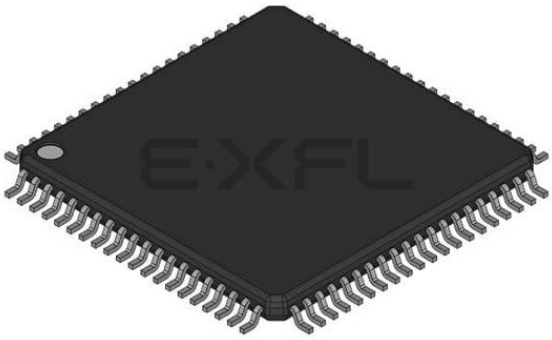

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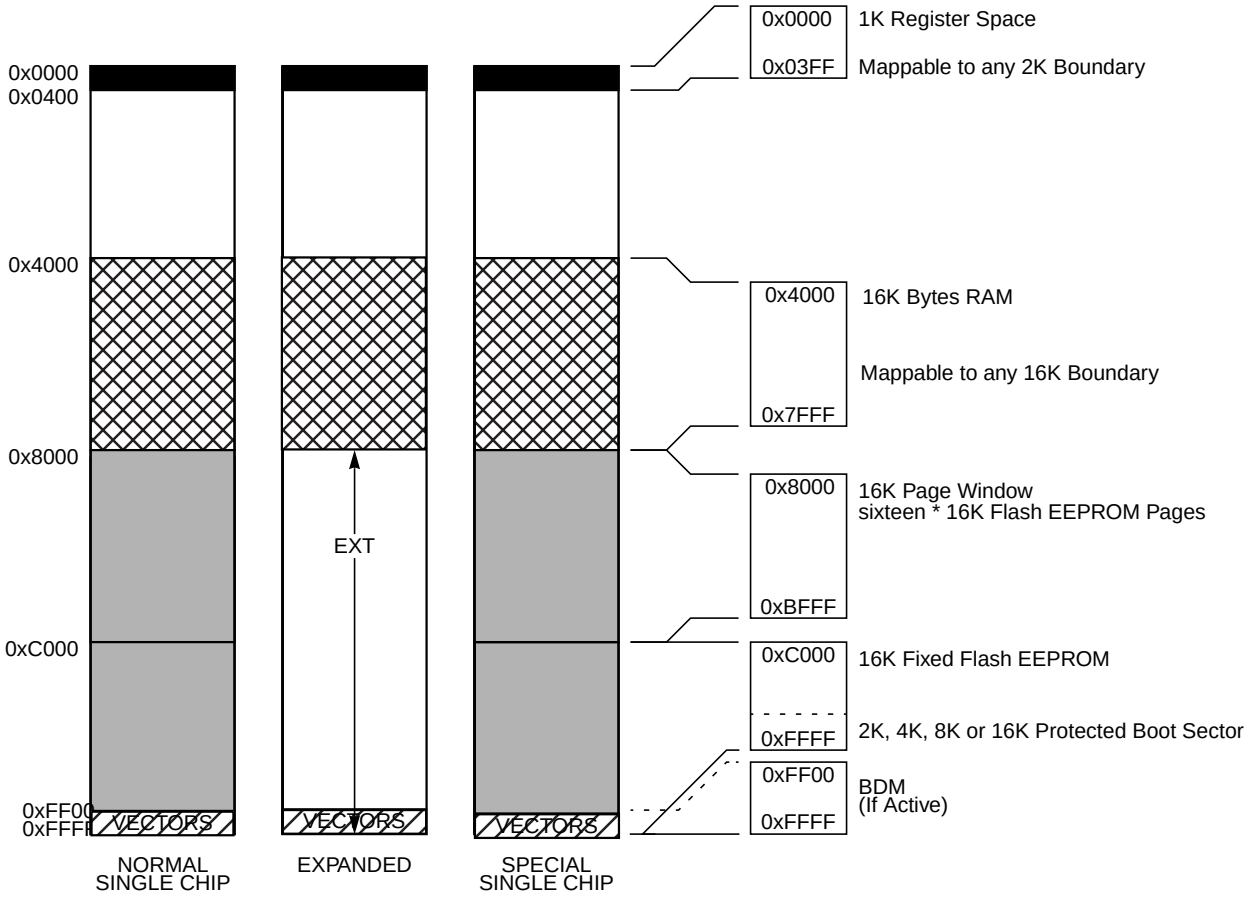
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS12
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	60
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.75V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s12e256vfue



The figure shows a useful map, which is not the map out of reset. After reset the map is:

0x0000–0x03FF: Register Space
0x0000–0x3FFF: 16K RAM (only 15K RAM visible 0x0400–0x3FFF)

Figure 1-2. MC9S12E256 User Configurable Memory Map

1.4.19 PAD[15:0] / AN[15:0] / KWAD[15:0] — Port AD I/O Pins [15:0]

PAD[15:0] are the analog inputs for the analog to digital converter (ADC). They can also be configured as general purpose digital input or output pin. When enabled as digital inputs or outputs, the PAD[15:0] can also be configured as Keypad Wake-up pins (KWU) and generate interrupts causing the MCU to exit STOP or WAIT mode. Consult Chapter 3, “Port Integration Module (PIM9E256V1) Block Description” and the Chapter 6, “Analog-to-Digital Converter (ATD10B16CV4) Block Description” for information about pin configurations.

1.4.20 PM7 / SCL — Port M I/O Pin 7

PM7 is a general purpose input or output pin. When the IIC module is enabled it becomes the serial clock line (SCL) for the IIC module (IIC). While in reset and immediately out of reset the PM7 pin is configured as a high impedance input pin. Consult Chapter 3, “Port Integration Module (PIM9E256V1) Block Description” and Chapter 10, “Inter-Integrated Circuit (IICV2) Block Description” for information about pin configurations.

1.4.21 PM6 / SDA — Port M I/O Pin 6

PM6 is a general purpose input or output pin. When the IIC module is enabled it becomes the Serial Data Line (SDL) for the IIC module (IIC). While in reset and immediately out of reset the PM6 pin is configured as a high impedance input pin. Consult Chapter 3, “Port Integration Module (PIM9E256V1) Block Description” and Chapter 10, “Inter-Integrated Circuit (IICV2) Block Description” for information about pin configurations.

1.4.22 PM5 / TXD2 — Port M I/O Pin 5

PM5 is a general purpose input or output. When the Serial Communications Interface 2 (SCI2) transmitter is enabled the PM5 pin is configured as the transmit pin TXD2 of SCI2. While in reset and immediately out of reset the PM5 pin is configured as a high impedance input pin. Consult Chapter 3, “Port Integration Module (PIM9E256V1) Block Description” and Chapter 8, “Serial Communication Interface (SCIV4) Block Description” for information about pin configurations.

1.4.23 PM4 / RXD2 — Port M I/O Pin 4

PM4 is a general purpose input or output. When the Serial Communications Interface 2 (SCI2) receiver is enabled the PM4 pin is configured as the receive pin RXD2 of SCI2. While in reset and immediately out of reset the PM4 pin is configured as a high impedance input pin. Consult Chapter 3, “Port Integration Module (PIM9E256V1) Block Description” and Chapter 8, “Serial Communication Interface (SCIV4) Block Description” for information about pin configurations.

1.4.24 PM3 — Port M I/O Pin 3

PM3 is a general purpose input or output pin. While in reset and immediately out of reset the PM3 pin is configured as a high impedance input pin. Consult Chapter 3, “Port Integration Module (PIM9E256V1) Block Description” for information about pin configurations.

1.7 Security

The device will make available a security feature preventing the unauthorized read and write of the memory contents. This feature allows:

- Protection of the contents of FLASH,
- Operation in single-chip mode,
- Operation from external memory with internal FLASH disabled.

The user must be reminded that part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program. This code would defeat the purpose of security. At the same time the user may also wish to put a back door in the user's program. An example of this is the user downloads a key through the SCI which allows access to a programming routine that updates parameters.

1.7.1 Securing the Microcontroller

Once the user has programmed the FLASH, the part can be secured by programming the security bits located in the FLASH module. These non-volatile bits will keep the part secured through resetting the part and through powering down the part.

The security byte resides in a portion of the Flash array.

Check Chapter 2, "256 Kbyte Flash Module (S12FTS256K2V1)" for more details on the security configuration.

1.7.2 Operation of the Secured Microcontroller

1.7.2.1 Normal Single Chip Mode

This will be the most common usage of the secured part. Everything will appear the same as if the part was not secured with the exception of BDM operation. The BDM operation will be blocked.

1.7.2.2 Executing from External Memory

The user may wish to execute from external space with a secured microcontroller. This is accomplished by resetting directly into expanded mode. The internal FLASH will be disabled. BDM operations will be blocked.

1.7.3 Unsecuring the Microcontroller

In order to unsecure the microcontroller, the internal FLASH must be erased. This can be done through an external program in expanded mode.

Once the user has erased the FLASH, the part can be reset into special single chip mode. This invokes a program that verifies the erasure of the internal FLASH. Once this program completes, the user can erase and program the FLASH security bits to the unsecured state. This is generally done through the BDM, but the user could also change to expanded mode (by writing the mode bits through the BDM) and jumping to

NOTE: Oscillator in Colpitts mode.

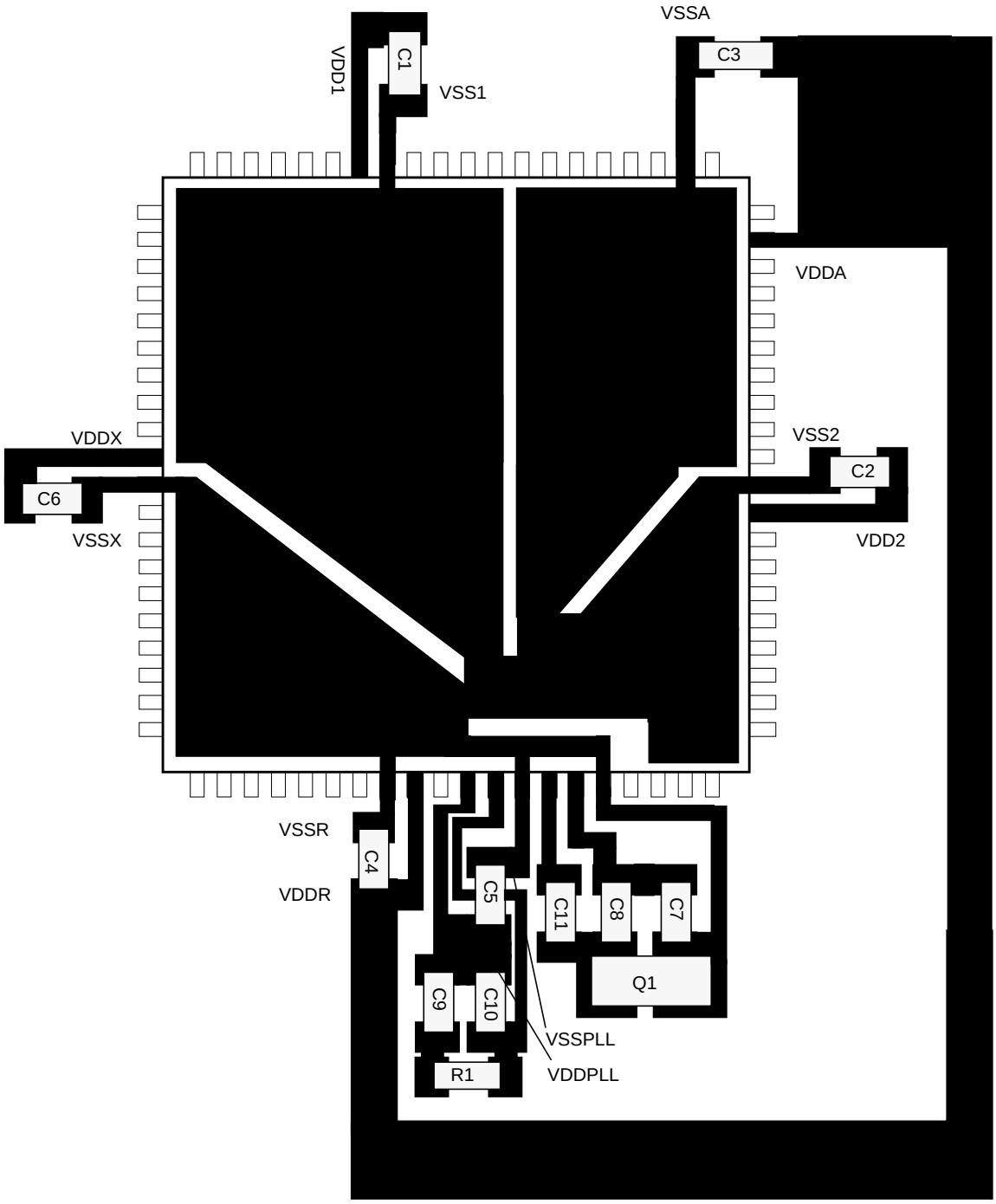


Figure 1-9. Recommended PCB Layout (80-QFP)

2.4.1.3.2 Data Compress Command

The data compress command is used to check Flash code integrity by compressing data from a selected portion of the Flash block into a signature analyzer. The starting address for the data compress operation is defined by the address written during the command write sequence. The number of consecutive word addresses compressed is defined by the data written during the command write sequence. The number of words that can be compressed in a single data compress operation ranges from 1 to 16,384. After launching the data compress command, the CCIF flag in the FSTAT register will set after the data compress operation has completed. The number of bus cycles required to execute the data compress operation is equal to two times the number of addresses read plus 20 bus cycles as measured from the time the CBEIF flag is cleared until the CCIF flag is set. After the CCIF flag is set, the signature generated by the data compress operation is available in the FDATA register. The signature in the FDATA register can be compared to the expected signature to determine the integrity of the selected data stored in the Flash block. If the last address of the Flash block is reached during the data compress operation, data compression will continue with the starting address of the Flash block.

NOTE

Since the FDATA register (or data buffer) is written to as part of the data compress operation, a command write sequence is not allowed to be buffered behind a data compress command write sequence. The CBEIF flag will not set after launching the data compress command to indicate that a command must not be buffered behind it. If an attempt is made to start a new command write sequence with a data compress operation active, the ACCERR flag in the FSTAT register will be set. A new command write sequence must only be started after reading the signature stored in the FDATA register.

In order to take corrective action, it is recommended that the data compress command be executed on a Flash sector or subset of a Flash sector. If the data compress operation on a Flash sector returns an invalid signature, the Flash sector should be erased using the sector erase command and then reprogrammed using the program command.

NOTE

During the data compress operation, the Flash array is read with a sense-amp margin setting that is different from the normal array read setting. Therefore, if the data compress operation returns an invalid signature, the section of the Flash array compressed may still be functional. The failing section of the Flash array could be validated using normal array read operations.

The data compress command can be used to verify that a sector or sequential set of sectors are erased.

3.4 Functional Description

Each pin associated with ports AD, M, P, Q, S, T and U can act as general-purpose I/O. In addition the pin can act as an output from a peripheral module or an input to a peripheral module.

A set of configuration registers is common to all ports. All registers can be written at any time, however a specific configuration might not become active.

> Example: Selecting a pull-up resistor. This resistor does not become active while the port is used as a push-pull output.

3.4.1 I/O Register

The I/O Register holds the value driven out to the pin if the port is used as a general-purpose I/O. Writing to the I/O Register only has an effect on the pin if the port is used as general-purpose output.

When reading the I/O Register, the value of each pin is returned if the corresponding Data Direction Register bit is set to 0 (pin configured as input). If the data direction register bits is set to 1, the content of the I/O Register bit is returned. This is independent of any other configuration (Figure 3-49).

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on the I/O Register when changing the data direction register.

3.4.2 Input Register

The Input Register is a read-only register and generally returns the value of the pin (Figure 3-49). It can be used to detect overload or short circuit conditions.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on the Input Register when changing the Data Direction Register.

3.4.3 Data Direction Register

The Data Direction Register defines whether the pin is used as an input or an output. A Data Direction Register bit set to 0 configures the pin as an input. A Data Direction Register bit set to 0 configures the pin as an output. If a peripheral module controls the pin the contents of the data direction register is ignored (Figure 3-49).

3.6 Interrupts

3.6.1 General

Port AD generates an edge sensitive interrupt if enabled. It offers sixteen I/O pins with edge triggered interrupt capability in wired-or fashion. The interrupt enable as well as the sensitivity to rising or falling edges can be individually configured on per pin basis. All eight bits/pins share the same interrupt vector. Interrupts can be used with the pins configured as inputs (with the corresponding ATDDIEN1 bit set to 1) or outputs.

An interrupt is generated when a bit in the port interrupt flag register and its corresponding port interrupt enable bit are both set. This external interrupt feature is capable to wake up the CPU when it is in stop or wait mode.

A digital filter on each pin prevents pulses (Figure 3-52) shorter than a specified time from generating an interrupt. The minimum time varies over process conditions, temperature and voltage (Figure 3-51 and Table 3-38).

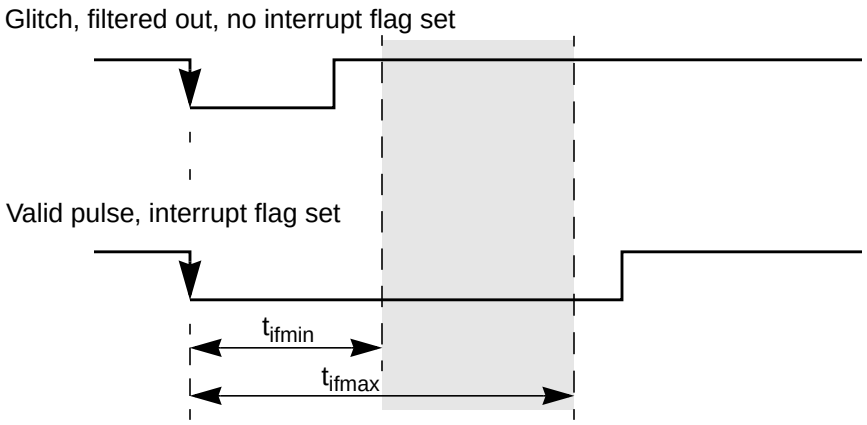


Figure 3-51. Interrupt Glitch Filter on Port AD (PPS = 0)

Table 3-38. Pulse Detection Criteria

Pulse	Mode			
	$\overline{STOP}$		STOP[1]	
		Unit		Unit
Ignored	t_{pulse} <= 3	Bus Clock	t_{pulse} <= 3.2	µs
Uncertain	3 < t_{pulse} < 4	Bus Clock	3.2 < t_{pulse} < 10	µs
Valid	t_{pulse} >= 4	Bus Clock	t_{pulse} >= 10	µs

1 These values include the spread of the oscillator frequency over temperature, voltage and process.

Chapter 7
Digital-to-Analog Converter (DAC8B1CV1) Block Description

7.1 Introduction

The DAC8B1C is a 8-bit, 1-channel digital-to-analog converter module.

7.1.1 Features

The DAC8B1C includes these features:

- 8-bit resolution.
- One output independent monotonic channel.

7.1.2 Modes of Operation

The DAC8B1C functions the same in normal, special, and emulation modes. It has two low-power modes, wait and stop modes.

7.1.2.1 Run Mode

Normal mode of operation.

7.1.2.2 Wait Mode

Entering wait mode, the DAC conversion either continues or aborts for low power, depending on the logical state of the DACWAI bit.

7.1.2.3 Stop Mode

The DAC8B1C module is disabled in stop mode for reduced power consumption. The STOP instruction does not affect DAC register states.

7.1.3 Block Diagram

Figure 7-1 illustrates the functional block diagram of the DAC8B1C module.

7.3.2.2 Reserved Register (DACC1)

This register is reserved.

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 7-4. Reserved Register (DACC1)

Read: always read $00

Write: unimplemented

7.3.2.3 DAC Data Register — Left Justified (DACD)

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset	0	0	0	0	0	0	0	0

Figure 7-5. DAC Data Register — Left Justified (DACD)

Read: read zeroes when DJM is set

Write: unimplemented when DJM is set

The DAC data register is an 8-bit readable/writable register that stores the data to be converted when DJM bit is clear. When the DACE bit is set, the value in this register is converted into an analog voltage such that values from $00 to $FF result in equal voltage increments from V_{SSA} to V_{REF}. When DJM bit is set, this register reads zeroes and cannot be written.

Table 8-8. SCISR1 Field Descriptions (continued)

Field	Description
3 OR	**Overrun Flag**[2] — OR is set when software fails to read the SCI data register before the receive shift register receives the next frame. The OR bit is set immediately after the stop bit has been completely received for the second frame. The data in the shift register is lost, but the data already in the SCI data registers is not affected. Clear OR by reading SCI status register 1 (SCISR1) with OR set and then reading SCI data register low (SCIDRL). 0 No overrun 1 Overrun
2 NF	**Noise Flag** — NF is set when the SCI detects noise on the receiver input. NF bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. Clear NF by reading SCI status register 1(SCISR1), and then reading SCI data register low (SCIDRL). 0 No noise 1 Noise
1 FE	**Framing Error Flag** — FE is set when a logic 0 is accepted as the stop bit. FE bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. FE inhibits further data reception until it is cleared. Clear FE by reading SCI status register 1 (SCISR1) with FE set and then reading the SCI data register low (SCIDRL). 0 No framing error 1 Framing error
0 PF	**Parity Error Flag** — PF is set when the parity enable bit (PE) is set and the parity of the received data does not match the parity type bit (PT). PF bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. Clear PF by reading SCI status register 1 (SCISR1), and then reading SCI data register low (SCIDRL). 0 No parity error 1 Parity error

1 When the receiver wakeup bit (RWU) is set, an idle line condition does not set the IDLE flag.

2 The OR flag may read back as set when RDRF flag is clear. This may happen if the following sequence of events occurs:

1. After the first frame is received, read status register SCISR1 (returns RDRF set and OR flag clear);
2. Receive second frame without reading the first frame in the data register (the second frame is not received and OR flag is set);
3. Read data register SCIDRL (returns first frame and clears RDRF flag in the status register);
4. Read status register SCISR1 (returns RDRF clear and OR set).

Event 3 may be at exactly the same time as event 2 or any time after. When this happens, a dummy SCIDRL read following event 4 will be required to clear the OR flag if further frames are to be received.

Table 10-5. IIC Divider and Hold Values (Sheet 5 of 5)

IBC[7:0] (hex)	SCL Divider (clocks)	SDA Hold (clocks)	SCL Hold (start)	SCL Hold (stop)
96	416	84	184	212
97	512	84	232	260
98	320	36	152	164
99	384	36	184	196
9A	448	68	216	228
9B	512	68	248	260
9C	576	100	280	292
9D	640	100	312	324
9E	768	132	376	388
9F	960	132	472	484
A0	640	68	312	324
A1	768	68	376	388
A2	896	132	440	452
A3	1024	132	504	516
A4	1152	196	568	580
A5	1280	196	632	644
A6	1536	260	760	772
A7	1920	260	952	964
A8	1280	132	632	644
A9	1536	132	760	772
AA	1792	260	888	900
AB	2048	260	1016	1028
AC	2304	388	1144	1156
AD	2560	388	1272	1284
AE	3072	516	1528	1540
AF	3840	516	1912	1924
B0	2560	260	1272	1284
B1	3072	260	1528	1540
B2	3584	516	1784	1796
B3	4096	516	2040	2052
B4	4608	772	2296	2308
B5	5120	772	2552	2564
B6	6144	1028	3064	3076
B7	7680	1028	3832	3844
B8	5120	516	2552	2564
B9	6144	516	3064	3076
BA	7168	1028	3576	3588
BB	8192	1028	4088	4100
BC	9216	1540	4600	4612
BD	10240	1540	5112	5124
BE	12288	2052	6136	6148
BF	15360	2052	7672	7684

11, the PWMs are enabled when the next PWM half cycle begins regardless of the state of the logic level detected by the filter at the fault. See Figure 11-77 and Figure 11-78.

- PWM pins disabled by the FAULT1 pin or the FAULT3 pin are enabled when
  - — Software clears the corresponding FFLAGx flag
  - — The filter detects a logic zero on the fault pin at the start of the next PWM half cycle boundary. See Figure 11-79.

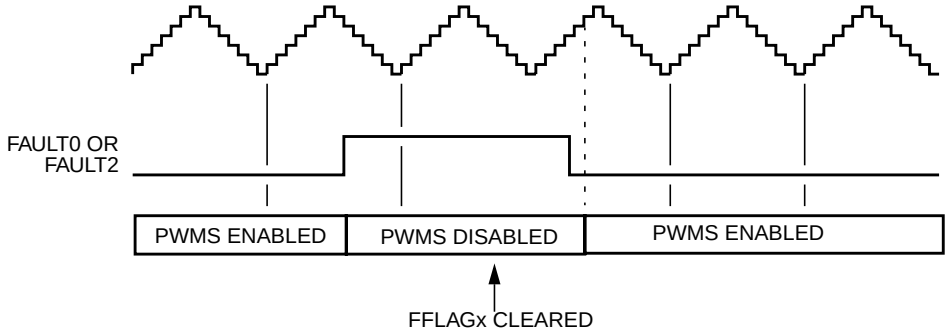


Figure 11-77. Manual Fault Clearing (Faults 0 and 2) — QSMP = 00

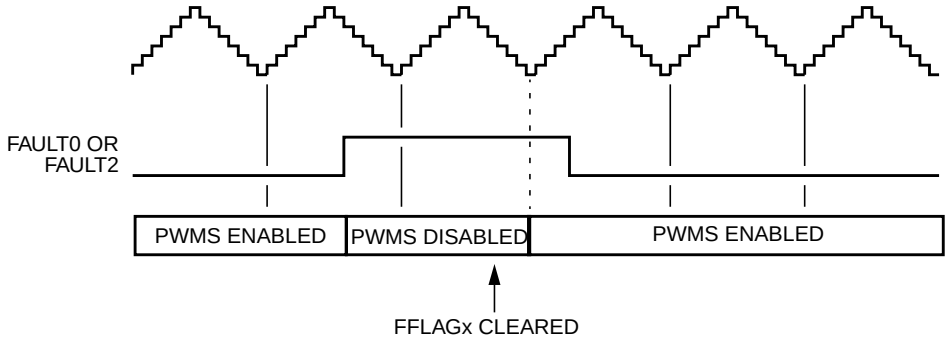


Figure 11-78. Manual Fault Clearing (Faults 0 and 2) — QSMP = 01, 10, or 11

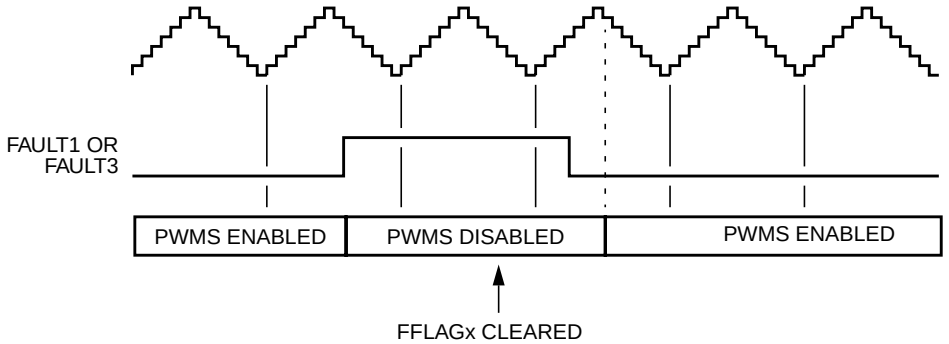


Figure 11-79. Manual Fault Clearing (Faults 1 and 3)

NOTE

PWM half-cycle boundaries occur at both the PWM cycle start and when the counter equals the modulus, so in edge-aligned operation full-cycles and half-cycles are equal.

Table 12-5. PWMPRCLK Field Descriptions

Field	Description
6:5 PCKB[2:0]	**Prescaler Select for Clock B** — Clock B is 1 of two clock sources which can be used for channels 2 or 3. These three bits determine the rate of clock B, as shown in Table 12-6.
2:0 PCKA[2:0]	**Prescaler Select for Clock A** — Clock A is 1 of two clock sources which can be used for channels 0, 1, 4, or 5. These three bits determine the rate of clock A, as shown in Table 12-7.

Table 12-6. Clock B Prescaler Selects

PCKB2	PCKB1	PCKB0	Value of Clock B
0	0	0	Bus Clock
0	0	1	Bus Clock / 2
0	1	0	Bus Clock / 4
0	1	1	Bus Clock / 8
1	0	0	Bus Clock / 16
1	0	1	Bus Clock / 32
1	1	0	Bus Clock / 64
1	1	1	Bus Clock / 128

Table 12-7. Clock A Prescaler Selects

PCKA2	PCKA1	PCKA0	Value of Clock A
0	0	0	Bus Clock
0	0	1	Bus Clock / 2
0	1	0	Bus Clock / 4
0	1	1	Bus Clock / 8
1	0	0	Bus Clock / 16
1	0	1	Bus Clock / 32
1	1	0	Bus Clock / 64
1	1	1	Bus Clock / 128

12.3.2.5 PWM Center Align Enable Register (PWMCAE)

The PWMCAE register contains six control bits for the selection of center aligned outputs or left aligned outputs for each PWM channel. If the CAEx bit is set to a 1, the corresponding PWM output will be center aligned. If the CAEx bit is cleared, the corresponding PWM output will be left aligned. Reference Section 12.4.2.5, “Left Aligned Outputs,” and Section 12.4.2.6, “Center Aligned Outputs,” for a more detailed description of the PWM output modes.

Shown below is the output waveform generated.

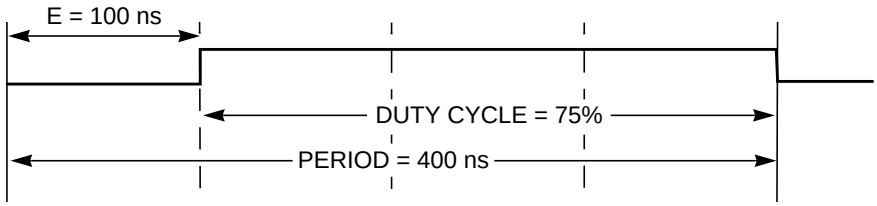


Figure 12-37. PWM Left Aligned Output Example Waveform

12.4.2.6 Center Aligned Outputs

For center aligned output mode selection, set the CAEx bit (CAEx = 1) in the PWMCAE register and the corresponding PWM output will be center aligned.

The 8-bit counter operates as an up/down counter in this mode and is set to up whenever the counter is equal to 0x0000. The counter compares to two registers, a duty register and a period register as shown in the block diagram in Figure 12-35. When the PWM counter matches the duty register the output flip-flop changes state causing the PWM waveform to also change state. A match between the PWM counter and the period register changes the counter direction from an up-count to a down-count. When the PWM counter decrements and matches the duty register again, the output flip-flop changes state causing the PWM output to also change state. When the PWM counter decrements and reaches 0, the counter direction changes from a down-count back to an up-count and a load from the double buffer period and duty registers to the associated registers is performed as described in Section 12.4.2.3, “PWM Period and Duty.” The counter counts from 0 up to the value in the period register and then back down to 0. Thus the effective period is PWMPERx*2.

NOTE

Changing the PWM output mode from left aligned output to center aligned output (or vice versa) while channels are operating can cause irregularities in the PWM output. It is recommended to program the output mode before enabling the PWM channel.

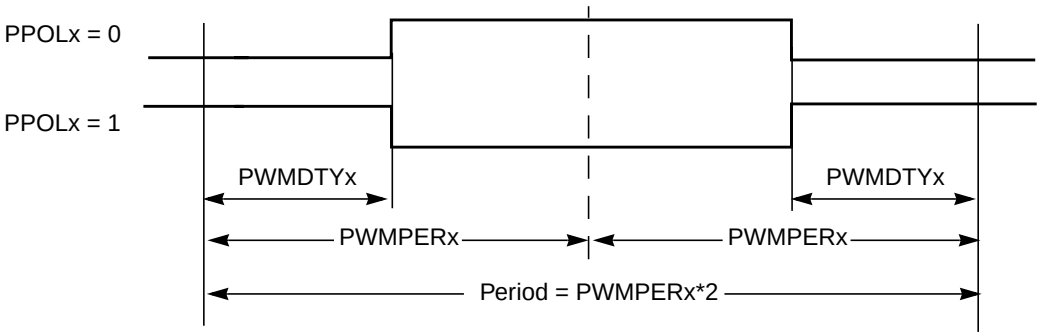


Figure 12-38. PWM Center Aligned Output Waveform

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x001A	TC5 (High)	R	tc5 15	tc5 14	tc5 13	tc5 12	tc5 11	tc5 10	tc5 9	tc5 8
		W								
0x001B	TC5 (Low)	R	tc5 7	tc5 6	tc5 5	tc5 4	tc5 3	tc5 2	tc5 1	tc5 0
		W								
0x001C	TC6 (High)	R	tc6 15	tc6 14	tc6 13	tc6 12	tc6 11	tc6 10	tc6 9	tc6 8
		W								
0x001D	TC6(Low)	R	tc6 7	tc6 6	tc6 5	tc6 4	tc6 3	tc6 2	tc6 1	tc6 0
		W								
0x001E	TC7 (High)	R	tc7 15	tc7 14	tc7 13	tc7 12	tc7 11	tc7 10	tc7 9	tc7 8
		W								
0x001F	TC7 (Low)	R	tc7 7	tc7 6	tc7 5	tc7 4	tc7 3	tc7 2	tc7 1	tc7 0
		W								
0x0020	PACTL	R	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
		W								
0x0021	PAFLG	R	0	0	0	0	0	0	PAOVF	PAIF
		W								
0x0022	PACNT (High)	R	pacnt 15	pacnt 14	pacnt 13	pacnt 12	pacnt 11	pacnt 10	pacnt 9	pacnt 8
		W								
0x0023	PACNT (Low)	R	pacnt 7	pacnt 6	pacnt 5	pacnt 4	pacnt 3	pacnt 2	pacnt 1	pacnt 0
		W								
0x0024 ↓ 0x002C	Reserved	R								
		W								
0x002D	TIMTST	R	Timer Test Register							
		W								
0x002E ↓ 0x002F	Reserved	R								
		W								

= Unimplemented or Reserved

Figure 13-2. TIM16B4CV1 Register Summary (Sheet 2 of 2)

13.3.3 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

13.3.3.1 Timer Input Capture/Output Compare Select (TIOS)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	IOS7	IOS6	IOS5	IOS4	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 13-3. Timer Input Capture/Output Compare Select (TIOS)

Read or write anytime.

Table 13-1. TIOS Field Descriptions

Field	Description
7–4 IOS[7:4]	**Input Capture or Output Compare Channel Configuration** 0 The corresponding channel acts as an input capture. 1 The corresponding channel acts as an output compare.

13.3.3.2 Timer Compare Force Register (CFORC)

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W	FOC7	FOC6	FOC5	FOC4				
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 13-4. Timer Compare Force Register (CFORC)

Read anytime but will always return $00. Write anytime.

Table 13-2. CFORC Field Descriptions

Field	Description
7–4 FOC[7:4]	**Force Output Compare Action for Channel 7-4** — A write to this register with the corresponding (FOC 7:4) data bit(s) set causes the action programmed for output compare on channel “n” to occur immediately.The action taken is the same as if a successful comparison had just taken place with the TCn register except the interrupt flag does not get set. 0 Force Output Compare Action disabled 1 Force Output Compare Action enabled **Note:** A successful channel 7 output compare overrides any channel 6:4 compares. If forced output compare on any channel occurs at the same time as the successful output compare then forced output compare action will take precedence and interrupt flag will not get set.

13.3.3.14 Timer Input Capture/Output Compare Registers (TC4–TC7)

TC4 Module Base + 0x0018–0x0019

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	tc4	tc4	tc4	tc4	tc4	tc4	tc4	tc4	tc4	tc4	tc4	tc4	tc4	tc4	tc4	tc4
W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TC5 Module Base + 0x001A–0x001B

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	tc5	tc5	tc5	tc5	tc5	tc5	tc5	tc5	tc5	tc5	tc5	tc5	tc5	tc5	tc5	tc5
W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TC6 Module Base + 0x001C–0x001D

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	tc6	tc6	tc6	tc6	tc6	tc6	tc6	tc6	tc6	tc6	tc6	tc6	tc6	tc6	tc6	tc6
W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TC7 Module Base + 0x001E–0x001F

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	tc7	tc7	tc7	tc7	tc7	tc7	tc7	tc7	tc7	tc7	tc7	tc7	tc7	tc7	tc7	tc7
W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 13-16. Timer Input Capture/Output Compare Registers (TC4–TC7)

Read anytime. Write anytime for output compare function. Writes to these registers have no effect during input capture.

Depending on the TIOS bit for the corresponding channel, these registers are used to latch the value of the free-running counter when a defined transition is sensed by the corresponding input capture edge detector or to trigger an output action for output compare.

NOTE

Read/Write access in byte mode for high byte should takes place before low byte otherwise it will give a different result.

Table 19-1. MMC Memory Map (continued)

Address Offset	Register	Access
0x0017	Reserved	—
. .	. .	—
0x001C	Memory Size Register 0 (MEMSIZ0)	R
0x001D	Memory Size Register 1 (MEMSIZ1)	R
. .	. .	
0x0030	Program Page Index Register (PPAGE)	R/W
0x0031	Reserved	—

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}{}^2$$

Which is the sum of all output currents on I/O ports associated with VDDX and VDDM.

For R_{DSON} is valid:

$$R_{DSON} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

respectively

$$R_{DSON} = \frac{V_{DD5} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

I_{DDR} is the current shown in Table A-8 and not the overall current flowing into VDDR, which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}{}^2$$

Which is the sum of all output currents on I/O ports associated with VDDX and VDDR.

Table A-5. Thermal Package Characteristics[1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Thermal Resistance LQFP112, single sided PCB[2]	θ_{JA}	—	—	54	°C/W
2	T	Thermal Resistance LQFP112, double sided PCB with 2 internal planes[3]	θ_{JA}	—	—	41	°C/W
3	T	Junction to Board LQFP112	θ_{JB}	—	—	31	°C/W
4	T	Junction to Case LQFP112	θ_{JC}	—	—	11	°C/W
5	T	Junction to Package Top LQFP112	Ψ_{JT}	—	—	2	°C/W
6	T	Thermal Resistance QFP 80, single sided PCB	θ_{JA}	—	—	51	°C/W
7	T	Thermal Resistance QFP 80, double sided PCB with 2 internal planes	θ_{JA}	—	—	41	°C/W
8	T	Junction to Board QFP80	θ_{JB}	—	—	27	°C/W
9	T	Junction to Case QFP80	θ_{JC}	—	—	14	°C/W
10	T	Junction to Package Top QFP80	Ψ_{JT}	—	—	3	°C/W

1 The values for thermal resistance are achieved by package simulations

2 PC Board according to EIA/JEDEC Standard 51-3

3 PC Board according to EIA/JEDEC Standard 51-7