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Details	
Product Status	Active
Core Processor	H8/300L
Core Size	8-Bit
Speed	10MHz
Connectivity	SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
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1.3.2 Pin Functions

Table 1.5 outlines the pin functions of the H8/38024 Group.

Table 1.5 Pin Functions

		Pin No.							
Type	**Symbol**	**FP-80A TFP-80C**	**FP-80B**	**TLP-85V**	**Pad No.*1**	**Pad No.*2**	**Pad No.*3**	**I/O**	**Name and Functions**
Power source pins	V_{CC}	52	54	E8	53	54	52	Input	**Power supply:** All V_{CC} pins should be connected to the system power supply.
	V_{SS}	8 (= AV_{SS}) 53	10 (= AV_{SS}) 55	D8 E1 (= AV_{SS})	9 54	10 55	8 53	Input	**Ground:** All V_{SS} pins should be connected to the system power supply (0 V).
	AV_{CC}	1	3	B1	1	2	1	Input	**Analog power supply:** This is the power supply pin for the A/D converter. When the A/D converter is not used, connect this pin to the system power supply.
	AV_{SS}	8 (= V_{SS})	10 (= V_{SS})	E1 (= V_{SS})	8	9	8	Input	**Analog ground:** This is the A/D converter ground pin. It should be connected to the system power supply (0V).
	V_1 V_2 V_3	51 50 49	53 52 51	F9 E9 F8	52 51 50	53 52 51	51 50 49	Input	**LCD power supply:** These are the power supply pins for the LCD controller/driver.
	CV_{CC}*4	4	—	—	—	—	—	Input	**Power supply:** This is the internal step-down power supply pin. To ensure stability, a capacitor with a rating of about 0.1 µF should be connected between this pin and the V_{SS} pin.

5.5 Subsleep Mode

5.5.1 Transition to Subsleep Mode

The system goes from subactive mode to subsleep mode when a SLEEP instruction is executed while the SSBY bit in SYSCR1 is cleared to 0, LSON bit in SYSCR1 is set to 1, and TMA3 bit in TMA is set to 1. In subsleep mode, operation of on-chip peripheral modules other than the A/D converter and PWM is in active state. As long as a minimum required voltage is applied, the contents of CPU registers, the on-chip RAM and some registers of the on-chip peripheral modules are retained. I/O ports keep the same states as before the transition.

5.5.2 Clearing Subsleep Mode

Subsleep mode is cleared by an interrupt (timer A, timer C, timer F, timer G, asynchronous event counter, SCI3, IRQAEC, IRQ_4, IRQ_3, IRQ_1, IRQ_0, WKP_7 to WKP_0) or by a low input at the $\overline{RES}$ pin.

- Clearing by interrupt

  When an interrupt is requested, subsleep mode is cleared and interrupt exception handling starts. Subsleep mode is not cleared if the I bit of CCR is set to 1 or the particular interrupt is disabled in the interrupt enable register.

  To synchronize the interrupt request signal with the system clock, up to $2/\phi_{SUB}$(s) delay may occur after the interrupt request signal occurrence, before the interrupt exception handling start.

- Clearing by $\overline{RES}$ input

  Clearing by $\overline{RES}$ pin is the same as for standby mode; see Clearing by $\overline{RES}$ pin in section 5.3.2, Clearing Standby Mode.

Section 8 I/O Ports

8.1 Overview

The LSI is provided with five 8-bit I/O ports, two 4-bit I/O ports, one 3-bit I/O port, one 8-bit input-only port, one 1-bit input-only port, and one 6-bit output-only port. Table 8.1 indicates the functions of each port.

Each port has of a port control register (PCR) that controls input and output, and a port data register (PDR) for storing output data. Input or output can be assigned to individual bits. See section 2.9.2, Notes on Bit Manipulation, for information on executing bit-manipulation instructions to write data in PCR or PDR.

Ports 5, 6, 7, 8, and A are also used as liquid crystal display segment and common pins, selectable in 4-bit units.

Block diagrams of each port are given in Appendix C, I/O Port Block Diagrams.

Table 8.1 Port Functions

Port	Description	Pins	Other Functions	Function Switching Registers
Port 1	• 4-bit I/O port • MOS input pull-up option	$P1_7$/$\overline{IRQ_3}$/TMIF	External interrupt 3, timer event input pin TMIF	PMR1 TCRF
		$P1_6$*1	None	
		$P1_4$/$\overline{IRQ_4}$/$\overline{ADTRG}$	External interrupt 4, A/D converter external trigger	PMR1 AMR
		$P1_3$/TMIG	Timer G input capture	PMR1 PMR2
Port 3	• 8-bit I/O port • MOS input pull-up option • Large-current port*2 • MOS open drain output selectable (only $P3_5$)	$P3_7$/AEVL $P3_6$/AEVH	Asynchronous counter event input pins AEVL, AEVH	PMR3 ECCR
		$P3_5$ to $P3_3$	None	PMR2
		$P3_2$, TMOFH $P3_1$, TMOFL	Timer F output compare output	PMR3
		$P3_0$/UD	Timer C count up/down selection input	PMR3

8.7 Port 7

8.7.1 Overview

Port 7 is an 8-bit I/O port, configured as shown in figure 8.6.

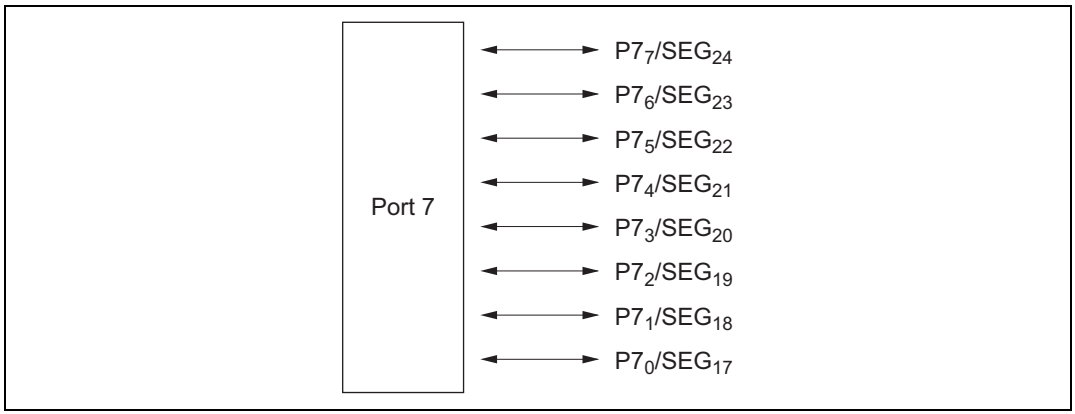


Figure 8.6 Port 7 Pin Configuration

8.7.2 Register Configuration and Description

Table 8.17 shows the port 7 register configuration.

Table 8.17 Port 7 Registers

Name	Abbr.	R/W	Initial Value	Address
Port data register 7	PDR7	R/W	H'00	H'FFDA
Port control register 7	PCR7	W	H'00	H'FFEA

8.10 Port A

8.10.1 Overview

Port A is a 4-bit I/O port, configured as shown in figure 8.9.

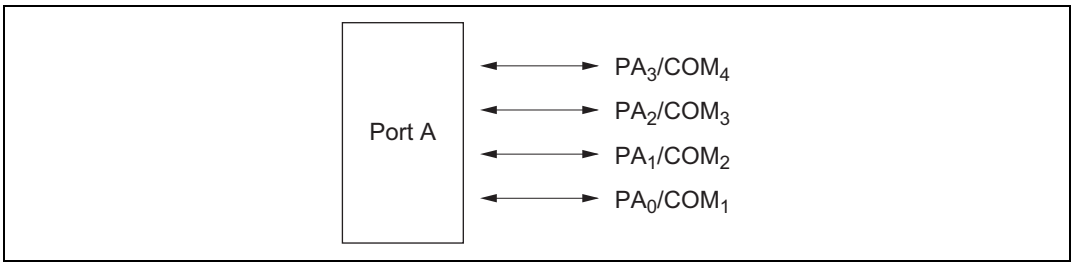


Figure 8.9 Port A Pin Configuration

8.10.2 Register Configuration and Description

Table 8.26 shows the port A register configuration.

Table 8.26 Port A Registers

Name	Abbr.	R/W	Initial Value	Address
Port data register A	PDRA	R/W	H'F0	H'FFDD
Port control register A	PCRA	W	H'F0	H'FFED

Port Data Register A (PDRA)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	PA_3	PA_2	PA_1	PA_0
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	—	R/W	R/W	R/W	R/W

PDRA is an 8-bit register that stores data for port A pins PA_3 to PA_0. If port A is read while PCRA bits are set to 1, the values stored in PDRA are read, regardless of the actual pin states. If port A is read while PCRA bits are cleared to 0, the pin states are read.

Upon reset, PDRA is initialized to H'F0.

9.2.4 Timer A Operation States

Table 9.3 summarizes the timer A operation states.

Table 9.3 Timer A Operation States

Operation Mode		Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	Module Standby
TCA	Interval	Reset	Functions	Functions	Halted	Halted	Halted	Halted	Halted
	Clock time base	Reset	Functions	Functions	Functions	Functions	Functions	Halted	Halted
TMA		Reset	Functions	Retained	Retained	Functions	Retained	Retained	Retained

Note: When the real-time clock time base function is selected as the internal clock of TCA in active mode or sleep mode, the internal clock is not synchronous with the system clock, so it is synchronized by a synchronizing circuit. This may result in a maximum error of 1/ϕ (s) in the count cycle.

9.2.5 Application Note

When bit 0 (TACKSTP) of the clock stop register 1 (CKSTPR1) is cleared to 0, bit 3 (TMA3) of the timer mode register A (TMA) cannot be rewritten.

Set bit 0 (TACKSTP) of the clock stop register 1 (CKSTPR1) to 1 before rewriting bit 3 (TMA3) of the timer mode register A (TMA).

Timer Counter C (TCC)

Bit	7	6	5	4	3	2	1	0
	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

TCC is an 8-bit read-only up/down-counter, which is incremented or decremented by internal clock or external event input. The clock source for input to this counter is selected by bits TMC2 to TMC0 in timer mode register C (TMC). TCC values can be read by the CPU at any time.

When TCC overflows from H'FF to H'00 or to the value set in TLC, or underflows from H'00 to H'FF or to the value set in TLC, the IRRTC bit in IRR2 is set to 1.

TCC is allocated to the same address as TLC.

Upon reset, TCC is initialized to H'00.

Timer Load Register C (TLC)

Bit	7	6	5	4	3	2	1	0
	TLC7	TLC6	TLC5	TLC4	TLC3	TLC2	TLC1	TLC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

TLC is an 8-bit write-only register for setting the reload value of timer counter C (TCC).

When a reload value is set in TLC, the same value is loaded into timer counter C as well, and TCC starts counting up/down from that value. When TCC overflows or underflows during operation in auto-reload mode, the TLC value is loaded into TCC. Accordingly, overflow/underflow period can be set within the range of 1 to 256 input clocks.

The same address is allocated to TLC as to TCC.

Upon reset, TLC is initialized to H'00.

9.7.4 Asynchronous Event Counter Operation Modes

Asynchronous event counter operation modes are shown in table 9.21.

Table 9.21 Asynchronous Event Counter Operation Modes

Operation Mode	Reset	Active	Sleep	Watch	Subactive	Subsleep	Standby	Module Standby
AEGSR	Reset	Functions	Functions	Retained*1	Functions	Functions	Retained*1	Retained
ECCR	Reset	Functions	Functions	Retained*1	Functions	Functions	Retained*1	Retained
ECCSR	Reset	Functions	Functions	Retained*1	Functions	Functions	Retained*1	Retained
ECH	Reset	Functions	Functions	Functions*1*2	Functions*2	Functions*2	Functions*1*2	Halted
ECL	Reset	Functions	Functions	Functions*1*2	Functions*2	Functions*2	Functions*1*2	Halted
IRQAEC	Reset	Functions	Functions	Retained*3	Functions	Functions	Retained*3	Retained*4
Event counter PWM	Reset	Functions	Functions	Retained	Retained	Retained	Retained	Retained

Notes: 1. When an asynchronous external event is input, the counter increments but the counter overflow H/L flags are not affected.
2. Operates when asynchronous external events are selected; halted and retained otherwise.
3. Clock control by IRQAEC operates, but interrupts do not.
4. As the clock is stopped in module standby mode, IRQAEC has no effect.

9.7.5 Application Notes

1. When reading the values in ECH and ECL, the correct value will not be returned if the event counter increments during the read operation. Therefore, if the counter is being used in the 8-bit mode, clear bits CUEH and CUEL in ECCSR to 0 before reading ECH or ECL. If the counter is being used in the 16-bit mode, clear CUEL only to 0 before reading ECH or ECL.
2. Use a clock with a frequency of up to 16 MHz for input to the AEVH and AEVL pins, and ensure that the high and low widths of the clock are at least half the OSC clock cycle duration. The duty cycle is immaterial.

10.2.7 Serial Status Register (SSR)

Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	OER	FER	PER	TEND	MPBR	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Note: * Only a write of 0 for flag clearing is possible.

SSR is an 8-bit register containing status flags that indicate the operational status of SCI3.

SSR can be read or written to by the CPU at any time, but 1 cannot be written to bits TDRE, RDRF, OER, PER, and FER.

Bits TEND and MPBR are read-only bits, and cannot be modified.

SSR is initialized to H'84 upon reset, and in standby, module standby, or watch mode.

Bit 7—Transmit Data Register Empty (TDRE)

Bit 7 indicates that transmit data has been transferred from TDR to TSR.

Bit 7 TDRE	Description
0	Transmit data written in TDR has not been transferred to TSR Clearing conditions: After reading TDRE = 1, cleared by writing 0 to TDRE When data is written to TDR by an instruction
1	Transmit data has not been written to TDR, or transmit data written in TDR has been transferred to TSR Setting conditions: When bit TE in SCR3 is cleared to 0 When data is transferred from TDR to TSR (initial value)

10.3.2 Operation in Asynchronous Mode

In asynchronous mode, serial communication is performed with synchronization provided character by character. A start bit indicating the start of communication and one or two stop bits indicating the end of communication are added to each character before it is sent.

SCI3 has separate transmission and reception units, allowing full-duplex communication. As the transmission and reception units are both double-buffered, data can be written during transmission and read during reception, making possible continuous transmission and reception.

Data Transfer Format

The general data transfer format in asynchronous communication is shown in figure 10.3.

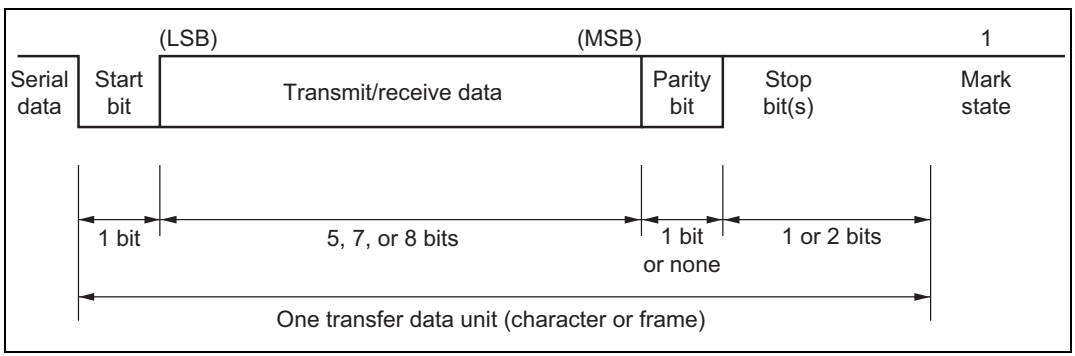


Figure 10.3 Data Format in Asynchronous Communication

In asynchronous communication, the communication line is normally in the mark state (high level). SCI3 monitors the communication line and when it detects a space (low level), identifies this as a start bit and begins serial data communication.

One transfer data character consists of a start bit (low level), followed by transmit/receive data (LSB-first format, starting from the least significant bit), a parity bit (high or low level), and finally one or two stop bits (high level).

In asynchronous mode, synchronization is performed by the falling edge of the start bit during reception. The data is sampled on the 8th pulse of a clock with a frequency 16 times the bit period, so that the transfer data is latched at the center of each bit.

Figure 10.5 shows an example of a flowchart for initializing SCI3.

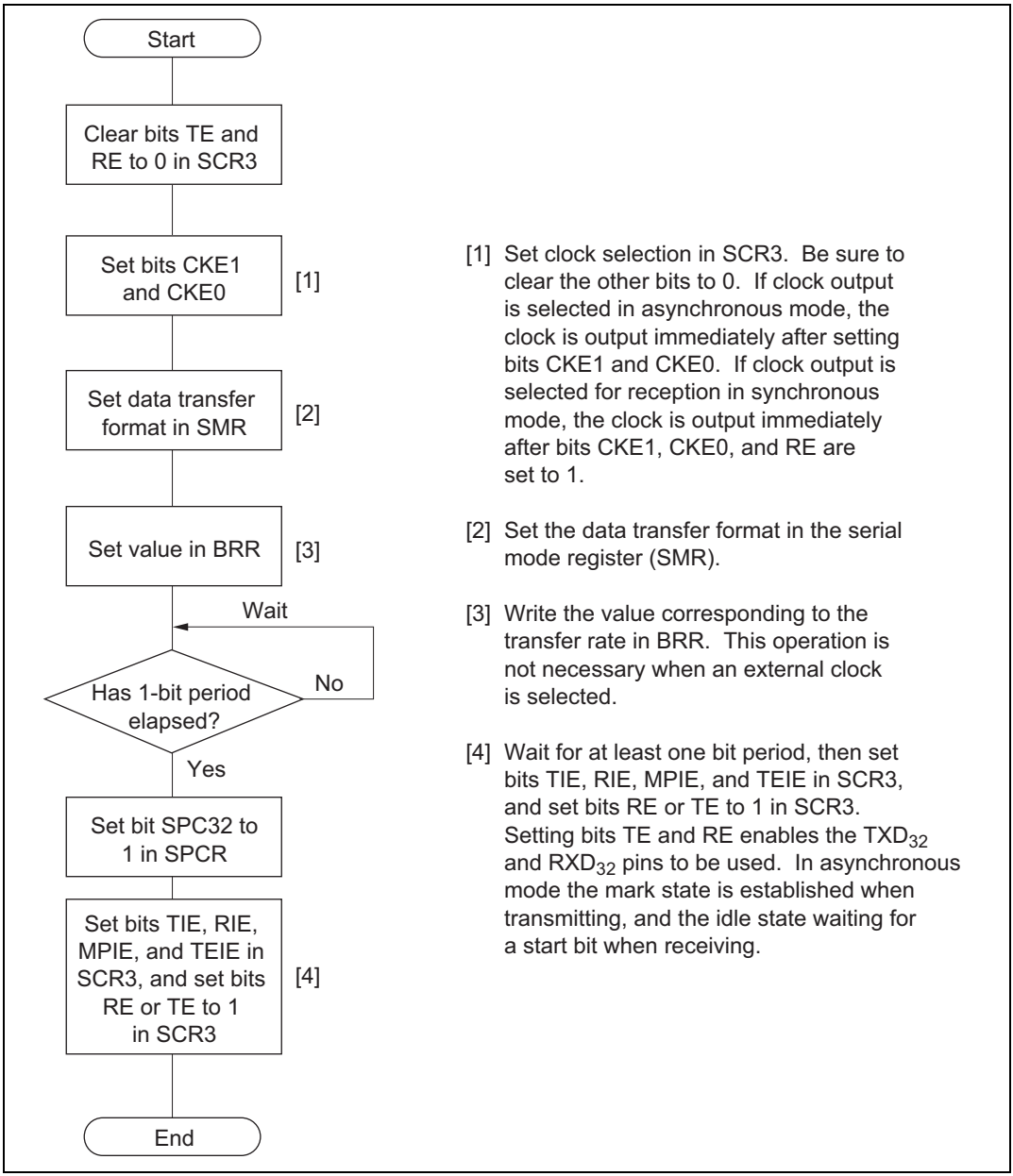


Figure 10.5 Example of SCI3 Initialization Flowchart

Notes: 1. When switching from transmission to simultaneous transmission/reception, check that SCI3 has finished transmitting and that bits TDRE and TEND are set to 1, clear bit TE to 0, and then set bits TE and RE to 1 simultaneously.

2. When switching from reception to simultaneous transmission/reception, check that SCI3 has finished receiving, clear bit RE to 0, then check that bit RDRF and the error flags (OER, FER, and PER) are cleared to 0, and finally set bits TE and RE to 1 simultaneously.

12.1.2 Block Diagram

Figure 12.1 shows a block diagram of the A/D converter.

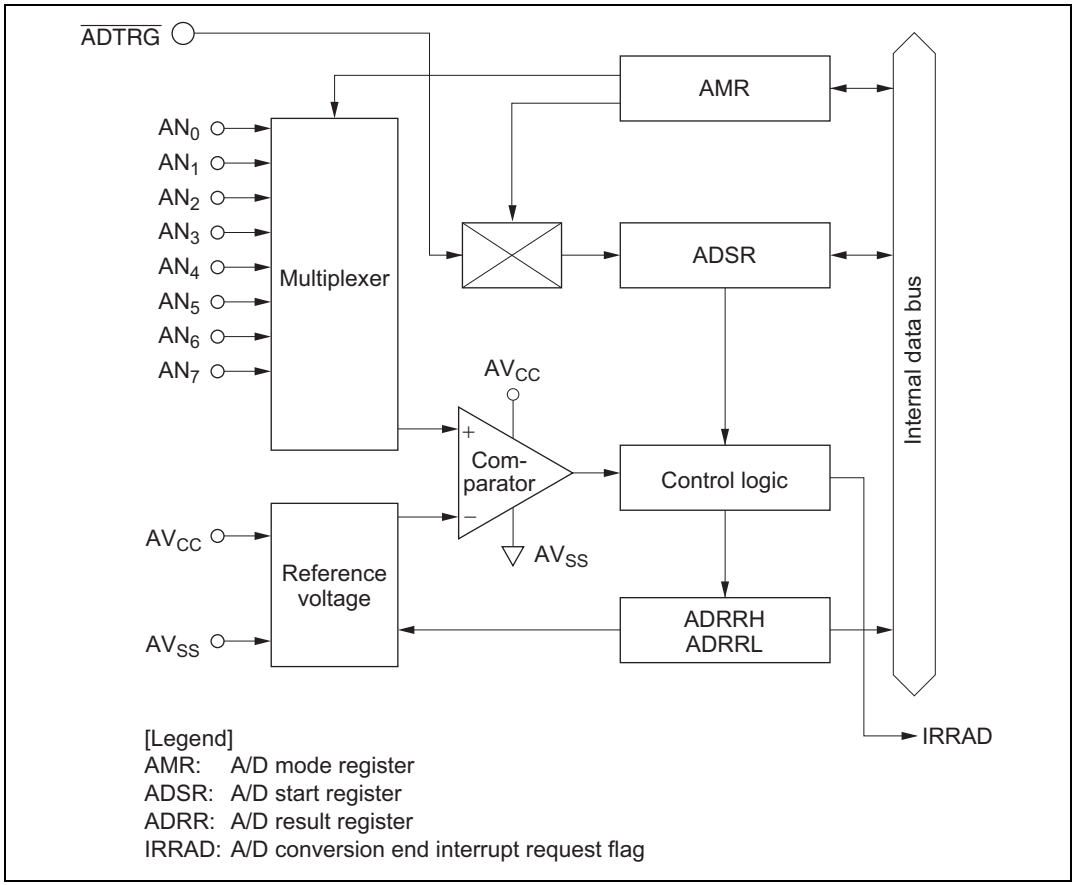


Figure 12.1 Block Diagram of the A/D Converter

When the power-supply voltage does not fall below Vreset1 (typ. = 2.3 V) voltage but rises above Vint (U) (typ. = 4.0 V) voltage, the LVDI sets the $\overline{\text{LVDINT}}$ signal to 1. If the LVDUE bit is 1 at this time, the LVDUF bit in LVDSR is set to 1 and an IRQ0 interrupt request is simultaneously generated.

If the power supply voltage (Vcc) falls below Vreset1 (typ. = 2.3 V) voltage, the LVDR function is performed.

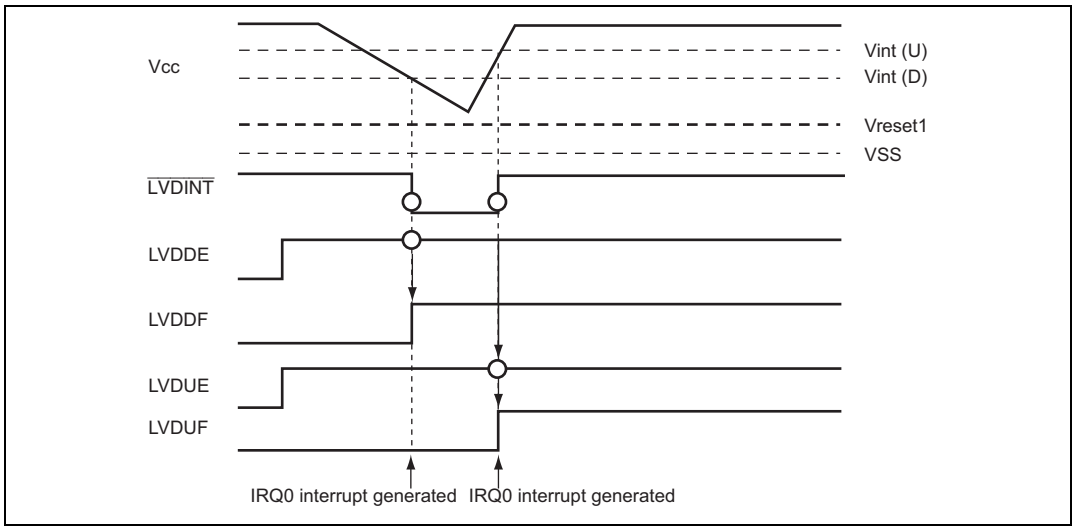
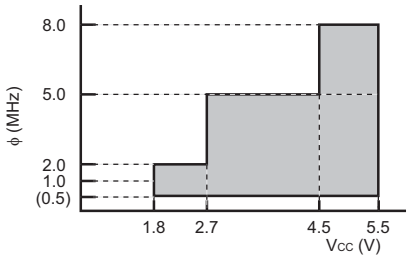


Figure 14.4 Operational Timing of LVDI Circuit

The reference voltage, power supply voltage drop detection level, and power supply voltage rise detection level can be input to the LSI from external sources via the Vref, extD, and extU pins. Figure 14.5 shows the operational timing using input from the Vref, extD, and extU pins.

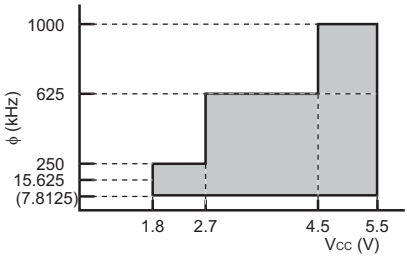
First, make sure that the voltages input to pins extD and extU are set to higher levels than the interrupt detection voltage Vexd. After initial settings are made, a power supply drop interrupt is generated if the extD input voltage drops below Vexd. After a power supply drop interrupt is generated, if the external power supply voltage rises and the extU input voltage rises higher than Vexd, a power supply rise interrupt is generated. As with the on-chip circuit, the above function should be used in conjunction with LVDR (Vreset1) when the LVDI function is used.

Power Supply Voltage and Operating Frequency Range



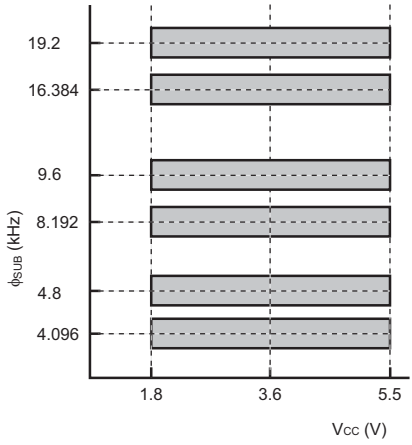
- Active (high-speed) mode
- Sleep (high-speed) mode (except CPU)

Note: 1. The figure in parentheses is the minimum operating frequency when an external clock is input. When using an oscillator, the minimum operating frequency (ϕ) is 1 MHz.



- Active (medium-speed) mode
- Sleep (medium-speed) mode (except A/D converter)

Note: 2. The figure in parentheses is the minimum operating frequency when an external clock is input. When using an oscillator, the minimum operating frequency (ϕ) is 15.625 kHz.



- Subactive mode
- Subsleep mode (except CPU)
- Watch mode (except CPU)

16.2.5 LCD Characteristics

Table 16.6 shows the LCD characteristics.

Table 16.6 LCD Characteristics

V_{CC} = 1.8 V to 5.5 V, AV_{CC} = 1.8 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications), T_a = +75°C (Die) (including subactive mode) unless otherwise specified.

Item	Symbol	Applicable Pins	Values			Unit	Test Conditions	Reference Figure
			Min	Typ	Max			
Segment driver drop voltage	V_{DS}	SEG_1 to SEG_{32}	—	—	0.6	V	I_D = 2 µA V_1 = 2.7 V to 5.5 V	*1
Common driver drop voltage	V_{DC}	COM_1 to COM_4	—	—	0.3	V	I_D = 2 µA V_1 = 2.7 V to 5.5 V	*1
LCD power supply split-resistance	R_{LCD}		0.5	3.0	9.0	MΩ	Between V_1 and V_{SS}	
Liquid crystal display voltage	V_{LCD}	V_1	2.2	—	5.5	V		*2

Notes: 1. The voltage drop from power supply pins V_1, V_2, V_3, and VSS to each segment pin or common pin.

2. When the liquid crystal display voltage is supplied from an external power source, ensure that the following relationship is maintained: $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_{SS}$.

C.7 Block Diagram of Port 8

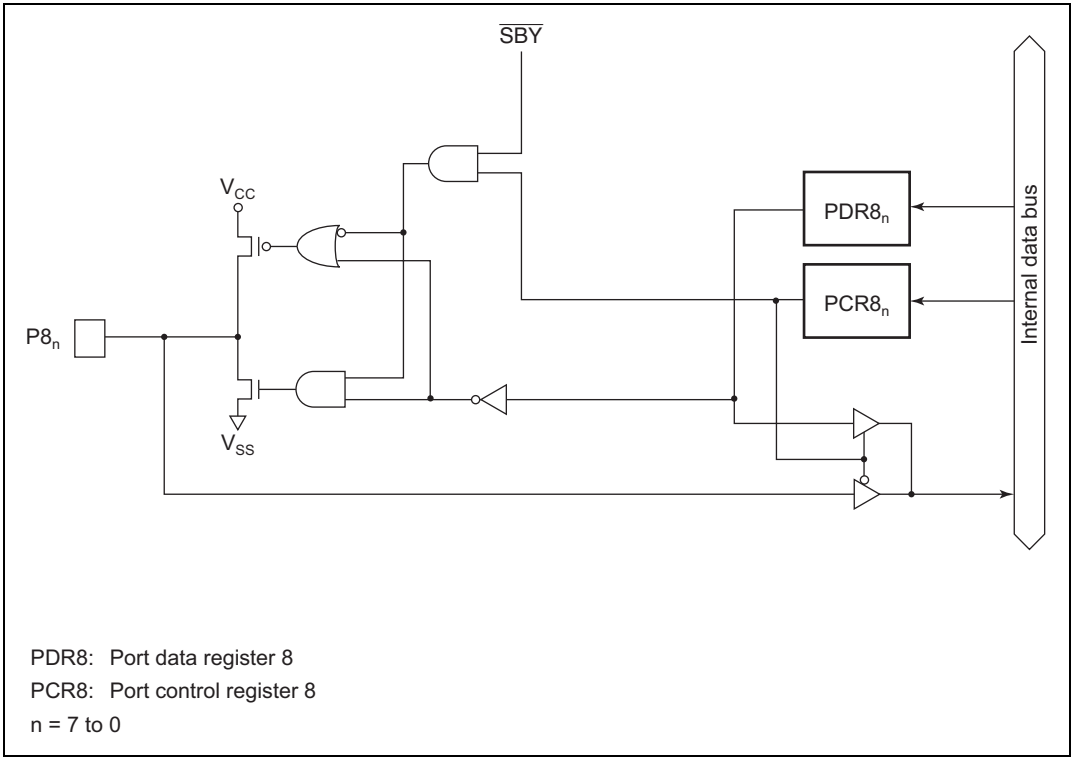


Figure C.7 Port 8 Block Diagram