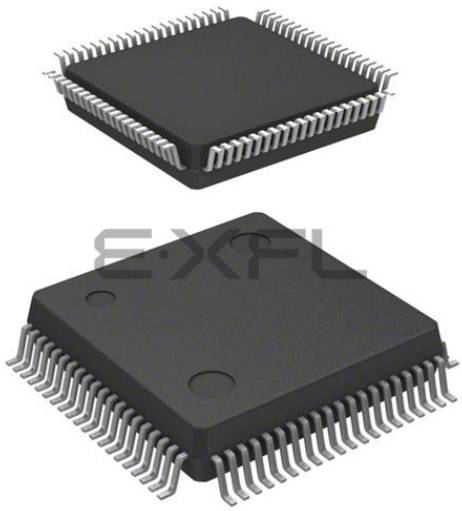


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	10MHz
Connectivity	SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38124hwv

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

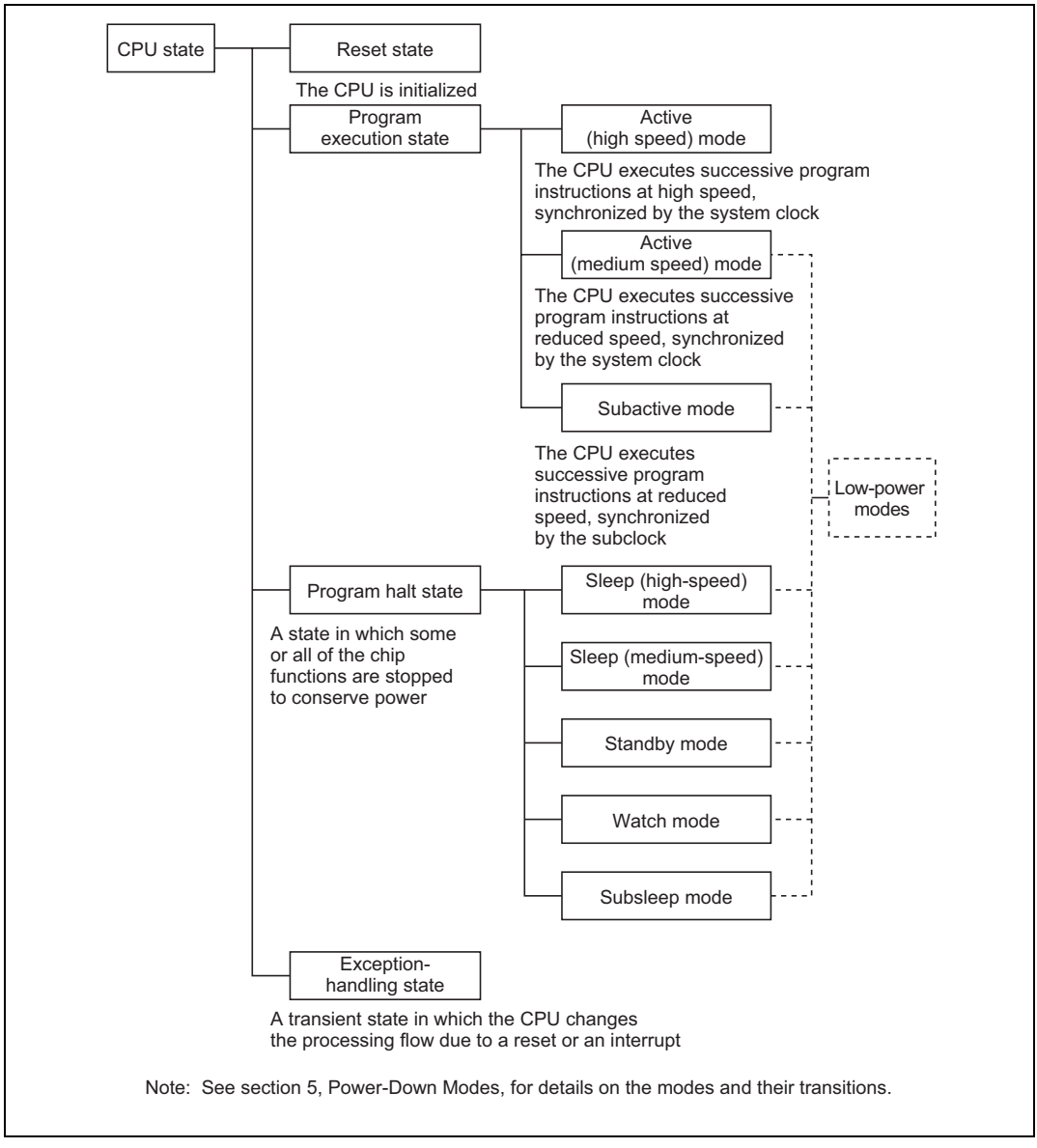


Figure 2.14 CPU Operation States

Prescaler W (PSW)

Prescaler W is a 5-bit counter using a 32.768 kHz/38.4 kHz signal divided by 4 ($\phi_W/4$) as its input clock.

Prescaler W is initialized to H'00 by a reset, and starts counting on exit from the reset state.

Even in standby mode, watch mode, subactive mode, or subsleep mode, prescaler W continues functioning so long as clock signals are supplied to pins X1 and X2.

Prescaler W can be reset by setting 1s in bits TMA3 and TMA2 of timer mode register A (TMA).

Output from prescaler W can be used to drive timer A, in which case timer A functions as a time base for timekeeping.

5.2.2 Clearing Sleep Mode

Sleep mode is cleared by any interrupt (timer A, timer C, timer F, timer G, asynchronous event counter, IRQAEC, IRQ_4, IRQ_3, IRQ_1, IRQ_0, WKP_7 to WKP_0, SCI3, A/D converter), or by input at the $\overline{RES}$ pin.

- Clearing by interrupt

  When an interrupt is requested, sleep mode is cleared and interrupt exception handling starts. A transition is made from sleep (high-speed) mode to active (high-speed) mode, or from sleep (medium-speed) mode to active (medium-speed) mode. Sleep mode is not cleared if the I bit of the condition code register (CCR) is set to 1 or the particular interrupt is disabled in the interrupt enable register.

  To synchronize the interrupt request signal with the system clock, up to 2/ϕ(s) delay may occur after the interrupt request signal occurrence, before the interrupt exception handling start.

- Clearing by $\overline{RES}$ input

  When the $\overline{RES}$ pin goes low, the CPU goes into the reset state and sleep mode is cleared.

5.2.3 Clock Frequency in Sleep (Medium-Speed) Mode

Operation in sleep (medium-speed) mode is clocked at the frequency designated by the MA1 and MA0 bits in SYSCR1.

- When a oscillator is used

  The table below gives settings for various operating frequencies. Set bits STS2 to STS0 for a wait time at least as long as the oscillation stabilization time.

Table 5.4(1) Clock Frequency and Stabilization Time (H8/38024, H8/38024S, H8/38024R Group)

(Unit: ms)

STS2	STS1	STS0	Wait Time	5 MHz	2 MHz
0	0	0	8,192 states	1.638	4.1
		1	16,384 states	3.277	8.2
	1	0	1,024 states	0.205	0.512
		1	2,048 states	0.410	1.024
1	0	0	4,096 states	0.819	2.048
		1	2 states (Use prohibited with other than external clock)	0.0004	0.001
	1	0	8 states	0.002	0.004
		1	16 states	0.003	0.008

Table 5.4(2) Clock Frequency and Stabilization Time (H8/38124 Group)

(Unit: ms)

STS2	STS1	STS0	Wait Time	5 MHz	2 MHz
0	0	0	8,192 states	1.638	4.1
		1	16,384 states	3.277	8.2
	1	0	32,768 states	6.554	16.4
		1	65,536 states	13.108	32.8
1	0	0	131,072 states	26.216	65.5
		1	2 states (Use prohibited with other than external clock)	0.0004	0.001
	1	0	8 states	0.002	0.004
		1	16 states	0.003	0.008

- When an external clock is used

  STS2 = 1, STS1 = 0, and STS0 = 1 should be set. Other values possible use, but CPU sometimes will start operation before wait time completion.

Register Name	Bit Name		Operation
CKSTPR2	LDCKSTP	1	LCD module standby mode is cleared
		0	LCD is set to module standby mode
	PW1CKSTP	1	PWM1 module standby mode is cleared
		0	PWM1 is set to module standby mode
	WDCKSTP	1	Watchdog timer module standby mode is cleared
		0	Watchdog timer is set to module standby mode
	AECKSTP	1	Asynchronous event counter module standby mode is cleared
		0	Asynchronous event counter is set to module standby mode
	PW2CKSTP	1	PWM2 module standby mode is cleared
		0	PWM2 is set to module standby mode
	LVDCKSTP*	1	LVD module standby mode is cleared
		0	LVD is set to module standby mode

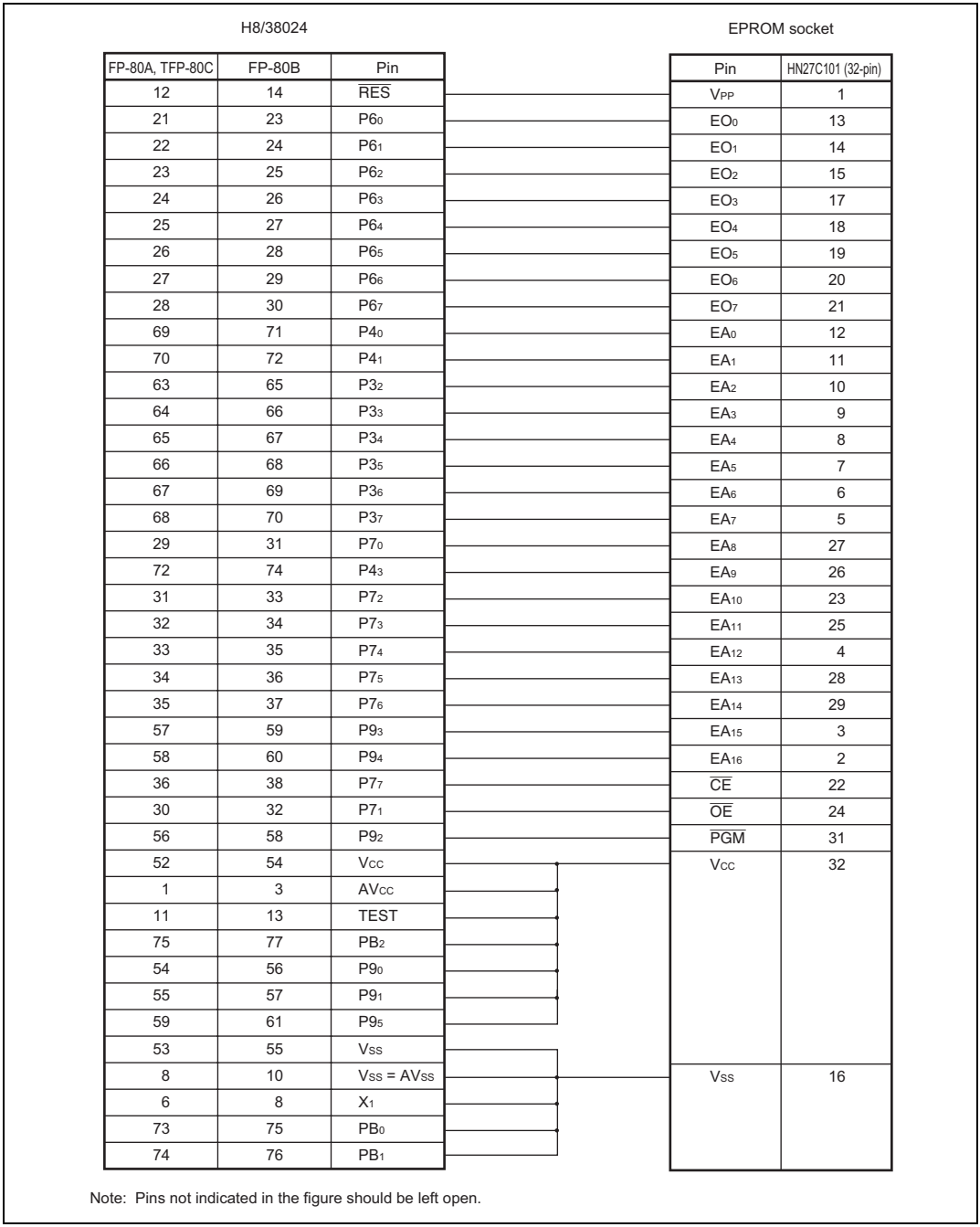
Notes: For details of module operation, see the sections on the individual modules.
* LVDCKSTP is implemented on the H8/38124 group only.

5.10 Usage Note

5.10.1 Contention Between Module Standby and Interrupts

If, due to timing with which a peripheral module issues interrupt requests, the module in question is set to module standby mode before an interrupt is processed, the module will stop with the interrupt request still pending. In this situation, interrupt processing will be repeated indefinitely unless interrupts are prohibited.

It is therefore necessary to ensure that no interrupts are generated when a module is set to module standby mode. The surest way to do this is to specify the module standby mode setting only when interrupts are prohibited (interrupts prohibited using the interrupt enable register or interrupts masked using bit CCR-1).



Note: Pins not indicated in the figure should be left open.

Figure 6.2 Socket Adapter Pin Correspondence (with HN27C101)

6.10.8 Programmer Mode Transition Time

Commands cannot be accepted during the oscillation stabilization period or the programmer mode setup period. After the programmer mode setup time, a transition is made to memory read mode.

Table 6.22 Stipulated Transition Times to Command Wait State

Item	Symbol	Min	Max	Unit	Notes
Oscillation stabilization time(crystal oscillator)	T_{osc1}	10	—	ms	Figure 6.20
Oscillation stabilization time(ceramic oscillator)	T_{osc1}	5	—	ms	
Programmer mode setup time	T_{bmv}	10	—	ms	
Vcc hold time	T_{dwn}	0	—	ms	

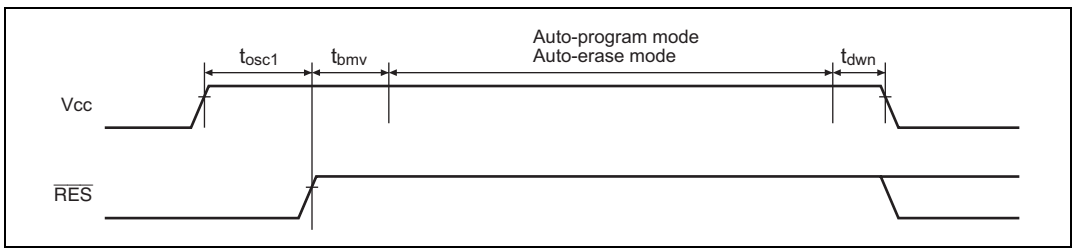


Figure 6.20 Oscillation Stabilization Time, Boot Program Transfer Time, and Power-Down Sequence

6.10.9 Notes on Memory Programming

1. When performing programming using programmer mode on a chip that has been programmed/erased in an on-board programming mode, auto-erasing is recommended before carrying out auto-programming.
2. The flash memory is initially in the erased state when the device is shipped by Renesas Technology. For other chips for which the erasure history is unknown, it is recommended that auto-erasing be executed to check and supplement the initialization (erase) level.

Port Data Register B (PDRB)

Bit	7	6	5	4	3	2	1	0
	PB_7	PB_6	PB_5	PB_4	PB_3	PB_2	PB_1	PB_0
Read/Write	R	R	R	R	R	R	R	R

Reading PDRB always gives the pin states. However, if a port B pin is selected as an analog input channel for the A/D converter by AMR bits CH3 to CH0, that pin reads 0 regardless of the input voltage.

Port Mode Register B (PMRB)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	IRQ1	—	—	—
Initial value	1	1	1	1	0	1	1	1
Read/Write	—	—	—	—	R/W	—	—	—

PMRB is an 8-bit read/write register controlling the selection of the PB_3 pin function. Upon reset, PMRB is initialized to H'F7.

Bits 7 to 4 and 2 to 0—Reserved

Bits 7 to 4 and 2 to 0 are reserved; they are always read as 1 and cannot be modified.

Bit 3—$PB_3/AN_3/\overline{IRQ_1}$ Pin Function Switch (IRQ1)

These bits select whether pin $PB_3/AN_3/\overline{IRQ_1}$ is used as PB_3/AN_3 or as $\overline{IRQ_1}$/TMIC.

Bit 3 IRQ1	Description	
0	Functions as PB_3/AN_3 input pin	(initial value)
1	Functions as $\overline{IRQ_1}$/TMIC input pin	

Note: Rising or falling edge sensing can be selected for the $\overline{IRQ_1}$/TMIC pin.

For TMIC pin setting information, see the Timer More Register C (TMC) description in section 9.3.2, Register Descriptions.

ECH is an 8-bit read-only up-counter that operates either as an independent 8-bit event counter or as the upper 8-bit up-counter of a 16-bit event counter configured in combination with ECL. The external asynchronous event AEVH pin, $\phi/2$, $\phi/4$, $\phi/8$, or the overflow signal from lower 8-bit counter ECL can be selected as the input clock source. ECH can be cleared to H'00 by software, and is also initialized to H'00 upon reset.

Event Counter L (ECL)

Bit	7	6	5	4	3	2	1	0
	ECL7	ECL6	ECL5	ECL4	ECL3	ECL2	ECL1	ECL0
Initial Value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

ECL is an 8-bit read-only up-counter that operates either as an independent 8-bit event counter or as the lower 8-bit up-counter of a 16-bit event counter configured in combination with ECH. The event clock from the external asynchronous event AEVL pin, $\phi/2$, $\phi/4$, or $\phi/8$ is used as the input clock source. ECL can be cleared to H'00 by software, and is also initialized to H'00 upon reset.

Clock Stop Register 2 (CKSTPR2)

Bit	7	6	5	4	3	2	1	0
	LVDCKSTP*	—	—	PW2CKSTP	AECKSTP	WDCKSTP	PW1CKSTP	LDCKSTP
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	—	—	R/W	R/W	R/W	R/W	R/W

Note: * Bits 6 and 5 are also reserved on products other than the H8/38124 Group.

CKSTPR2 is an 8-bit read/write register that performs module standby mode control for peripheral modules. Only the bit relating to the asynchronous event counter is described here. For details of the other bits, see the sections on the relevant modules.

Bit 3—Asynchronous Event Counter Module Standby Mode Control (AECKSTP)

Bit 3 controls setting and clearing of module standby mode for the asynchronous event counter.

AECKSTP	Description	
0	Asynchronous event counter is set to module standby mode	
1	Asynchronous event counter module standby mode is cleared	(initial value)

SCI3 operates as follows when transmitting data.

SCI3 monitors bit TDRE in SSR, and when it is cleared to 0, recognizes that data has been written to TDR and transfers data from TDR to TSR. It then sets bit TDRE to 1 and starts transmitting. If bit TIE in SCR3 is set to 1 at this time, a TXI request is made.

Serial data is transmitted from the TXD_{32} pin using the relevant data transfer format in table 10.11. When the stop bit is sent, SCI3 checks bit TDRE. If bit TDRE is cleared to 0, SCI3 transfers data from TDR to TSR, and when the stop bit has been sent, starts transmission of the next frame. If bit TDRE is set to 1, bit TEND in SSR bit is set to 1the mark state, in which 1s are transmitted, is established after the stop bit has been sent. If bit TEIE in SCR3 is set to 1 at this time, a TEI request is made.

Figure 10.7 shows an example of the operation when transmitting in asynchronous mode.

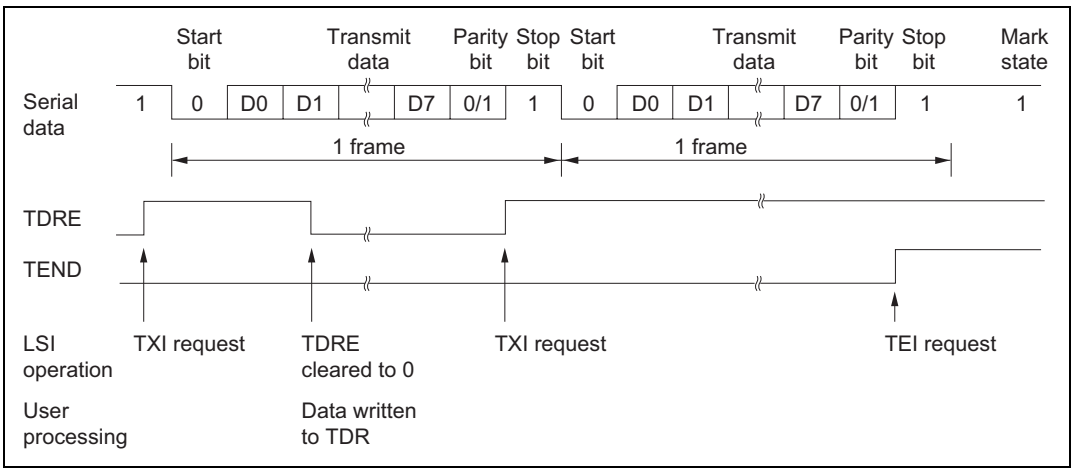


Figure 10.7 Example of Operation when Transmitting in Asynchronous Mode (8-bit data, parity, 1 stop bit)

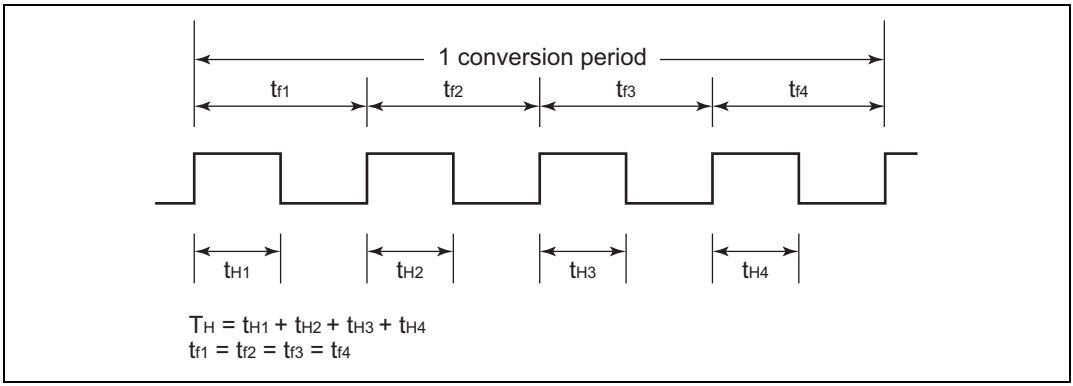


Figure 11.2 PWM Output Waveform

11.3.2 PWM Operation Modes

PWM operation modes are shown in table 11.3.

Table 11.3 PWM Operation Modes

Operation Mode	Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	Module Standby
PWCRm	Reset	Functions	Functions	Retained	Retained	Retained	Retained	Retained
PWDRUm	Reset	Functions	Functions	Retained	Retained	Retained	Retained	Retained
PWDRLm	Reset	Functions	Functions	Retained	Retained	Retained	Retained	Retained

14.1.3 Pin Description

The pins of the power-on reset circuit and low-voltage detection circuit are listed in table 14.1.

Table 14.1 Pin Description

Pin	Symbol	I/O	Function
Low-voltage detection circuit reference voltage input pin	Vref	Input	Reference voltage input for low-voltage detection circuit
Low-voltage detection circuit power supply drop detection voltage input pin	extD	Input	Power supply drop detection voltage input pin for low-voltage detection circuit
Low-voltage detection circuit power supply rise detection voltage input pin	extU	Input	Power supply rise detection voltage input pin for low-voltage detection circuit

14.1.4 Register Descriptions

The registers of the power-on reset circuit and low-voltage detection circuit are listed in table 14.2.

Table 14.2 Register Descriptions

Name	Symbol	R/W	Initial Value	Address
Low-voltage detection control register	LVDCR	R/W	H'00	H'FF86
Low-voltage detection status register	LVDSR	R/W	H'00	H'FF87
Low-voltage detection counter	LVDCNT	R	H'00	H'FFC3

14.2 Individual Register Descriptions

14.2.1 Low-Voltage Detection Control Register (LVDCR)

Bit	7	6	5	4	3	2	1	0
	LVDE	—	VINTDSEL	VINTUSEL	LVDSEL	LVDRE	LVDDE	LVDUE
Initial value	0*	0	0	0	0*	0*	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * These bits are not initialized by resets trigged by LVDR. They are initialized by power-on resets and watchdog timer resets.

15.2 When Not Using Internal Power Supply Step-Down Circuit

When the internal power supply step-down circuit is not used, connect the external power supply to the CV_{CC} pin and V_{CC} pin, as shown in figure 15.2. The external power supply is then input directly to the internal power supply. The permissible range for the power supply voltage is 2.7 V to 3.6 V. Operation cannot be guaranteed if a voltage outside this range (less than 3.0 V or more than 3.6 V) is input.

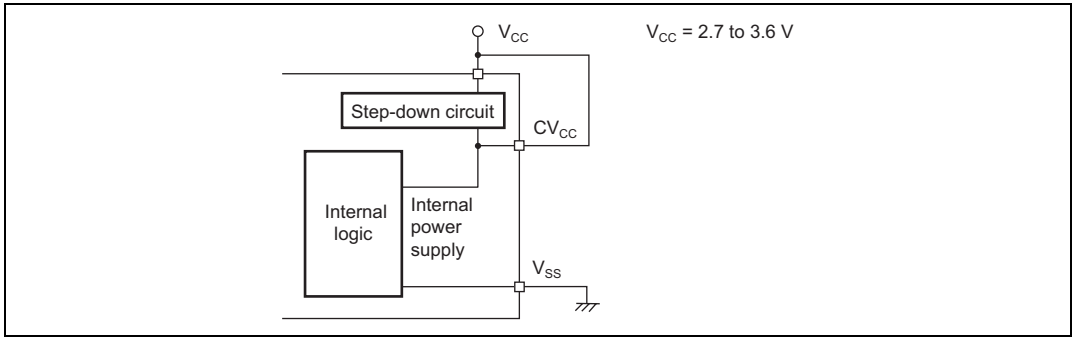


Figure 15.2 Power Supply Connection when Internal Step-Down Circuit is Not Used

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Input capacitance	C_{in}	All input pins except power supply pin	—	—	15.0	pF	f = 1 MHz, V_{IN} = 0.0 V, T_a = 25°C	
Active mode current consumption	I_{OPE1}	V_{CC}	—	0.6	—	mA	Active (high-speed) mode V_{CC} = 2.7 V, f_{OSC} = 2 MHz	*1 *3 *4 Approx. max. value = 1.1 × Typ.
			—	1.0	—			*2 *3 *4 Approx. max. value = 1.1 × Typ.
			—	0.8	—		Active (high-speed) mode V_{CC} = 5 V, f_{OSC} = 2 MHz	*1 *3 *4 Approx. max. value = 1.1 × Typ.
			—	1.5	—			*2 *3 *4 Approx. max. value = 1.1 × Typ.
			—	1.6	—		Active (high-speed) mode V_{CC} = 5 V, f_{OSC} = 4 MHz	*1 *3 *4 Approx. max. value = 1.1 × Typ.
			—	2.0	—			*2 *3 *4
			—	3.3	7.0		Active (high-speed) mode V_{CC} = 5 V, f_{OSC} = 10 MHz	*1 *3 *4
			—	4.0	7.0			*2 *3 *4

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Reference Figure
Input pin high width	t_{IH}	$\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ3}$, $\overline{IRQ4}$, IRQAEC, $\overline{WKP0}$ to $\overline{WKP7}$, TMIC, TMIF, TMIG, $\overline{ADTRG}$	2	—	—	t_{cyc} t_{subcyc}		Figure 16.4
		AEVL, AEVH	0.5	—	—	t_{OSC}		
Input pin low width	t_{IL}	$\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ3}$, $\overline{IRQ4}$, IRQAEC, $\overline{WKP0}$ to $\overline{WKP7}$, TMIC, TMIF, TMIG, $\overline{ADTRG}$	2	—	—	t_{cyc} t_{subcyc}		Figure 16.4
		AEVL, AEVH	0.5	—	—	t_{OSC}		
UD pin minimum transition width	t_{UDH} t_{UDL}	UD	4	—	—	t_{cyc} t_{subcyc}		Figure 16.7

Notes: 1. Determined by the SA1 and SA0 bits in the system control register 2 (SYSCR2).

2. These characteristics are given as ranges between minimum and maximum values in order to account for factors such as temperature, power supply voltage, and variation among production lots. When designing systems, make sure to give due consideration to the SPEC range. Please contact a Renesas sales or support representative for actual performance data on the product.

Table 16.24 Serial Interface (SCI3) Timing

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise specified

Item		Symbol	Values Min	Typ	Max	Unit	Test Condition	Reference Figure
Input clock cycle	Asynchronous	t_{scyc}	4	—	—	t_{cyc} or t_{subcyc}		Figure 16.5
	Clocked synchronous		6	—	—			
Input clock pulse width		t_{SCKW}	0.4	—	0.6	t_{scyc}		Figure 16.5
Transmit data delay time (clocked synchronous)		t_{TXD}	—	—	1	t_{cyc} or t_{subcyc}		Figure 16.6
Receive data setup time (clocked synchronous)		t_{RXS}	150.0	—	—	ns		Figure 16.6
Receive data hold time (clocked synchronous)		t_{RXH}	150.0	—	—	ns		Figure 16.6

Appendix B Internal I/O Registers

B.1 Addresses

Upper Address: H'F0

Lower Address	Register Name	Bit Names								Module Name
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'20	FLMCR1	—	SWE	ESU	PSU	EV	PV	E	P	ROM
H'21	FLMCR2	FLER	—	—	—	—	—	—	—	
H'22	FLPWCR	PDWND	—	—	—	—	—	—	—	
H'23	EBR	—	—	—	EB4	EB3	EB2	EB1	EB0	
H'24										
H'25										
H'26										
H'27										
H'28										
H'29										
H'2A										
H'2B	FENR	FLSHE	—	—	—	—	—	—	—	
H'2C										
H'2D										
H'2E										
H'2F										

ADRRH—A/D Result Register H **H'C4** **A/D Converter**
ADRRL—A/D Result Register L **H'C5**

ADRRH

Bit	7	6	5	4	3	2	1	0
	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R	R	R	R	R

A/D conversion result

ADRRL

Bit	7	6	5	4	3	2	1	0
	ADR1	ADR0	—	—	—	—	—	—
Initial value	Undefined	Undefined	—	—	—	—	—	—
Read/Write	R	R	—	—	—	—	—	—

A/D conversion result

ADSR—A/D Start Register **H'C7** **A/D Converter**

Bit	7	6	5	4	3	2	1	0
	ADSF	—	—	—	—	—	—	—
Initial value	0	1	1	1	1	1	1	1
Read/Write	R/W	—	—	—	—	—	—	—

A/D Start Flag

0	Read	Indicates completion of A/D conversion
	Write	Stops A/D conversion
1	Read	Indicates A/D conversion in progress
	Write	Starts A/D conversion

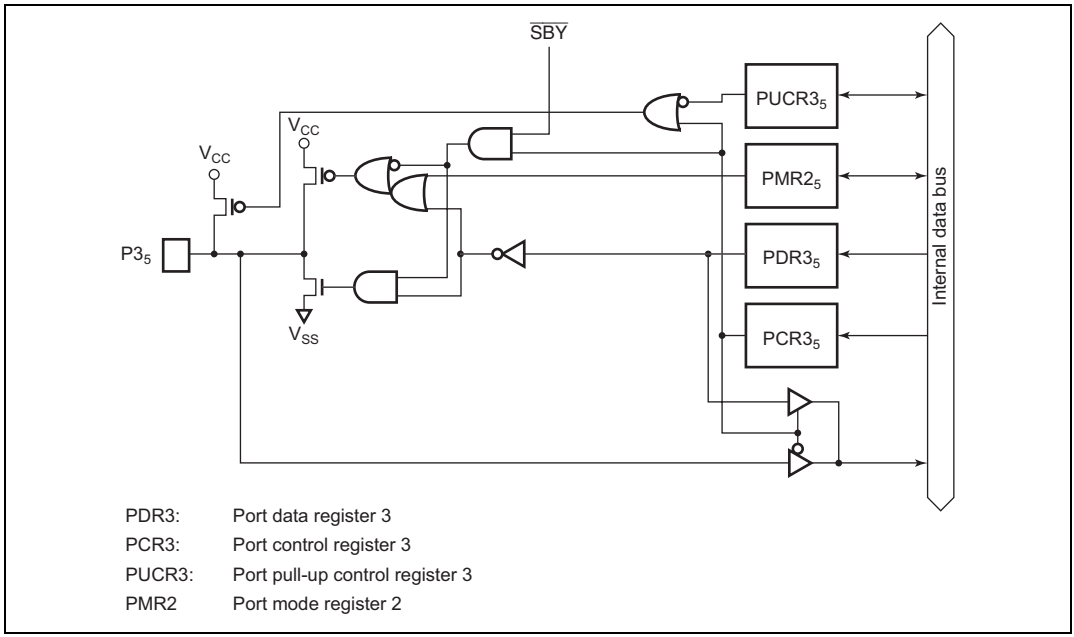


Figure C.2(b) Port 3 Block Diagram (Pin $P3_5$)