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Details	
Product Status	Active
Core Processor	H8/300L
Core Size	8-Bit
Speed	10MHz
Connectivity	SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38124wv

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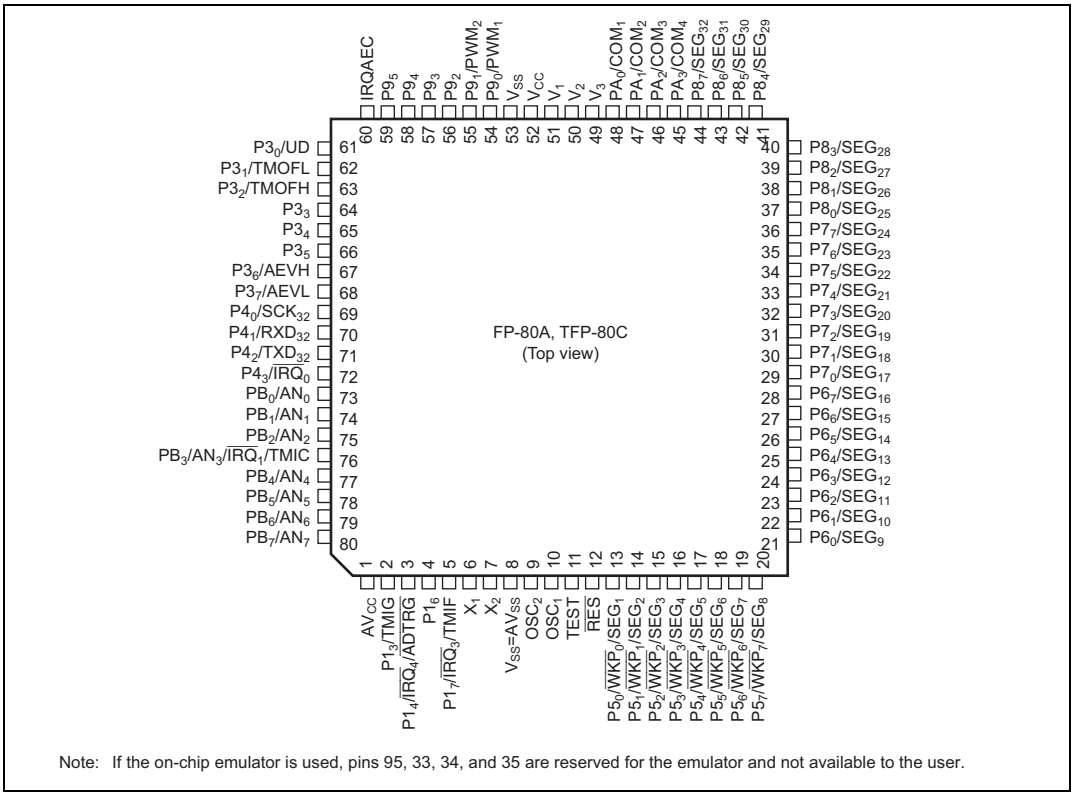
1.3 Pin Arrangement and Functions

1.3.1 Pin Arrangement

The H8/38024 Group, H8/38024R Group, H8/38024S Group, and H8/38124 Group pin arrangements are shown in figures 1.2, 1.3, and 1.4. The bonding pad location diagram of the HCD64338024, HCD64338023, HCD64338022, HCD64338021, and HCD64338020 is shown in figure 1.5. The bonding pad coordinates of the HCD64338024, HCD64338023, HCD64338022, HCD64338021, and HCD64338020 are given in table 1.2. The bonding pad location diagram of the HCD64F38024, HCD64F38024R is shown in figure 1.6. The bonding pad coordinates of the HCD64F38024 are given in table 1.3. The bonding pad location diagram of the HCD64338024S, HCD64338023S, HCD64338022S, HCD64338021S, and HCD64338020S is shown in figure 1.7. The bonding pad coordinates of the HCD64338024S, HCD64338023S, HCD64338022S, HCD64338021S, and HCD64338020S are given in table 1.4.



Note: If the on-chip emulator is used, pins 95, 33, 34, and 35 are reserved for the emulator and not available to the user.

Figure 1.2(1) Pin Arrangement (FP-80A, TFP-80C: Top View, H8/38024 Group, H8/38024R Group, H8/38024S Group)

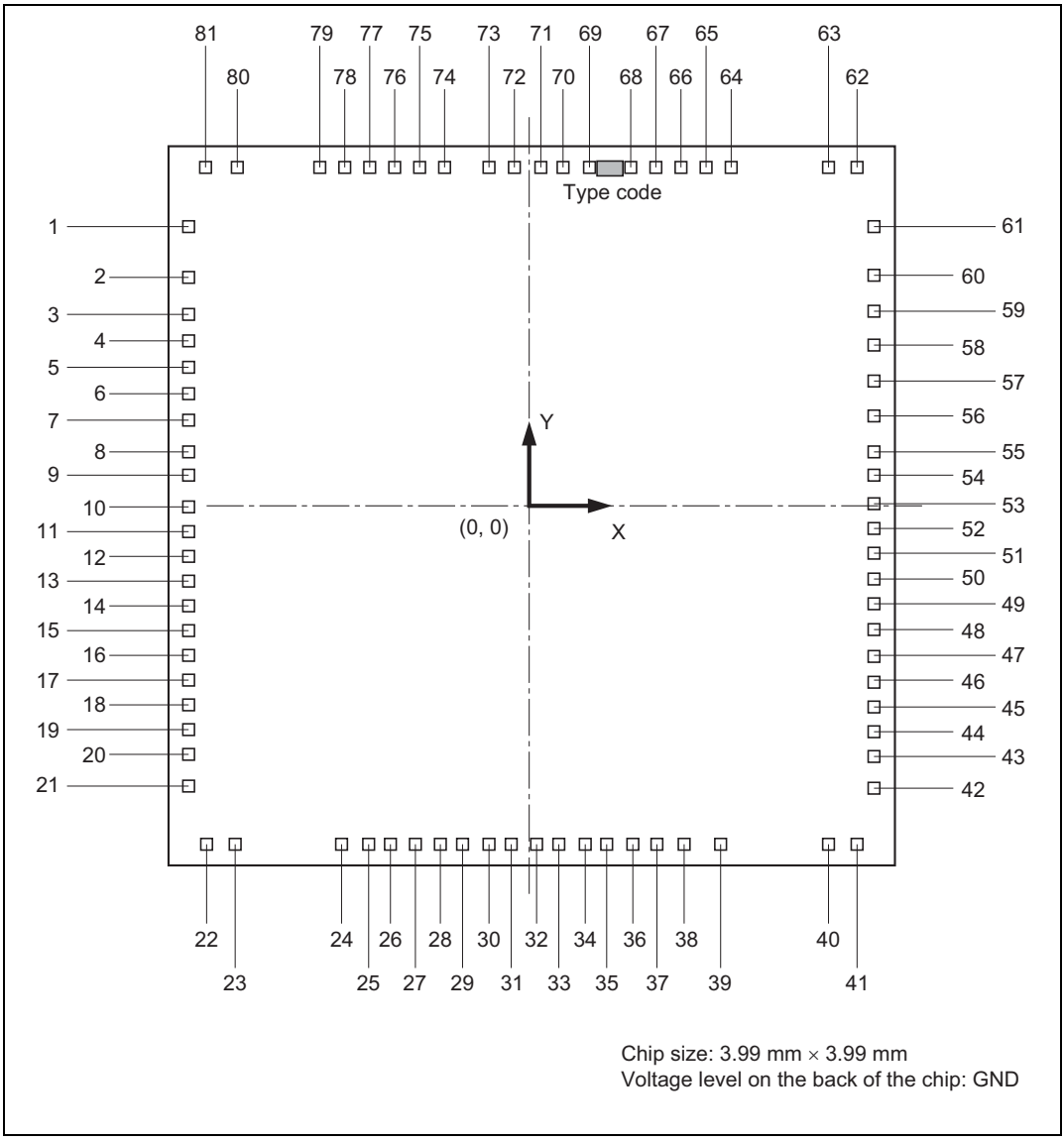


Figure 1.5 Bonding Pad Location Diagram of HCD64338024, HCD64338023, HCD64338022, HCD64338021, and HCD64338020 (Top View)

- When a oscillator is used

  The table below gives settings for various operating frequencies. Set bits STS2 to STS0 for a wait time at least as long as the oscillation stabilization time.

Table 5.4(1) Clock Frequency and Stabilization Time (H8/38024, H8/38024S, H8/38024R Group)

(Unit: ms)

STS2	STS1	STS0	Wait Time	5 MHz	2 MHz
0	0	0	8,192 states	1.638	4.1
		1	16,384 states	3.277	8.2
	1	0	1,024 states	0.205	0.512
		1	2,048 states	0.410	1.024
1	0	0	4,096 states	0.819	2.048
		1	2 states (Use prohibited with other than external clock)	0.0004	0.001
	1	0	8 states	0.002	0.004
		1	16 states	0.003	0.008

Table 5.4(2) Clock Frequency and Stabilization Time (H8/38124 Group)

(Unit: ms)

STS2	STS1	STS0	Wait Time	5 MHz	2 MHz
0	0	0	8,192 states	1.638	4.1
		1	16,384 states	3.277	8.2
	1	0	32,768 states	6.554	16.4
		1	65,536 states	13.108	32.8
1	0	0	131,072 states	26.216	65.5
		1	2 states (Use prohibited with other than external clock)	0.0004	0.001
	1	0	8 states	0.002	0.004
		1	16 states	0.003	0.008

- When an external clock is used

  STS2 = 1, STS1 = 0, and STS0 = 1 should be set. Other values possible use, but CPU sometimes will start operation before wait time completion.

6.6.3 Erase Block Register (EBR)

Bit	7	6	5	4	3	2	1	0
	—	—	—	EB4	EB3	EB2	EB1	EB0
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

EBR specifies the flash memory erase area block. EBR is initialized to H'00 when the SWE bit in FLMCR1 is 0. Do not set more than one bit at a time, as this will cause all the bits in EBR to be automatically cleared to 0. When each bit is set to 1 in EBR, the corresponding block can be erased. Other blocks change to the erase-protection state. See table 6.6 for the method of dividing blocks of the flash memory. When the whole bits are to be erased, erase them in turn in unit of a block.

Table 6.6 Division of Blocks to Be Erased

EBR	Bit Name	Block (Size)	Address
0	EB0	EB0 (1 Kbyte)	H'0000 to H'03FF
1	EB1	EB1 (1 Kbyte)	H'0400 to H'07FF
2	EB2	EB2 (1 Kbyte)	H'0800 to H'0BFF
3	EB3	EB3 (1 Kbyte)	H'0C00 to H'0FFF
4	EB4	EB4 (12 Kbytes)	H'1000 to H'3FFF (HD64F38122)
		EB4 (28 Kbytes)	H'1000 to H'7FFF (HD64F38124, HD64F38024, HD64F38024R)

6.6.4 Flash Memory Power Control Register (FLPWCR)

Bit	7	6	5	4	3	2	1	0
	PDWND	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	—	—	—	—	—	—	—

FLPWCR enables or disables a transition to the flash memory power-down mode when the LSI switches to subactive mode. The power supply circuit can be read in the subactive mode, although it is partly halted in the power-down mode.

Port Data Register 5 (PDR5)

Bit	7	6	5	4	3	2	1	0
	$P5_7$	$P5_6$	$P5_5$	$P5_4$	$P5_3$	$P5_2$	$P5_1$	$P5_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR5 is an 8-bit register that stores data for port 5 pins $P5_7$ to $P5_0$. If port 5 is read while PCR5 bits are set to 1, the values stored in PDR5 are read, regardless of the actual pin states. If port 5 is read while PCR5 bits are cleared to 0, the pin states are read.

Upon reset, PDR5 is initialized to H'00.

Port Control Register 5 (PCR5)

Bit	7	6	5	4	3	2	1	0
	$PCR5_7$	$PCR5_6$	$PCR5_5$	$PCR5_4$	$PCR5_3$	$PCR5_2$	$PCR5_1$	$PCR5_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PCR5 is an 8-bit register for controlling whether each of the port 5 pins $P5_7$ to $P5_0$ functions as an input pin or output pin. Setting a PCR5 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. PCR5 and PDR5 settings are valid when the corresponding pins are designated for general-purpose input/output by PMR5 and bits SGS3 to SGS0 in LPCR.

Upon reset, PCR5 is initialized to H'00.

PCR5 is a write-only register, which is always read as all 1s.

Port Pull-Up Control Register 5 (PUCR5)

Bit	7	6	5	4	3	2	1	0
	$PUCR5_7$	$PUCR5_6$	$PUCR5_5$	$PUCR5_4$	$PUCR5_3$	$PUCR5_2$	$PUCR5_1$	$PUCR5_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PUCR5 controls whether the MOS pull-up of each of port 5 pins $P5_7$ to $P5_0$ is on or off. When a PCR5 bit is cleared to 0, setting the corresponding PUCR5 bit to 1 turns on the MOS pull-up for the corresponding pin, while clearing the bit to 0 turns off the MOS pull-up.

Upon reset, PUCR5 is initialized to H'00.

Port Mode Register 5 (PMR5)

Bit	7	6	5	4	3	2	1	0
	WKP_7	WKP_6	WKP_5	WKP_4	WKP_3	WKP_2	WKP_1	WKP_0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PMR5 is an 8-bit read/write register, controlling the selection of pin functions for port 5 pins.

Upon reset, PMR5 is initialized to H'00.

Bit n—$P5_n/\overline{WKP}_n/SEG_{n+1}$ Pin Function Switch (WKPn)

When pin P5n/$\overline{WKP}$n/SEGn+1 is not used as SEG_{n+1}, these bits select whether the pin is used as P5n or $\overline{WKP}_n$.

Bit n WKPn	Description	
0	Functions as P5n I/O pin	(initial value)
1	Functions as $\overline{WKP}_n$ input pin	

(n = 7 to 0)

Note: For use as SEG_{n+1}, see section 13.2.1, LCD Port Control Register (LPCR).

8.13 Application Note

8.13.1 The Management of the Un-Use Terminal

If an I/O pin not used by the user system is floating, pull it up or down.

- If an unused pin is an input pin, handle it in one of the following ways:
  - Pull it up to V_{CC} with an on-chip pull-up MOS.
  - Pull it up to V_{CC} with an external resistor of approximately 100 kΩ.
  - Pull it down to V_{SS} with an external resistor of approximately 100 kΩ.
  - For a pin also used by the A/D converter, pull it up to AV_{CC}.
- If an unused pin is an output pin, handle it in one of the following ways:
  - Set the output of the unused pin to high and pull it up to V_{CC} with an on-chip pull-up MOS.
  - Set the output of the unused pin to high and pull it up to V_{CC} with an external resistor of approximately 100 kΩ.
  - Set the output of the unused pin to low and pull it down to GND with an external resistor of approximately 100 kΩ.

9.2.4 Timer A Operation States

Table 9.3 summarizes the timer A operation states.

Table 9.3 Timer A Operation States

Operation Mode		Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	Module Standby
TCA	Interval	Reset	Functions	Functions	Halted	Halted	Halted	Halted	Halted
	Clock time base	Reset	Functions	Functions	Functions	Functions	Functions	Halted	Halted
TMA		Reset	Functions	Retained	Retained	Functions	Retained	Retained	Retained

Note: When the real-time clock time base function is selected as the internal clock of TCA in active mode or sleep mode, the internal clock is not synchronous with the system clock, so it is synchronized by a synchronizing circuit. This may result in a maximum error of 1/ϕ (s) in the count cycle.

9.2.5 Application Note

When bit 0 (TACKSTP) of the clock stop register 1 (CKSTPR1) is cleared to 0, bit 3 (TMA3) of the timer mode register A (TMA) cannot be rewritten.

Set bit 0 (TACKSTP) of the clock stop register 1 (CKSTPR1) to 1 before rewriting bit 3 (TMA3) of the timer mode register A (TMA).

7. Relation between RDR reads and bit RDRF

In a receive operation, SCI3 continually checks the RDRF flag. If bit RDRF is cleared to 0 when reception of one frame ends, normal data reception is completed. If bit RDRF is set to 1, this indicates that an overrun error has occurred.

When the contents of RDR are read, bit RDRF is cleared to 0 automatically. Therefore, if bit RDR is read more than once, the second and subsequent read operations will be performed while bit RDRF is cleared to 0. Note that, when an RDR read is performed while bit RDRF is cleared to 0, if the read operation coincides with completion of reception of a frame, the next frame of data may be read. This is illustrated in figure 10.17.

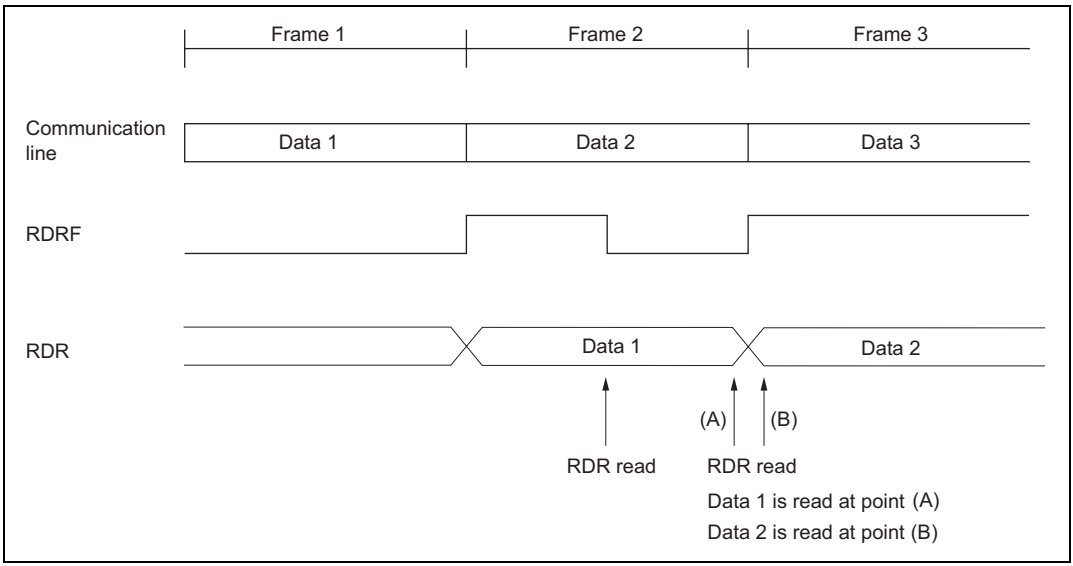


Figure 10.17 Relation between RDR Read Timing and Data

In this case, only a single RDR read operation (not two or more) should be performed after first checking that bit RDRF is set to 1. If two or more reads are performed, the data read the first time should be transferred to RAM, etc., and the RAM contents used. Also, ensure that there is sufficient margin in an RDR read operation before reception of the next frame is completed. To be precise in terms of timing, the RDR read should be completed before bit 7 is transferred in synchronous mode, or before the STOP bit is transferred in asynchronous mode.

8. Transmit and receive operations when making a state transition

Make sure that transmit and receive operations have completely finished before carrying out state transition processing.

9. Switching SCK_{32} function

If pin SCK_{32} is used as a clock output pin by SCI3 in synchronous mode and is then switched to a general input/output pin (a pin with a different function), the pin outputs a low level signal for half a system clock (ϕ) cycle immediately after it is switched.

This can be prevented by either of the following methods according to the situation.

a. When an SCK_{32} function is switched from clock output to non clock-output

   When stopping data transfer, issue one instruction to clear bits TE and RE to 0 and to set bits CKE1 and CKE0 in SCR3 to 1 and 0, respectively. In this case, bit COM in SMR should be left 1. The above prevents SCK_{32} from being used as a general input/output pin. To avoid an intermediate level of voltage from being applied to SCK_{32}, the line connected to SCK_{32} should be pulled up to the V_{CC} level via a resistor, or supplied with output from an external device.

b. When an SCK_{32} function is switched from clock output to general input/output

   When stopping data transfer,

   (i) Issue one instruction to clear bits TE and RE to 0 and to set bits CKE1 and CKE0 in SCR3 to 1 and 0, respectively.

   (ii) Clear bit COM in SMR to 0

   (iii) Clear bits CKE1 and CKE0 in SCR3 to 0

   Note that special care is also needed here to avoid an intermediate level of voltage from being applied to SCK_{32}.

10. Set up at subactive or subsleep mode

At subactive or subsleep mode, SCI3 becomes possible use only at CPU clock is $\phi w/2$.

11. Oscillator use with serial communications interface (H8/38124 Group only)

When implementing the serial communications interface on the H8/38124 Group, the system clock oscillator must be used. The on-chip oscillator should not be used in this case. See on-chip oscillator selection method in section 4.2, System Clock Generator, for information on switching between the system clock oscillator and the on-chip oscillator.

Section 11 10-Bit PWM

11.1 Overview

The H8/38024 Group is provided with two on-chip 10-bit PWMs (pulse width modulators), designated PWM1 and PWM2, with identical functions. The PWMs can be used as D/A converters by connecting a low-pass filter. In this section the suffix m (m = 1 or 2) is used with register names, etc., as in PWDRLm, which denotes the PWDRL registers for each PWM.

11.1.1 Features

Features of the 10-bit PWMs are as follows.

- Choice of four conversion periods
  Any of the following conversion periods can be chosen:
  4,096/ϕ, with a minimum modulation width of 4/ϕ
  2,048/ϕ, with a minimum modulation width of 2/ϕ
  1,024/ϕ, with a minimum modulation width of 1/ϕ
  512/ϕ, with a minimum modulation width of 1/2 ϕ
- Pulse division method for less ripple
- Use of module standby mode enables this module to be placed in standby mode independently when not used.

On the H8/38124 Group it is possible to select between two types of PWM output: pulse-division PWM and event counter PWM (PWM incorporating AEC). (The H8/38024 Group, H8/38024F-ZTAT Group, and H8/38024S Group can only produce pulse-division PWM output.) Refer to section 9.7, Asynchronous Event Counter, for information on event counter PWM.

14.1.3 Pin Description

The pins of the power-on reset circuit and low-voltage detection circuit are listed in table 14.1.

Table 14.1 Pin Description

Pin	Symbol	I/O	Function
Low-voltage detection circuit reference voltage input pin	Vref	Input	Reference voltage input for low-voltage detection circuit
Low-voltage detection circuit power supply drop detection voltage input pin	extD	Input	Power supply drop detection voltage input pin for low-voltage detection circuit
Low-voltage detection circuit power supply rise detection voltage input pin	extU	Input	Power supply rise detection voltage input pin for low-voltage detection circuit

14.1.4 Register Descriptions

The registers of the power-on reset circuit and low-voltage detection circuit are listed in table 14.2.

Table 14.2 Register Descriptions

Name	Symbol	R/W	Initial Value	Address
Low-voltage detection control register	LVDCR	R/W	H'00	H'FF86
Low-voltage detection status register	LVDSR	R/W	H'00	H'FF87
Low-voltage detection counter	LVDCNT	R	H'00	H'FFC3

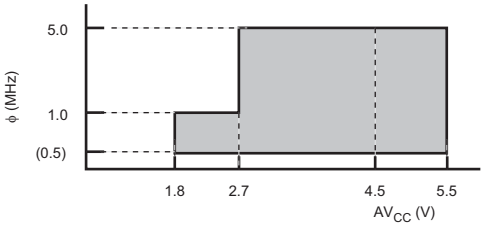
14.2 Individual Register Descriptions

14.2.1 Low-Voltage Detection Control Register (LVDCR)

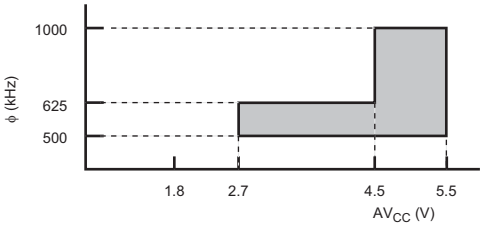
Bit	7	6	5	4	3	2	1	0
	LVDE	—	VINTDSEL	VINTUSEL	LVDSEL	LVDRE	LVDDE	LVDUE
Initial value	0*	0	0	0	0*	0*	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * These bits are not initialized by resets trigged by LVDR. They are initialized by power-on resets and watchdog timer resets.

Analog Power Supply Voltage and A/D Converter Operating Range



- Active (high-speed) mode
- Sleep (high-speed) mode



- Active (medium-speed) mode
- Sleep (medium-speed) mode

Note: 3. When AVCC = 1.8 V to 2.7 V, the operating range is limited to ϕ = 1.0 MHz when using an oscillator, and is ϕ = 0.5 MHz to 1.0 MHz when using an external clock.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Allowable output high current (total)	$\sum -I_{OH}$	All output pins	—	—	10.0	mA		

Notes: Connect the TEST pin to V_{SS}.

1. Pin states during current measurement.

Mode	$\overline{RES}$ Pin	Internal State	Other Pins	LCD Power Supply	Oscillator Pins
Active (high-speed) mode (I_{OPE1})	V_{CC}	Operates	V_{CC}	Halted	System clock oscillator: crystal
Active (medium-speed) mode (I_{OPE2})					Subclock oscillator: Pin X_1 = GND
Sleep mode	V_{CC}	Only on-chip timers operate	V_{CC}	Halted	
Subactive mode	V_{CC}	Operates	V_{CC}	Halted	System clock oscillator:
Subsleep mode	V_{CC}	Only on-chip timers operate, CPU stops	V_{CC}	Halted	crystal Subclock oscillator:
Watch mode	V_{CC}	Only time base operates, CPU stops	V_{CC}	Halted	crystal
Standby mode	V_{CC}	CPU and timers both stop	V_{CC}	Halted	System clock oscillator: crystal Subclock oscillator: Pin X_1 = GND

2. Excludes current in pull-up MOS transistors and output buffers.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Input capacitance	C_{in}	All input pins except power supply pin	—	—	15.0	pF	f = 1 MHz, V_{IN} = 0.0 V, T_a = 25°C	
Active mode current consumption	I_{OPE1}	V_{CC}	—	0.6	—	mA	Active (high-speed) mode V_{CC} = 2.7 V, f_{OSC} = 2 MHz	*1 *3 *4 Approx. max. value = 1.1 × Typ.
			—	1.0	—			*2 *3 *4 Approx. max. value = 1.1 × Typ.
			—	0.8	—		Active (high-speed) mode V_{CC} = 5 V, f_{OSC} = 2 MHz	*1 *3 *4 Approx. max. value = 1.1 × Typ.
			—	1.5	—			*2 *3 *4 Approx. max. value = 1.1 × Typ.
			—	1.6	—		Active (high-speed) mode V_{CC} = 5 V, f_{OSC} = 4 MHz	*1 *3 *4 Approx. max. value = 1.1 × Typ.
			—	2.0	—			*2 *3 *4
			—	3.3	7.0		Active (high-speed) mode V_{CC} = 5 V, f_{OSC} = 10 MHz	*1 *3 *4
			—	4.0	7.0			*2 *3 *4

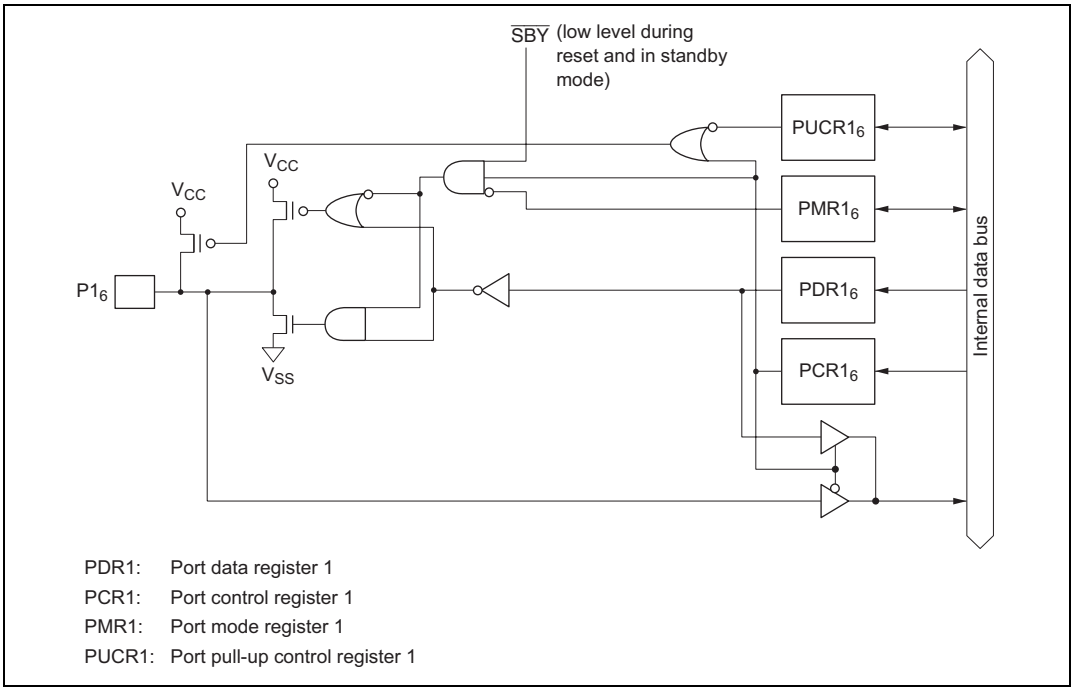


Figure C.1(b) Port 1 Block Diagram (Pin P1$_6$, Products other than H8/38124 Group)

Item	Page	Revision (See Manual for Details)
16.8.2 DC Characteristics Table 16.22 DC Characteristics	506	Table amended

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{WKP_0}$ to $\overline{WKP_7}$, $\overline{IRQ_0}$, $\overline{IRQ_3}$, $\overline{IRQ_4}$, AEVL, AEVH, TMIC, TMIF, TMIG, ADTRG, SCK_{32}	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	V	V_{CC} = 4.0 V to 5.5 V	
			$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$		Other than above	
		$\overline{IRQ_1}$	$V_{CC} \times 0.8$	—	$AV_{CC} + 0.3$	V	V_{CC} = 4.0 V to 5.5 V	
			$V_{CC} \times 0.9$	—	$AV_{CC} + 0.3$		Other than above	

16.8.10 Power Supply Characteristics	525	Newly added

B.1 Addresses	548	Table amended

Lower Address	Register Name	Bit Names Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
H'AA	SCR3	TIE	RIE	TE	RE	—	TEIE	CKE1	CKE0	SCI3
H'AC	SSR	TDRE	RDRF	OER	FER	PER	TEND	—	—	

B.2 Functions	564	Figure amended

SMR—Serial Mode Register H'A8 SCI3

Bit	7	6	5	4	3	2	1	0
	COM	CHR	PE	PM	STOP	MP	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ϕ clock
0	1	ϕ_W/2 clock
1	0	ϕ/16 clock
1	1	ϕ/64 clock

5 Bit Communication

0	5 bits communication disabled
1	5 bits communication enabled

Item	Page	Revision (See Manual for Details)
Appendix F Package Dimensions	642	Figure replaced
Figure F.4 TLP-85V Package Dimensions		
Appendix I Specifications of Chip Tray	648	Figure replaced
Figure I.3 Specifications of Chip Tray for the HCD64338024S, HCD64338023S, HCD64338022S, HCD64338021S, and HCD64338020S		