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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	10MHz
Connectivity	SCI
Peripherals	LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38124wwv

Type	Symbol	Pin No. FP-80A TFP-80C	FP-80B	TLP-85V	Pad No.*1	Pad No.*2	Pad No.*3	I/O	Name and Functions
Clock pins	OSC_1	10	12	F2	11	12	10	Input	These pins connect to a crystal or ceramic oscillator, or can be used to input an external clock. See section 4, Clock Pulse Generators, for a typical connection diagram.
	OSC_2	9	11	E3	10	11	9	Output	
	X_1	6	8	D3	6	7	6	Input	These pins connect to a 32.768-kHz or 38.4-kHz*5 crystal oscillator. See section 4, Clock Pulse Generators, for a typical connection diagram.
	X_2	7	9	D2	7	8	7	Output	
System control	$\overline{RES}$	12	14	F3	13	14	12	Input	**Reset:** When this pin is driven low, the chip is reset
	TEST	11	13	E2	12	13	11	Input	**Test pin:** This pin is reserved and cannot be used. It should be connected to V_{SS}.
Interrupt pins	$\overline{IRQ_0}$ $\overline{IRQ_1}$ $\overline{IRQ_3}$ $\overline{IRQ_4}$	72 76 5 3	74 78 7 5	C5 B3 D1 B2	73 77 5 3	74 78 6 4	72 76 5 3	Input	**IRQ interrupt request 0, 1, 3, and 4:** These are input pins for edge-sensitive external interrupts, with a selection of rising or falling edge
	IRQAEC	60	62	C10	61	62	60	Input	**Asynchronous event counter event signal:** This is an interrupt input pin for enabling asynchronous event input. On the H8/38124 Group, this must be fixed at V_{CC} or GND because the oscillator is selected by the input level during resets. Refer to section 4, Clock Pulse Generators, for information on the selection method.

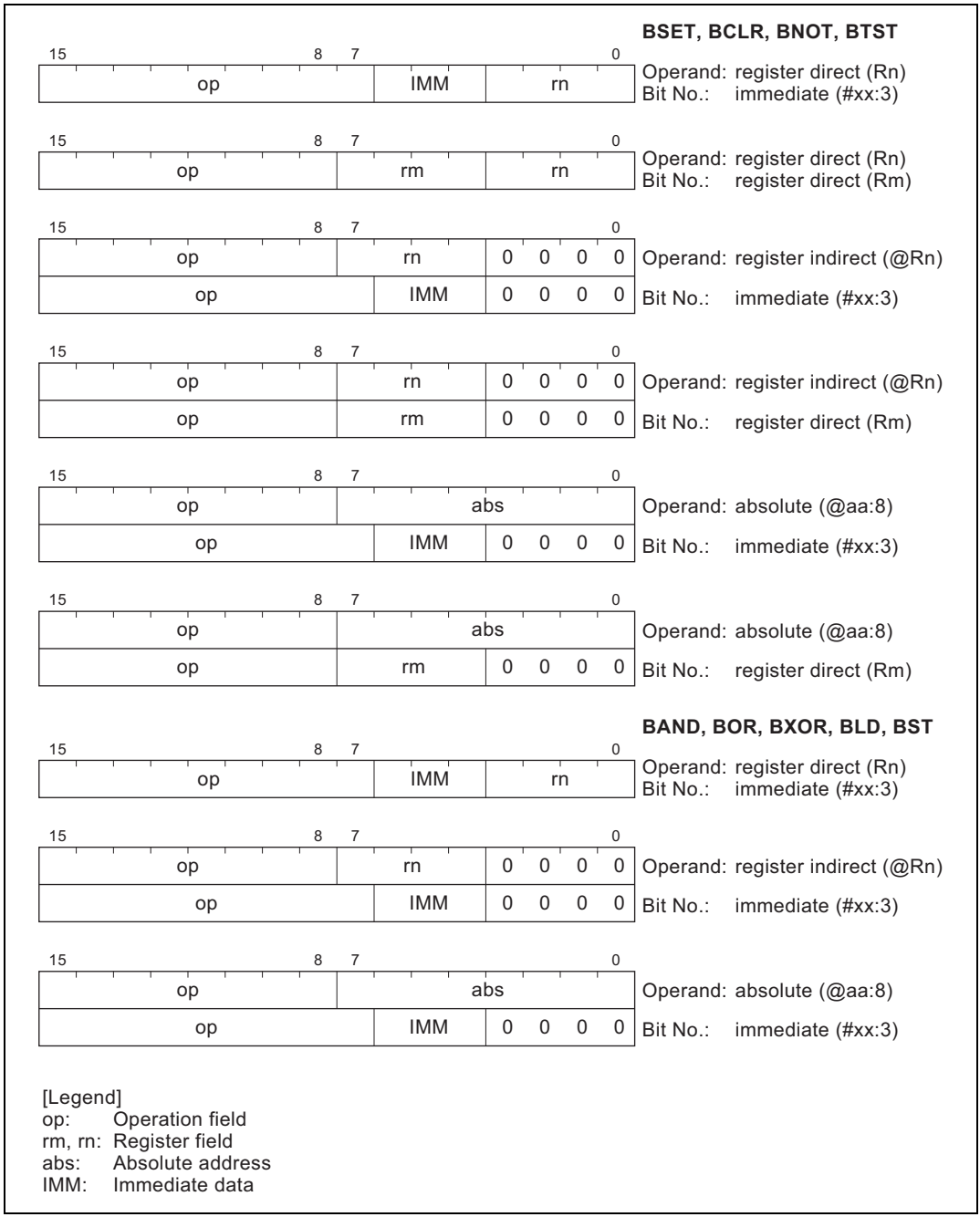


Figure 2.7 Bit Manipulation Instruction Codes

Bit 4—$\overline{IRQ_4}$ Edge Select (IEG4)

Bit 4 selects the input sensing of the $\overline{IRQ_4}$ pin and $\overline{ADTRG}$ pin.

Bit 4 IEG4	Description	
0	Falling edge of $\overline{IRQ_4}$ and $\overline{ADTRG}$ pin input is detected	(initial value)
1	Rising edge of $\overline{IRQ_4}$ and $\overline{ADTRG}$ pin input is detected	

Bit 3—$\overline{IRQ_3}$ Edge Select (IEG3)

Bit 3 selects the input sensing of the $\overline{IRQ_3}$ pin and TMIF pin.

Bit 3 IEG3	Description	
0	Falling edge of $\overline{IRQ_3}$ and TMIF pin input is detected	(initial value)
1	Rising edge of $\overline{IRQ_3}$ and TMIF pin input is detected	

Bit 2—Reserved

Bit 2 is reserved: it can only be written with 0.

Bit 1—$\overline{IRQ_1}$ Edge Select (IEG1)

Bit 1 selects the input sensing of the $\overline{IRQ_1}$ pin and TMIC pin.

Bit 1 IEG1	Description	
0	Falling edge of $\overline{IRQ_1}$ and TMIC pin input is detected	(initial value)
1	Rising edge of $\overline{IRQ_1}$ and TMIC pin input is detected	

Bit 0—$\overline{IRQ_0}$ Edge Select (IEG0)

Bit 0 selects the input sensing of pin $\overline{IRQ_0}$.

Bit 0 IEG0	Description	
0	Falling edge of $\overline{IRQ_0}$ pin input is detected	(initial value)
1	Rising edge of $\overline{IRQ_0}$ pin input is detected	

3.3.6 Interrupt Response Time

Table 3.4 shows the number of wait states after an interrupt request flag is set until the first instruction of the interrupt handler is executed.

Table 3.4 Interrupt Wait States

Item	States	Total
Waiting time for completion of executing instruction*	1 to 13	15 to 27
Saving of PC and CCR to stack	4	
Vector fetch	2	
Instruction fetch	4	
Internal processing	4	

Note: * Not including EEPMOV instruction.

Bit 3 EV	Description	
0	Erase-verify mode is cancelled	(initial value)
1	The flash memory changes to erase-verify mode	

Bit 2—Program-Verify (PV)

This bit is to set changing to or cancelling program-verify mode (do not set SWE, ESU, PSU, EV, E, and P bits at the same time).

Bit 2 PV	Description	
0	Program-verify mode is cancelled	(initial value)
1	The flash memory changes to program-verify mode	

Bit 1—Erase (E)

This bit is to set changing to or cancelling erase mode (do not set SWE, ESU, PSU, EV, PV, and P bits at the same time).

Bit 1 E	Description	
0	Erase mode is cancelled	(initial value)
1	When this bit is set to 1, while the SWE = 1 and ESU = 1, the flash memory changes to erase mode.	

Bit 0—Program (P)

This bit is to set changing to or cancelling program mode (do not set SWE, ESU, PSU, EV, PV, and E bits at the same time).

Bit 0 P	Description	
0	Program mode is cancelled	(initial value)
1	When this bit is set to 1, while the SWE = 1 and PSU = 1, the flash memory changes to program mode.	

This section only deals with the bits related to timer G and the watchdog timer. For the functions of the bits, see the descriptions of port 3 (POF1) and port 4 (IRQ0).

Bit 2—Watchdog Timer Source Clock (WDCKS)

This bit selects the watchdog timer source clock. Note that stabilization times for the H8/38024, H8/38024S, and H8/38024R Group and for the H8/38124 Group are different.

- **H8/38024, H8/38024S, H8/38024R Group**

Bit 2 WDCKS	Description	
0	Selects ϕ/8192	(initial value)
1	Selects ϕ_W/32	

- **H8/38124 Group**

Bit 2 WDCKS	Description	
0	Selects clock based on timer mode register W (TMW) setting*	(initial value)
1	Selects ϕ_W/32	

Note: * See section 9.6, Watchdog Timer, for details.

Bit 1—TMIG Noise Canceller Select (NCS)

This bit selects controls the noise cancellation circuit of the input capture input signal (TMIG).

Bit 1 NCS	Description	
0	No noise cancellation circuit	(initial value)
1	Noise cancellation circuit	

Port Data Register 5 (PDR5)

Bit	7	6	5	4	3	2	1	0
	$P5_7$	$P5_6$	$P5_5$	$P5_4$	$P5_3$	$P5_2$	$P5_1$	$P5_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR5 is an 8-bit register that stores data for port 5 pins $P5_7$ to $P5_0$. If port 5 is read while PCR5 bits are set to 1, the values stored in PDR5 are read, regardless of the actual pin states. If port 5 is read while PCR5 bits are cleared to 0, the pin states are read.

Upon reset, PDR5 is initialized to H'00.

Port Control Register 5 (PCR5)

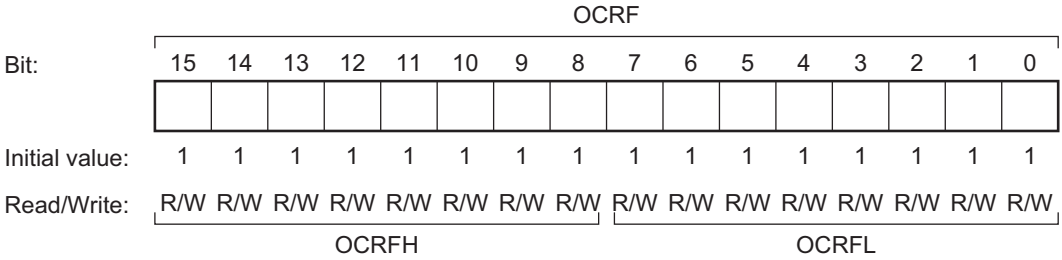
Bit	7	6	5	4	3	2	1	0
	$PCR5_7$	$PCR5_6$	$PCR5_5$	$PCR5_4$	$PCR5_3$	$PCR5_2$	$PCR5_1$	$PCR5_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PCR5 is an 8-bit register for controlling whether each of the port 5 pins $P5_7$ to $P5_0$ functions as an input pin or output pin. Setting a PCR5 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. PCR5 and PDR5 settings are valid when the corresponding pins are designated for general-purpose input/output by PMR5 and bits SGS3 to SGS0 in LPCR.

Upon reset, PCR5 is initialized to H'00.

PCR5 is a write-only register, which is always read as all 1s.

16-bit Output Compare Register (OCRF)
8-bit Output Compare Register (OCRFH)
8-bit Output Compare Register (OCRFL)



OCRF is a 16-bit read/write register composed of the two registers OCRFH and OCRFL. In addition to the use of OCRF as a 16-bit register with OCRFH as the upper 8 bits and OCRFL as the lower 8 bits, OCRFH and OCRFL can also be used as independent 8-bit registers.

OCRFH and OCRFL can be read and written by the CPU, but when they are used in 16-bit mode, data transfer to and from the CPU is performed via a temporary register (TEMP). For details of TEMP, see section 9.4.3, CPU Interface.

OCRFH and OCRFL are each initialized to H'FF upon reset.

a. 16-bit mode (OCRF)

When CKSH2 is cleared to 0 in TCRF, OCRF operates as a 16-bit register. OCRF contents are constantly compared with TCF, and when both values match, CMFH is set to 1 in TCSRF. At the same time, IRRTFH is set to 1 in IRR2. If IENTFH in IENR2 is 1 at this time, an interrupt request is sent to the CPU.

Toggle output can be provided from the TMOFH pin by means of compare matches, and the output level can be set (high or low) by means of TOLH in TCRF.

b. 8-bit mode (OCRFH/OCRFL)

When CKSH2 is set to 1 in TCRF, OCRFH, and OCRFL operate as two independent 8-bit registers. OCRFH contents are compared with TCFH, and OCRFL contents are with TCFL. When the OCRFH (OCRFL) and TCFH (TCFL) values match, CMFH (CMFL) is set to 1 in TCSRF. At the same time, IRRTFH (IRRTFL) is set to 1 in IRR2. If IENTFH (IENTFL) in IENR2 is 1 at this time, an interrupt request is sent to the CPU.

Toggle output can be provided from the TMOFH pin (TMOFL pin) by means of compare matches, and the output level can be set (high or low) by means of TOLH (TOLL) in TCRF.

Mode		Maximum AEVH/AEVL Pin Input Clock Frequency
Active (high-speed), sleep (high-speed)		16 MHz
Active (medium-speed), sleep (medium-speed)	(ϕ/16)	2 • f_{OSC}
	(ϕ/32)	f_{OSC}
	(ϕ/64)	1/2 • f_{OSC}
f_{OSC} = 1 MHz to 4 MHz	(ϕ/128)	1/4 • f_{OSC}
Watch, subactive, subsleep, standby	(ϕw/2)	1000 kHz
	(ϕw/4)	500 kHz
ϕw = 32.768 kHz or 38.4 kHz*	(ϕw/8)	250 kHz

Note: * Does not apply to H8/38124 Group.

3. When using the clock in the 16-bit mode, set CUEH to 1 first, then set CRCH to 1 in ECCSR. Or, set CUEH and CRCH simultaneously before inputting the clock. After that, do not change the CUEH value while using in the 16-bit mode. Otherwise, an error counter increment may occur. Also, to reset the counter, clear CRCH and CRCL to 0 simultaneously or clear CRCL and CRCH to 0 sequentially, in that order.
4. When ECPWME in AEGSR is 1, event counter PWM is operating and therefore ECPWCRH, ECPWCRL, ECPWDRH, and ECPWDRL should not be modified.

   When changing the data, event counter PWM must be halted by clearing ECPWME to 0 in AEGSR before modifying these registers.
5. The event counter PWM data register and event counter PWM compare register must be set so that event counter PWM data register < event counter PWM compare register. If the settings do not satisfy this condition, do not set ECPWME to 1 in AEGSR.
6. As synchronization is established internally when an IRQAEC interrupt is generated, a maximum error of 1 t_{cyc} will occur between clock halting and interrupt acceptance.

10.1.2 Block Diagram

Figure 10.1 shows a block diagram of SCI3.

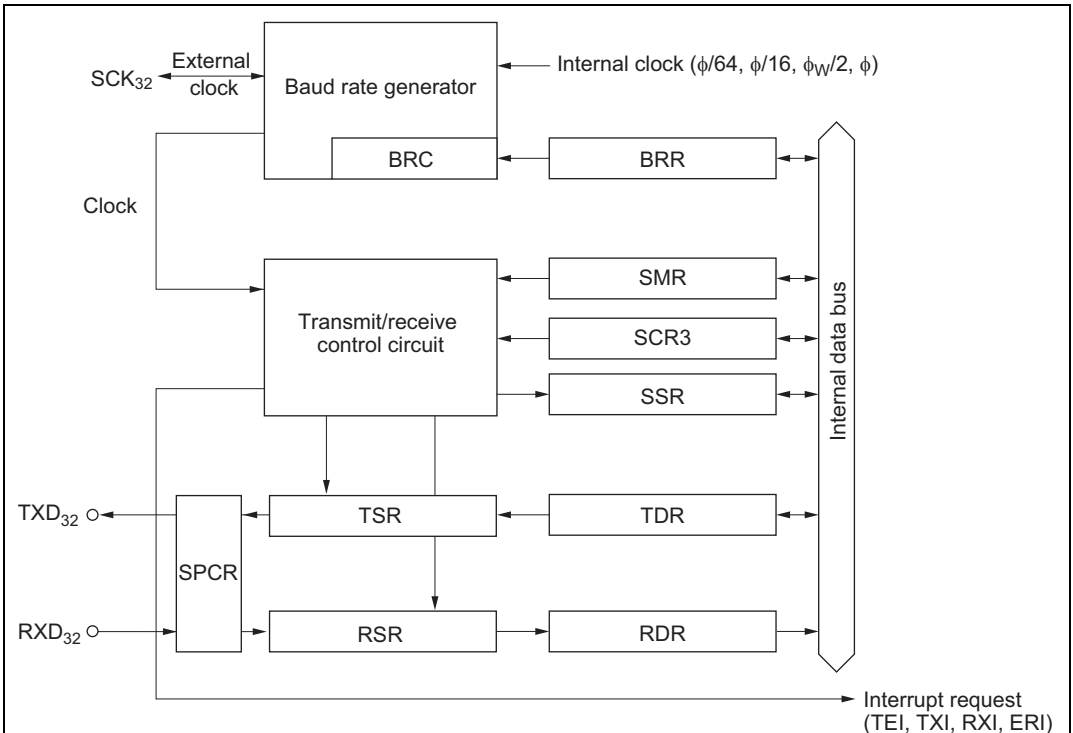


Figure 10.1 SCI3 Block Diagram

11.2.3 Clock Stop Register 2 (CKSTPR2)

Bit	7	6	5	4	3	2	1	0
	LVDCKSTP*	—	—	PW2CKSTP	AECKSTP	WDCKSTP	PW1CKSTP	LDCKSTP
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	—	—	R/W	R/W	R/W	R/W	R/W

Note: * Bits 6 and 5 are also reserved on products other than the H8/38124 Group.

CKSTPR2 is an 8-bit read/write register that performs module standby mode control for peripheral modules. Only the bit relating to the PWM is described here. For details of the other bits, see the sections on the relevant modules.

Bits 4 and 1—PWM Module Standby Mode Control (PWmCKSTP)

Bits 4 and 1 control setting and clearing of module standby mode for the PWMm.

PWmCKSTP	Description	
0	PWMm is set to module standby mode	
1	PWMm module standby mode is cleared	(initial value)

12.2 Register Descriptions

12.2.1 A/D Result Registers (ADRRH, ADRRL)

Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	—	—	—	—	—	—
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	—	—	—	—	—	—
Read/Write	R	R	R	R	R	R	R	R	R	R	—	—	—	—	—	—
	ADRRH								ADRRL							

ADRRH and ADRRL together comprise a 16-bit read-only register for holding the results of analog-to-digital conversion. The upper 8 bits of the data are held in ADRRH, and the lower 2 bits in ADRRL.

ADRRH and ADRRL can be read by the CPU at any time, but the ADRRH and ADRRL values during A/D conversion are not fixed. After A/D conversion is complete, the conversion result is stored as 10-bit data, and this data is held until the next conversion operation starts.

ADRRH and ADRRL are not cleared on reset.

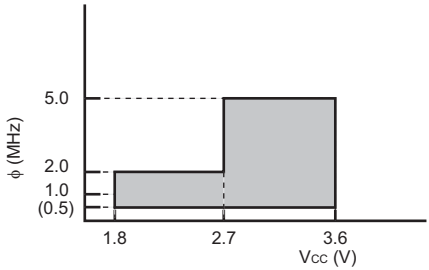
12.2.2 A/D Mode Register (AMR)

Bit	7	6	5	4	3	2	1	0
	CKS	TRGE	—	—	CH3	CH2	CH1	CH0
Initial value	0	0	1	1	0	0	0	0
Read/Write	R/W	R/W	—	—	R/W	R/W	R/W	R/W

AMR is an 8-bit read/write register for specifying the A/D conversion speed, external trigger option, and the analog input pins.

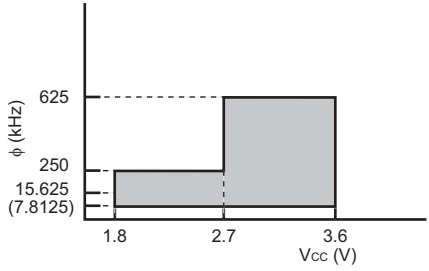
Upon reset, AMR is initialized to H'30.

Power Supply Voltage and Operating Frequency Range



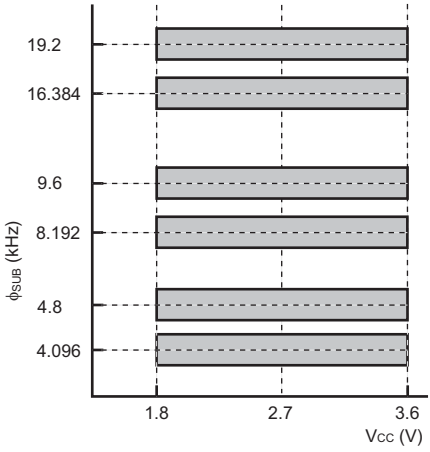
- Active (high-speed) mode
- Sleep (high-speed) mode (except CPU)

Note: 1. The figure in parentheses is the minimum operating frequency when an external clock is input. When using an oscillator, the minimum operating frequency (ϕ) is 1 MHz.



- Active (medium-speed) mode
- Sleep (medium-speed) mode (except A/D converter)

Note: 2. The figure in parentheses is the minimum operating frequency when an external clock is input. When using an oscillator, the minimum operating frequency (ϕ) is 15.625 kHz.



- Subactive mode
- Subsleep mode (except CPU)
- Watch mode (except CPU)

BRR—Bit Rate Register **H'A9** **SCI3**

Bit	7	6	5	4	3	2	1	0
	BRR7	BRR6	BRR5	BRR4	BRR3	BRR2	BRR1	BRR0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Serial transmit/receive bit rate

PMR5—Port Mode Register 5 **H'CC** **I/O Port**

Bit	7	6	5	4	3	2	1	0
	WKP_7	WKP_6	WKP_5	WKP_4	WKP_3	WKP_2	WKP_1	WKP_0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

$P5_n/\overline{WKP}_n/SEG_{n+1}$ Pin Function Switch

0	Functions as $P5_n$ I/O pin
1	Functions as $\overline{WKP}_n$ input pin

(n = 7 to 0)

PWCR2—PWM2 Control Register **H'CD** **10-Bit PWM**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	PWCR22	PWCR21	PWCR20
Initial value	1	1	1	1	1	0*2	0	0
Read/Write	—	—	—	—	—	R/W	W	W

Clock Select

0	0	The input clock is ϕ ($t\phi$*1 = 1/ϕ) The conversion period is 512/ϕ, with a minimum modulation width of 1/2ϕ
	1	The input clock is ϕ/2 ($t\phi$*1 = 2/ϕ) The conversion period is 1,024/ϕ, with a minimum modulation width of 1/ϕ
1	0	The input clock is ϕ/4 ($t\phi$*1 = 4/ϕ) The conversion period is 2,048/ϕ, with a minimum modulation width of 2/ϕ
	1	The input clock is ϕ/8 ($t\phi$*1 = 8/ϕ) The conversion period is 4,096/ϕ, with a minimum modulation width of 4/ϕ

PWH Output Select (H8/38124 Group only)

0	10-bit PWM
1	Event counter PWM

Notes: 1. $t\phi$: Period of PWM2 input clock
2. 1 on products other than the H8/38124 Group

PCR8—Port Control Register 8 **H'EB** **I/O Ports**

Bit	7	6	5	4	3	2	1	0
	$PCR8_7$	$PCR8_6$	$PCR8_5$	$PCR8_4$	$PCR8_3$	$PCR8_2$	$PCR8_1$	$PCR8_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 8 Input/Output Select

0	Input pin
1	Output pin

PMR9—Port Mode Register 9 **H'EC** **I/O Ports**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	PIOFF/—*	—	PWM2	PWM1
Initial value	1	1	1	1	0	—	0	0
Read/Write	—	—	—	—	R/W	W	R/W	R/W

P90/PWM1 Pin Function Switch

0	Functions as P90 output pin
1	Functions as PWM1 output pin

P91/PWM2 Pin Function Switch

0	Functions as P91 output pin
1	Functions as PWM2 output pin

P92 to P90 Step-up Circuit Control

0	Large-current port step-up circuit is turned on
1	Large-current port step-up circuit is turned off

Note: * Readable/writable reserved bit in the H8/38024S Group and H8/38124 Group.

IENR2—Interrupt Enable Register 2 **H'F4** **System Control**

Bit	7	6	5	4	3	2	1	0
	IENDT	IENAD	—	IENTG	IENTFH	IENTFL	IENTC	IENEC
Initial value	0	0	—	0	0	0	0	0
Read/Write	R/W	R/W	W	R/W	R/W	R/W	R/W	R/W

Asynchronous Event Counter Interrupt Enable

0	Disables asynchronous event counter interrupt requests
1	Enables asynchronous event counter interrupt requests

Timer C Interrupt Enable

0	Disables timer C interrupt requests
1	Enables timer C interrupt requests

Timer FL Interrupt Enable

0	Disables timer FL interrupt requests
1	Enables timer FL interrupt requests

Timer FH Interrupt Enable

0	Disables timer FH interrupt requests
1	Enables timer FH interrupt requests

Timer G Interrupt Enable

0	Disables timer G interrupt requests
1	Enables timer G interrupt requests

A/D Converter Interrupt Enable

0	Disables A/D converter interrupt requests
1	Enables A/D converter interrupt requests

Direct Transition Interrupt Enable

0	Disables direct transition interrupt requests
1	Enables direct transition interrupt requests

C.7 Block Diagram of Port 8

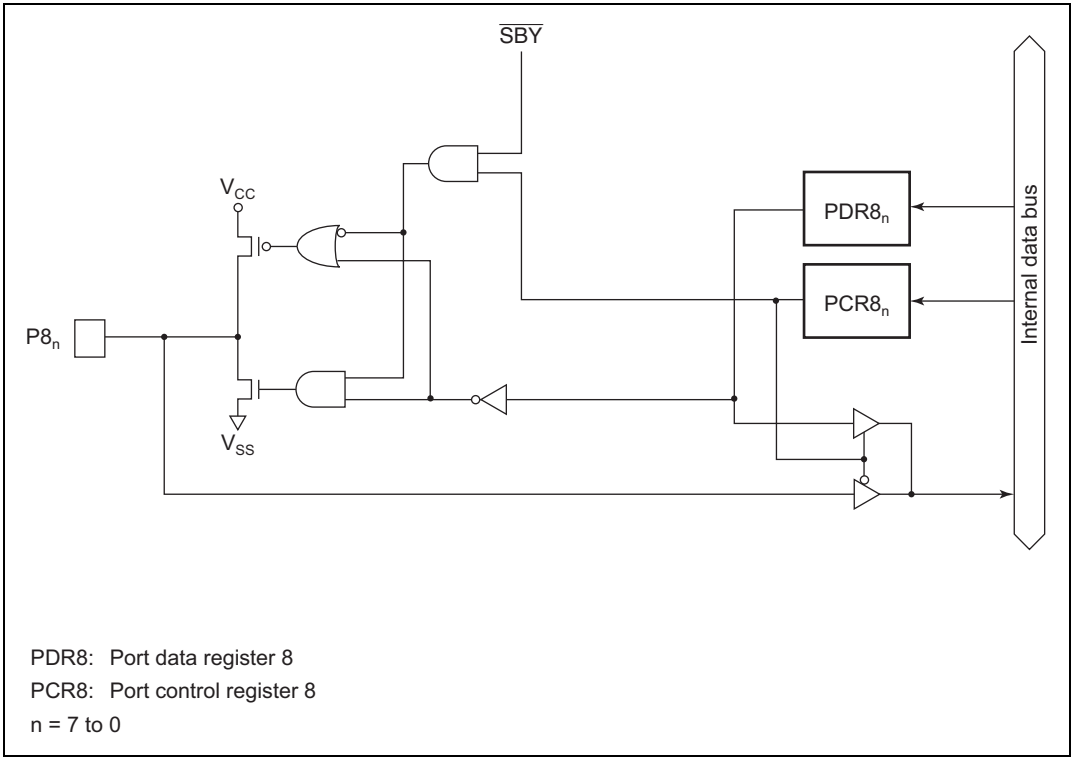


Figure C.7 Port 8 Block Diagram

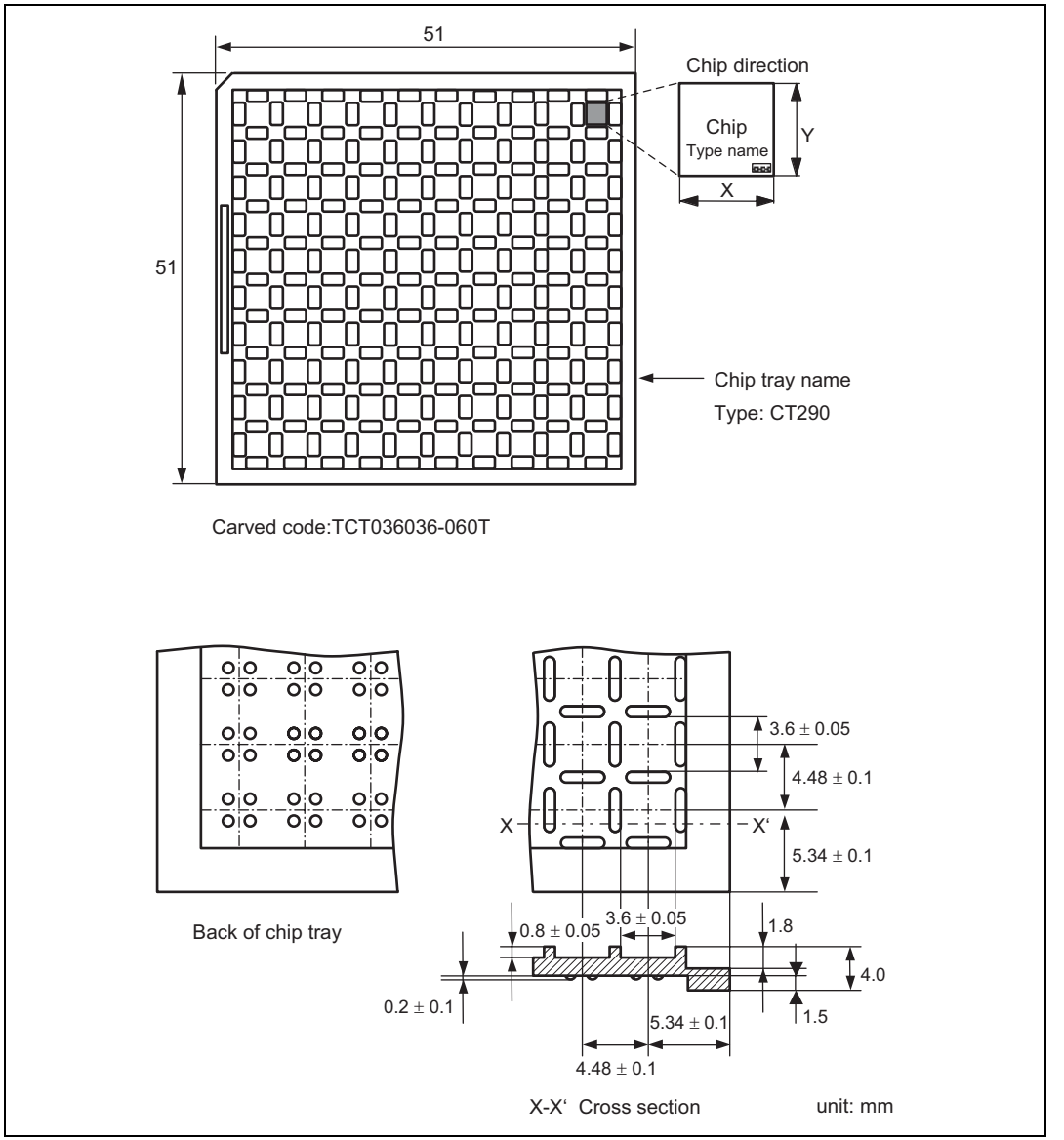


Figure I.3 Specifications of Chip Tray for the HCD64338024S, HCD64338023S, HCD64338022S, HCD64338021S, and HCD64338020S

Item	Page	Revision (See Manual for Details)
16.6.2 DC Characteristics Table 16.16 DC Characteristics	492	Table amended

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Subactive mode current dissipation	I_{SUB}	V_{CC}	—	6.2	—	µA	V_{CC} = 1.8 V, LCD on 32 kHz External Clock ($\phi_{SUB}=\phi_w/2$)	*1 *2 Reference value
			—	5.7	—	µA	V_{CC} = 1.8 V, LCD on 32 kHz crystal resonator ($\phi_{SUB}=\phi_w/2$)	
			—	4.4	—	µA	V_{CC} = 2.7 V, LCD on 32 kHz crystal resonator ($\phi_{SUB}=\phi_w/8$)	
			—	10	40	µA	V_{CC} = 2.7 V, LCD on 32 kHz External Clock ($\phi_{SUB}=\phi_w/2$)	*1 *2
			—	11	40	µA	V_{CC} = 2.7 V, LCD on 32 kHz crystal resonator ($\phi_{SUB}=\phi_w/2$)	
Subsleep mode current dissipation	I_{SUBSP}	V_{CC}	—	4.8	16.0	µA	V_{CC} = 2.7 V, LCD on 32 kHz External Clock ($\phi_{SUB}=\phi_w/2$)	*1 *2
			—	5.1	16.0	µA	V_{CC} = 2.7 V, LCD on 32 kHz crystal resonator ($\phi_{SUB}=\phi_w/2$)	
Watch mode current dissipation	I_{WATCH}	V_{CC}	—	1.2	—	µA	V_{CC} = 1.8 V, T_a = 25°C 32 kHz crystal oscillator LCD not used	*1 *2 Reference value
			—	2.0	—	µA	V_{CC} = 2.7 V, T_a = 25°C 32 kHz External Clock LCD not used	

	493	Table amended

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Watch mode current dissipation	I_{WATCH}	V_{CC}	—	2.3	—	µA	V_{CC} = 2.7 V, T_a = 25°C 32 kHz crystal resonator LCD not used	*1 *2 Reference value
			—	2.0	6.0	µA	V_{CC} = 2.7 V, 32 kHz External Clock LCD not used	*1 *2
			—	2.3	6.0	µA	V_{CC} = 2.7 V, 32 kHz crystal resonator LCD not used	