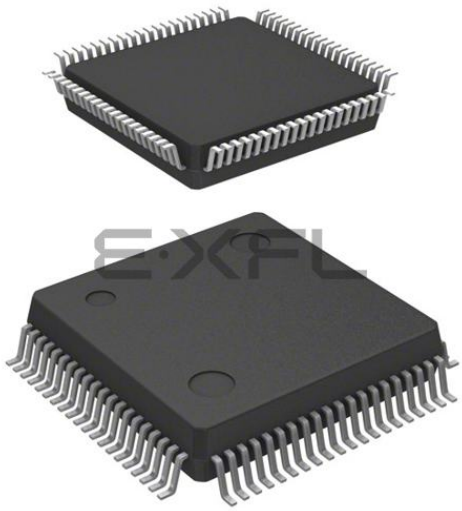

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64738024hv

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3.3 Interrupts

3.3.1 Overview

The interrupt sources include 13 external interrupts (WKP_7 to WKP_0, IRQ_4, IRQ_3, IRQ_1, IRQ_0, IRQAEC) and 9 internal interrupts from on-chip peripheral modules. Table 3.2 shows the interrupt sources, their priorities, and their vector addresses. When more than one interrupt is requested, the interrupt with the highest priority is processed.

The interrupts have the following features:

- Internal and external interrupts can be masked by the I bit in CCR. When the I bit is set to 1, interrupt request flags can be set but the interrupts are not accepted.
- IRQ_4, IRQ_3, IRQ_1, IRQ_0, and WKP_7 to WKP_0 can be set to either rising edge sensing or falling edge sensing, and IRQAEC can be set to either rising edge sensing, falling edge sensing, or both edge sensing.

Bits 1 and 0—IRQ_1 and IRQ_0 Interrupt Request Flags (IRRI1 and IRRI0)

Bit n IRRIn	Description
0	Clearing condition: (initial value) When IRRIn = 1, it is cleared by writing 0
1	Setting condition: When pin $\overline{IRQn}$ is designated for interrupt input and the designated signal edge is input

(n = 1 or 0)

Interrupt Request Register 2 (IRR2)

Bit	7	6	5	4	3	2	1	0
	IRRDT	IRRAD	—	IRRTG	IRRTFH	IRRTFL	IRRTC	IRREC
Initial value	0	0	—	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	W	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * Only a write of 0 for flag clearing is possible

IRR2 is an 8-bit read/write register, in which a corresponding flag is set to 1 when a direct transfer, A/D converter, Timer G, Timer FH, Timer FL, Timer C, or asynchronous event counter interrupt is requested. The flags are not cleared automatically when an interrupt is accepted. It is necessary to write 0 to clear each flag.

Bit 7—Direct Transfer Interrupt Request Flag (IRRDT)

Bit 7 IRRDT	Description
0	Clearing condition: (initial value) When IRRDT = 1, it is cleared by writing 0
1	Setting condition: When a direct transfer is made by executing a SLEEP instruction while DTON = 1 in SYSCR2

Wakeup Interrupt Request Register (IWPR)

Bit	7	6	5	4	3	2	1	0
	IWPF7	IWPF6	IWPF5	IWPF4	IWPF3	IWPF2	IWPF1	IWPF0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * Only a write of 0 for flag clearing is possible

IWPR is an 8-bit read/write register containing wakeup interrupt request flags. When one of pins $\overline{WKP}_7$ to $\overline{WKP}_0$ is designated for wakeup input and a rising or falling edge is input at that pin, the corresponding flag in IWPR is set to 1. A flag is not cleared automatically when the corresponding interrupt is accepted. Flags must be cleared by writing 0.

Bits 7 to 0—Wakeup Interrupt Request Flags (IWPF7 to IWPF0)

Bit n IWPFn	Description
0	Clearing condition: (initial value) When IWPFn= 1, it is cleared by writing 0
1	Setting condition: When pin $\overline{WKP}_n$ is designated for wakeup input and a rising or falling edge is input at that pin

(n = 7 to 0)

Section 5 Power-Down Modes

5.1 Overview

The LSI has nine modes of operation after a reset. These include eight power-down modes, in which power dissipation is significantly reduced. Table 5.1 gives a summary of the nine operating modes.

Table 5.1 Operating Modes

Operating Mode	Description
Active (high-speed) mode	The CPU and all on-chip peripheral functions are operable on the system clock in high-speed operation
Active (medium-speed) mode	The CPU and all on-chip peripheral functions are operable on the system clock in low-speed operation
Subactive mode	The CPU and all on-chip peripheral functions are operable on the subclock in low-speed operation
Sleep (high-speed) mode	The CPU halts. On-chip peripheral functions are operable on the system clock
Sleep (medium-speed) mode	The CPU halts. On-chip peripheral functions operate at a frequency of 1/128, 1/64, 1/32, or 1/16 of the system clock frequency
Subsleep mode	The CPU halts. The time-base function of timer A, timer C, timer F, timer G, SCI3, AEC, and LCD controller/driver are operable on the subclock
Watch mode	The CPU halts. The time-base function of timer A, timer F, timer G, AEC and LCD controller/driver are operable on the subclock
Standby mode	The CPU and all on-chip peripheral functions halt
Module standby mode	Individual on-chip peripheral functions specified by software enter standby mode and halt

Of these nine operating modes, all but the active (high-speed) mode are power-down modes. In this section the two active modes (high-speed and medium speed) will be referred to collectively as active mode.

Figure 5.1 shows the transitions among these operation modes. Table 5.2 indicates the internal states in each mode.

This section only deals with the bits related to timer G and the watchdog timer. For the functions of the bits, see the descriptions of port 3 (POF1) and port 4 (IRQ0).

Bit 2—Watchdog Timer Source Clock (WDCKS)

This bit selects the watchdog timer source clock. Note that stabilization times for the H8/38024, H8/38024S, and H8/38024R Group and for the H8/38124 Group are different.

- **H8/38024, H8/38024S, H8/38024R Group**

Bit 2 WDCKS	Description	
0	Selects ϕ/8192	(initial value)
1	Selects ϕ_W/32	

- **H8/38124 Group**

Bit 2 WDCKS	Description	
0	Selects clock based on timer mode register W (TMW) setting*	(initial value)
1	Selects ϕ_W/32	

Note: * See section 9.6, Watchdog Timer, for details.

Bit 1—TMIG Noise Canceller Select (NCS)

This bit selects controls the noise cancellation circuit of the input capture input signal (TMIG).

Bit 1 NCS	Description	
0	No noise cancellation circuit	(initial value)
1	Noise cancellation circuit	

8.6.4 Pin States

Table 8.16 shows the port 6 pin states in each operating mode.

Table 8.16 Port 6 Pin States

Pin	Reset	Sleep	Subsleep	Standby	Watch	Subactive	Active
$P6_7/SEG_{16}$ to $P6_0/SEG_9$	High-impedance	Retains previous state	Retains previous state	High-impedance*	Retains previous state	Functional	Functional

Note: * A high-level signal is output when the MOS pull-up is in the on state.

8.6.5 MOS Input Pull-Up

Port 6 has a built-in MOS pull-up function that can be controlled by software. When a PCR6 bit is cleared to 0, setting the corresponding PUCR6 bit to 1 turns on the MOS pull-up for that pin. The MOS pull-up function is in the off state after a reset.

$PCR6_n$	0	0	1
$PUCR6_n$	0	1	*
MOS input pull-up	Off	On	Off

(n = 7 to 0)

*: Don't care

8.7 Port 7

8.7.1 Overview

Port 7 is an 8-bit I/O port, configured as shown in figure 8.6.

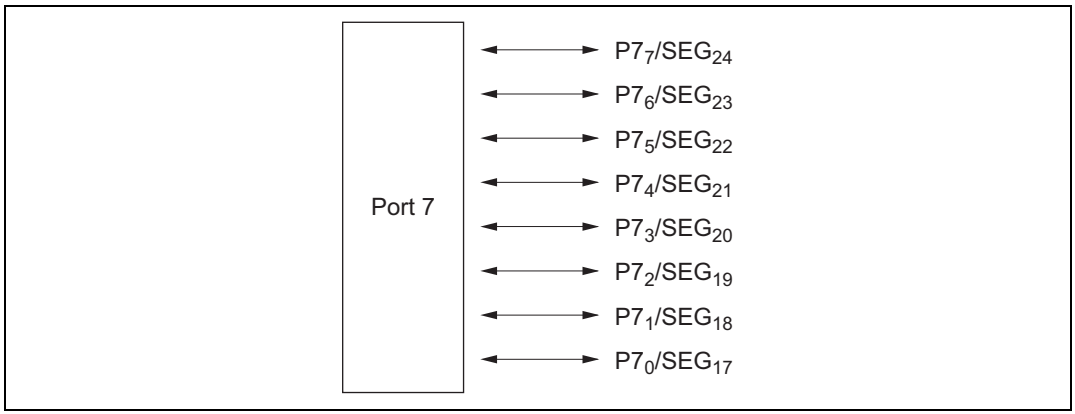


Figure 8.6 Port 7 Pin Configuration

8.7.2 Register Configuration and Description

Table 8.17 shows the port 7 register configuration.

Table 8.17 Port 7 Registers

Name	Abbr.	R/W	Initial Value	Address
Port data register 7	PDR7	R/W	H'00	H'FFDA
Port control register 7	PCR7	W	H'00	H'FFEA

Clock Stop Register 1 (CKSTPR1)

Bit:	7	6	5	4	3	2	1	0
	—	—	S32CKSTP	ADCKSTP	TGCKSTP	TFCKSTP	TCCKSTP	TACKSTP
Initial value:	1	1	1	1	1	1	1	1
Read/Write:	—	—	R/W	R/W	R/W	R/W	R/W	R/W

CKSTPR1 is an 8-bit read/write register that performs module standby mode control for peripheral modules. Only the bit relating to timer F is described here. For details of the other bits, see the sections on the relevant modules.

Bit 2—Timer F Module Standby Mode Control (TFCKSTP)

Bit 2 controls setting and clearing of module standby mode for timer F.

TFCKSTP	Description	
0	Timer F is set to module standby mode	
1	Timer F module standby mode is cleared	(initial value)

9.4.3 CPU Interface

TCF and OCRF are 16-bit read/write registers, but the CPU is connected to the on-chip peripheral modules by an 8-bit data bus. When the CPU accesses these registers, it therefore uses an 8-bit temporary register (TEMP).

When performing TCF read/write access or OCRF write access in 16-bit mode, data will not be transferred correctly if only the upper byte or only the lower byte is accessed. Access must be performed for all 16 bits (using two consecutive byte-size MOV instructions), and the upper byte must be accessed before the lower byte.

In 8-bit mode, there are no restrictions on the order of access.

Write Access

Write access to the upper byte results in transfer of the upper-byte write data to TEMP. Next, write access to the lower byte results in transfer of the data in TEMP to the upper register byte, and direct transfer of the lower-byte write data to the lower register byte.

ECH is an 8-bit read-only up-counter that operates either as an independent 8-bit event counter or as the upper 8-bit up-counter of a 16-bit event counter configured in combination with ECL. The external asynchronous event AEVH pin, $\phi/2$, $\phi/4$, $\phi/8$, or the overflow signal from lower 8-bit counter ECL can be selected as the input clock source. ECH can be cleared to H'00 by software, and is also initialized to H'00 upon reset.

Event Counter L (ECL)

Bit	7	6	5	4	3	2	1	0
	ECL7	ECL6	ECL5	ECL4	ECL3	ECL2	ECL1	ECL0
Initial Value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

ECL is an 8-bit read-only up-counter that operates either as an independent 8-bit event counter or as the lower 8-bit up-counter of a 16-bit event counter configured in combination with ECH. The event clock from the external asynchronous event AEVL pin, $\phi/2$, $\phi/4$, or $\phi/8$ is used as the input clock source. ECL can be cleared to H'00 by software, and is also initialized to H'00 upon reset.

Clock Stop Register 2 (CKSTPR2)

Bit	7	6	5	4	3	2	1	0
	LVDCKSTP*	—	—	PW2CKSTP	AECKSTP	WDCKSTP	PW1CKSTP	LDCKSTP
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	—	—	R/W	R/W	R/W	R/W	R/W

Note: * Bits 6 and 5 are also reserved on products other than the H8/38124 Group.

CKSTPR2 is an 8-bit read/write register that performs module standby mode control for peripheral modules. Only the bit relating to the asynchronous event counter is described here. For details of the other bits, see the sections on the relevant modules.

Bit 3—Asynchronous Event Counter Module Standby Mode Control (AECKSTP)

Bit 3 controls setting and clearing of module standby mode for the asynchronous event counter.

AECKSTP	Description	
0	Asynchronous event counter is set to module standby mode	
1	Asynchronous event counter module standby mode is cleared	(initial value)

Table 10.6 shows examples of BRR settings in synchronous mode. The values shown are for active (high-speed) mode.

Table 10.6 Examples of BRR Settings for Various Bit Rates (Synchronous Mode) (1)

Bit Rate (bit/s)	φ								
	19.2 kHz			1 MHz			2 MHz		
	n	N	Error	n	N	Error	n	N	Error
200	0	23	0	—	—	—	—	—	—
250	—	—	—	—	—	—	2	124	0
300	2	0	0	—	—	—	—	—	—
500				—	—	—	—	—	—
1K				0	249	0	—	—	—
2.5K				0	99	0	0	199	0
5K				0	49	0	0	99	0
10K				0	24	0	0	49	0
25K				0	9	0	0	19	0
50K				0	4	0	0	9	0
100K				—	—	—	0	4	0
250K				0	0	0	0	1	0
500K							0	0	0
1M									

Table 10.6 Examples of BRR Settings for Various Bit Rates (Synchronous Mode) (2)

Bit Rate (bit/s)	φ								
	5 MHz			8 MHz			10 MHz		
	n	N	Error	n	N	Error	n	N	Error
200	—	—	—	—	—	—	0	12499	0
250	—	—	—	3	124	0	2	624	0
300	—	—	—	—	—	—	0	8332	0
500	—	—	—	2	249	0	0	4999	0
1K	—	—	—	2	124	0	0	2499	0
2.5K	—	—	—	2	49	0	0	999	0
5K	0	249	0	2	24	0	0	499	0
10K	0	124	0	0	199	0	0	249	0
25K	0	49	0	0	79	0	0	99	0
50K	0	24	0	0	39	0	0	49	0
100K	—	—	—	0	19	0	0	24	0
250K	0	4	0	0	7	0	0	9	0
500K	—	—	—	0	3	0	0	4	0
1M	—	—	—	0	1	0	—	—	—

Blank: Cannot be set.

— : A setting can be made, but an error will result.

Notes: The value set in BRR is given by the following equation:

$$N = \frac{\phi}{(4 \times 2^{2n} \times B)} - 1$$

where B: Bit rate (bit/s)
N: Baud rate generator BRR setting ($0 \leq N \leq 255$)
φ: System clock frequency
n: Baud rate generator input clock number (n = 0, 2, or 3)
(The relation between n and the clock is shown in table 10.7.)

Table 10.11 shows the 16 data transfer formats that can be set in asynchronous mode. The format is selected by the settings in the serial mode register (SMR).

Table 10.11 Data Transfer Formats (Asynchronous Mode)

SMR				Serial Data Transfer Format and Frame Length
CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12
0	0	0	0	S 8-bit data STOP
0	0	0	1	S 8-bit data STOP STOP
0	0	1	0	Setting prohibited
0	0	1	1	Setting prohibited
0	1	0	0	S 8-bit data P STOP
0	1	0	1	S 8-bit data P STOP STOP
0	1	1	0	S 5-bit data STOP
0	1	1	1	S 5-bit data STOP STOP
1	0	0	0	S 7-bit data STOP
1	0	0	1	S 7-bit data STOP STOP
1	0	1	0	Setting prohibited
1	0	1	1	Setting prohibited
1	1	0	0	S 7-bit data P STOP
1	1	0	1	S 7-bit data P STOP STOP
1	1	1	0	S 5-bit data P STOP
1	1	1	1	S 5-bit data P STOP STOP

[Legend]
S: Start bit
STOP: Stop bit
P: Parity bit
MPB: Multiprocessor bit

Figure 10.5 shows an example of a flowchart for initializing SCI3.

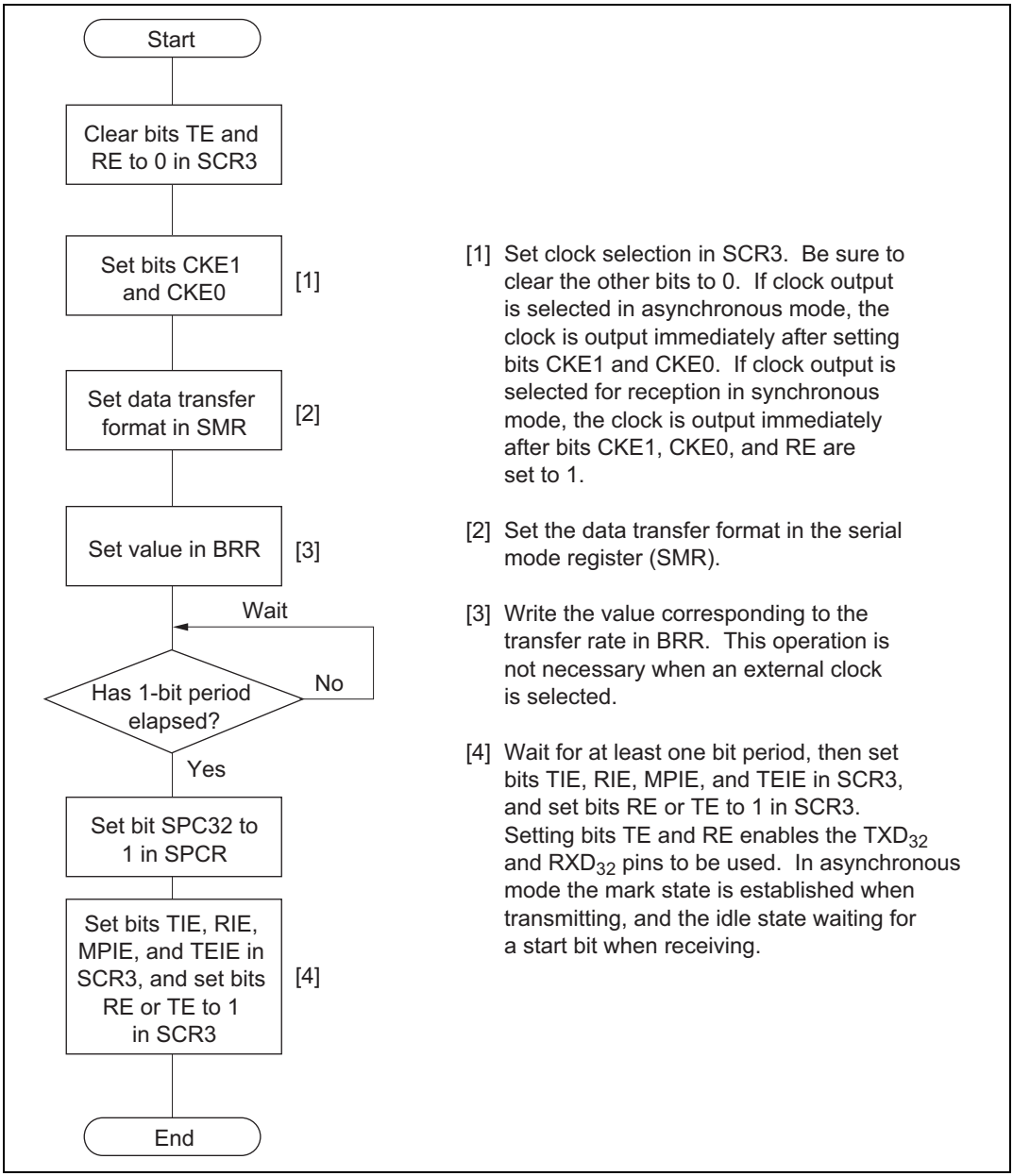
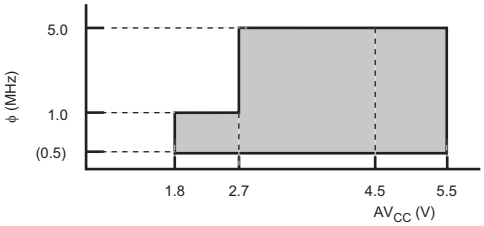
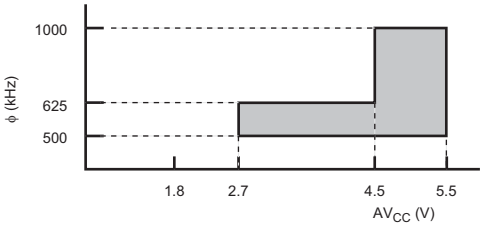


Figure 10.5 Example of SCI3 Initialization Flowchart

Analog Power Supply Voltage and A/D Converter Operating Range



- Active (high-speed) mode
- Sleep (high-speed) mode



- Active (medium-speed) mode
- Sleep (medium-speed) mode

Note: 3. When AVCC = 1.8 V to 2.7 V, the operating range is limited to ϕ = 1.0 MHz when using an oscillator, and is ϕ = 0.5 MHz to 1.0 MHz when using an external clock.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Output low voltage	V_{OL}	$P1_3$, $P1_4$, $P1_6$, $P1_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_2$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, PA_0 to PA_3	—	—	0.5	V	I_{OL} = 0.4 mA	
		$P9_0$ to $P9_2$	—	—	0.5	V	I_{OL} = 25 mA	*1
							I_{OL} = 10 mA	*2
		$P9_3$ to $P9_5$	—	—	0.5	V	I_{OL} = 10 mA	
Input/output leakage current	$\lvert I_{IL} \rvert$	$\overline{RES}$, $P4_3$, OSC_1, X_1, $P1_3$, $P1_4$, $P1_6$, $P1_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_2$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, IRQAEC, $P9_0$ to $P9_5$, PA_0 to PA_3	—	—	1.0	µA	V_{IN} = 0.5 V to V_{CC} – 0.5 V	
		PB_0 to PB_7	—	—	1.0	µA	V_{IN} = 0.5 V to AV_{CC} – 0.5 V	
Pull-up MOS current	$-I_p$	$P1_3$, $P1_4$, $P1_6$, $P1_7$, $P3_0$ to $P3_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$	30	—	180	µA	V_{CC} = 3 V, V_{IN} = 0 V	
Input capacitance	C_{IN}	All input pins except power supply and IRQAEC	—	—	15.0	pF	f = 1 MHz, V_{IN} =0 V, T_a = 25°C	
		IRQAEC	—	—	30.0	pF		

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Allowable output high current (per pin)	$-I_{OH}$	All output pins	—	—	0.2	mA		
Allowable output high current (total)	$\sum -I_{OH}$	All output pins	—	—	10.0	mA		

Notes: Connect the TEST pin to V_{SS}.

1. Applied when the PIOFF bit in the port mode register 9 is 0.
2. Applied when the PIOFF bit in the port mode register 9 is 1.
3. Pin states during current measurement.

Mode	$\overline{RES}$ Pin	Internal State	Other Pins	LCD Power Supply	Oscillator Pins
Active (high-speed) mode (I_{OPE1})	V_{CC}	Operates	V_{CC}	Halted	System clock oscillator: crystal
Active (medium-speed) mode (I_{OPE2})					Subclock oscillator: Pin X_1 = GND
Sleep mode	V_{CC}	Only on-chip timers operate	V_{CC}	Halted	
Subactive mode	V_{CC}	Operates	V_{CC}	Halted	System clock oscillator: crystal
Subsleep mode	V_{CC}	Only on-chip timers operate, CPU stops	V_{CC}	Halted	Subclock oscillator: crystal
Watch mode	V_{CC}	Only time base operates, CPU stops	V_{CC}	Halted	
Standby mode	V_{CC}	CPU and timers both stop	V_{CC}	Halted	System clock oscillator: crystal
					Subclock oscillator: Pin X_1 = GND

4. Excludes current in pull-up MOS transistors and output buffers.
5. Used for the judgment of user mode or boot mode when the reset is released.

PMR2—Port Mode Register 2 **H'C9** **I/O Port**

Bit	7	6	5	4	3	2	1	0
	—	—	POF1	—	—	WDCKS	NCS	IRQ0
Initial value	1	1	0	1	1	0	0	0
Read/Write	—	—	R/W	—	—	R/W	R/W	R/W

$P4_3/\overline{IRQ0}$ Pin Function Switch

0	Functions as $P4_3$ I/O pin
1	Functions as $\overline{IRQ}_0$ input pin

TMIG Noise Canceller Select

0	Noise cancellation function not used
1	Noise cancellation function used

Watchdog Timer Switch

0	Selects ϕ8192*
1	Selects ϕ_W/32

$P3_5$ Pin Output Buffer PMOS On/Off Control

0	CMOS output
1	NMOS open-drain output

Note: * On the H8/38124 Group the clock source can be selected using the TMW register.

Appendix H Form of Bonding Pads

The form of the bonding pads for the HCD64338024, HCD64338023, HCD64338022, HCD64338021, HCD64338020, HCD64F38024, HCD64F38024R, HCD64338024S, HCD64338023S, HCD64338022S, HCD64338021S, and HCD64338020S is shown in figure H.1.

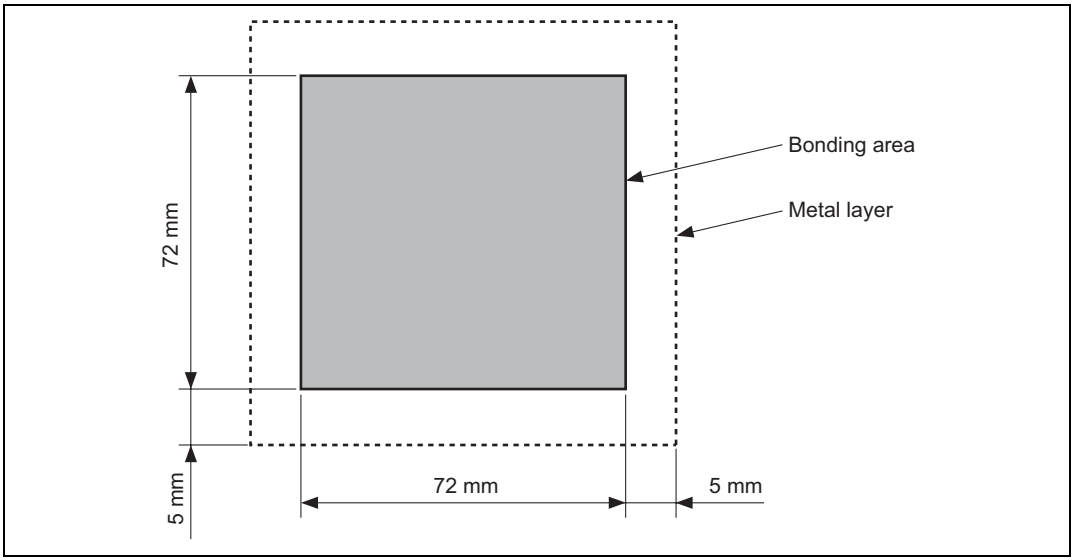


Figure H.1 Bonding Pad Form

Item	Page	Revision (See Manual for Details)
16.8.2 DC Characteristics Table 16.22 DC Characteristics	506	Table amended

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{WKP_0}$ to $\overline{WKP_7}$, $\overline{IRQ_0}$, $\overline{IRQ_3}$, $\overline{IRQ_4}$, AEVL, AEVH, TMIC, TMIF, TMIG, ADTRG, SCK_{32}	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	V	V_{CC} = 4.0 V to 5.5 V	
			$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$		Other than above	
		$\overline{IRQ_1}$	$V_{CC} \times 0.8$	—	$AV_{CC} + 0.3$	V	V_{CC} = 4.0 V to 5.5 V	
			$V_{CC} \times 0.9$	—	$AV_{CC} + 0.3$		Other than above	

16.8.10 Power Supply Characteristics	525	Newly added

B.1 Addresses	548	Table amended

Lower Address	Register Name	Bit Names Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
H'AA	SCR3	TIE	RIE	TE	RE	—	TEIE	CKE1	CKE0	SCI3
H'AC	SSR	TDRE	RDRF	OER	FER	PER	TEND	—	—	

B.2 Functions	564	Figure amended

SMR—Serial Mode Register H'A8 SCI3

Bit	7	6	5	4	3	2	1	0
	COM	CHR	PE	PM	STOP	MP	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	ϕ clock
0	1	ϕ_W/2 clock
1	0	ϕ/16 clock
1	1	ϕ/64 clock

5 Bit Communication

0	5 bits communication disabled
1	5 bits communication enabled