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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64738024wiv

Target Readers: This manual is designed for use by people who design application systems using the H8/38024 Group, H8/38024S Group, H8/38024R Group, and H8/38124 Group.
To use this manual, basic knowledge of electric circuits, logic circuits and microcomputers is required.

Purpose: This manual provides the information of the hardware functions and electrical characteristics of the H8/38024 Group, H8/38024S Group, H8/38024R Group, and H8/38124 Group. The H8/300L Series Software Manual contains detailed information of executable instructions. Please read the Software Manual together with this manual.

How to Use the Book:

- To understand general functions
  → Read the manual from the beginning.
  The manual explains the CPU, system control functions, peripheral functions and electrical characteristics in that order.
- To understanding CPU functions
  → Refer to the separate H8/300L Series Software Manual.

Explanatory Note: Bit sequence: upper bit at left, and lower bit at right

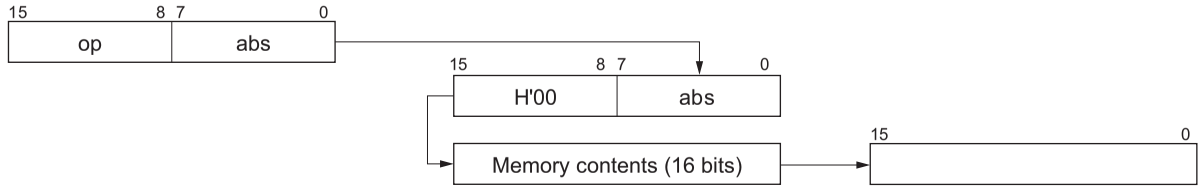
List of Related Documents: The latest documents are available on our Web site. Please make sure that you have the latest version.
(http://www.renesas.com/)

- User Manual for H8/38024 Group, H8/38024S Group, H8/38024R Group, and H8/38124 Group

Name of Document	Document No.
H8/38024 Group, H8/38024S Group, H8/38024R Group, H8/38124 Group Hardware Manual	This manual
H8/300L Series Software Manual	REJ09B0214

- User's Manual for Development Tools

Name of Document	Document No.
H8S, H8/300 Series, C/C++ Compiler, Assembler, Optimizing Linkage Editor User's Manual	REJ10B2039
H8S, H8/300 Series Simulator/Debugger User's Manual	REJ10B0211
High-Performance Embedded Workshop User's Manual	REJ10J2037

No.	Addressing Mode and Instruction Format	Effective Address Calculation Method	Effective Address (EA)
8	Memory indirect, @@aa:8		

[Legend]
rm, rn: Register field
op: Operation field
disp: Displacement
IMM: Immediate data
abs: Absolute address

Instruction	Size*	Function
BXOR	B	C ⊕ (<bit-No.> of <EAd>) → C XORs the C flag with a specified bit in a general register or memory, and stores the result in the C flag.
BIXOR	B	C ⊕ [~(<bit-No.> of <EAd>)] → C XORs the C flag with the inverse of a specified bit in a general register or memory, and stores the result in the C flag. The bit number is specified by 3-bit immediate data.
BLD	B	(<bit-No.> of <EAd>) → C Copies a specified bit in a general register or memory to the C flag.
BILD	B	~ (<bit-No.> of <EAd>) → C Copies the inverse of a specified bit in a general register or memory to the C flag. The bit number is specified by 3-bit immediate data.
BST	B	C → (<bit-No.> of <EAd>) Copies the C flag to a specified bit in a general register or memory.
BIST	B	~ C → (<bit-No.> of <EAd>) Copies the inverse of the C flag to a specified bit in a general register or memory. The bit number is specified by 3-bit immediate data.

Note: * Size: Operand size
B: Byte

Certain precautions are required in bit manipulation. See section 2.9.2, Notes on Bit Manipulation, for details.

Figure 2.7 lists the format of the bit manipulation instructions.

Bit 6—Software Write Enable (SWE)

This bit is to set enabling/disabling of programming/enabling of flash memory (set when bits 5 to 0 and the EBR register are to be set).

Bit 6 SWE	Description
0	Programming/erasing is disabled. Other FLMCR1 register bits and all EBR bits cannot be set. (initial value)
1	Flash memory programming/erasing is enabled.

Bit 5—Erase Setup (ESU)

This bit is to prepare for changing to erase mode. Set this bit to 1 before setting the E bit to 1 in FLMCR1 (do not set SWE, PSU, EV, PV, E, and P bits at the same time).

Bit 5 ESU	Description
0	The erase setup state is cancelled (initial value)
1	The flash memory changes to the erase setup state. Set this bit to 1 before setting the E bit to 1 in FLMCR1.

Bit 4—Program Setup (PSU)

This bit is to prepare for changing to program mode. Set this bit to 1 before setting the P bit to 1 in FLMCR1 (do not set SWE, ESU, EV, PV, E, and P bits at the same time).

Bit 4 PSU	Description
0	The program setup state is cancelled (initial value)
1	The flash memory changes to the program setup state. Set this bit to 1 before setting the P bit to 1 in FLMCR1.

Bit 3—Erase-Verify (EV)

This bit is to set changing to or cancelling erase-verify mode (do not set SWE, ESU, PSU, PV, E, and P bits at the same time).

8.4.4 Pin States

Table 8.10 shows the port 4 pin states in each operating mode.

Table 8.10 Port 4 Pin States

Pins	Reset	Sleep	Subsleep	Standby	Watch	Subactive	Active
$P4_3/\overline{IRQ_0}$ $P4_2/TXD_{32}$ $P4_1/RXD_{32}$ $P4_0/SCK_{32}$	High-impedance	Retains previous state	Retains previous state	High-impedance	Retains previous state	Functional	Functional

Bit 3—TXD_{32} Pin Output Data Inversion Switch

Bit 3 specifies whether or not TXD_{32} pin output data is to be inverted.

Bit 3 SCINV3	Description	
0	TXD_{32} output data is not inverted	(initial value)
1	TXD_{32} output data is inverted	

Bit 2—RXD_{32} Pin Input Data Inversion Switch

Bit 2 specifies whether or not RXD_{32} pin input data is to be inverted.

Bit 2 SCINV2	Description	
0	RXD_{32} input data is not inverted	(initial value)
1	RXD_{32} input data is inverted	

Bits 1 and 0—Reserved

Bits 1 and 0 are reserved; they can only be written with 0.

8.12.3 Note on Modification of Serial Port Control Register

When a serial port control register is modified, the data being input or output up to that point is inverted immediately after the modification, and an invalid data change is input or output. When modifying a serial port control register, do so in a state in which data changes are invalidated.

Bits 1 and 0—Clock Enable 1 and 0 (CKE1, CKE0)

Bits 1 and 0 select the clock source and enabling or disabling of clock output from the SCK_{32} pin. The combination of CKE1 and CKE0 determines whether the SCK_{32} pin functions as an I/O port, a clock output pin, or a clock input pin.

The CKE0 bit setting is only valid in case of internal clock operation (CKE1 = 0) in asynchronous mode. In synchronous mode, or when external clock operation is used (CKE1 = 1), bit CKE0 should be cleared to 0.

After setting bits CKE1 and CKE0, set the operating mode in the serial mode register (SMR).

For details on clock source selection, see table 10.9.

Bit 1 CKE1	Bit 0 CKE0	Description		
		Communication Mode	**Clock Source**	**SCK_{32} Pin Function**
0	0	Asynchronous	Internal clock	I/O port*1
		Synchronous	Internal clock	Serial clock output*1
0	1	Asynchronous	Internal clock	Clock output*2
		Synchronous	Reserved	
1	0	Asynchronous	External clock	Clock input*3
		Synchronous	External clock	Serial clock input
1	1	Asynchronous	Reserved	
		Synchronous	Reserved	

Notes: 1. Initial value
2. A clock with the same frequency as the bit rate is output.
3. Input a clock with a frequency 16 times the bit rate.

SCI3 operates as follows when transmitting data.

SCI3 monitors bit TDRE in SSR, and when it is cleared to 0, recognizes that data has been written to TDR and transfers data from TDR to TSR. It then sets bit TDRE to 1 and starts transmitting. If bit TIE in SCR3 is set to 1 at this time, a TXI request is made.

Serial data is transmitted from the TXD_{32} pin using the relevant data transfer format in table 10.11. When the stop bit is sent, SCI3 checks bit TDRE. If bit TDRE is cleared to 0, SCI3 transfers data from TDR to TSR, and when the stop bit has been sent, starts transmission of the next frame. If bit TDRE is set to 1, bit TEND in SSR bit is set to 1the mark state, in which 1s are transmitted, is established after the stop bit has been sent. If bit TEIE in SCR3 is set to 1 at this time, a TEI request is made.

Figure 10.7 shows an example of the operation when transmitting in asynchronous mode.

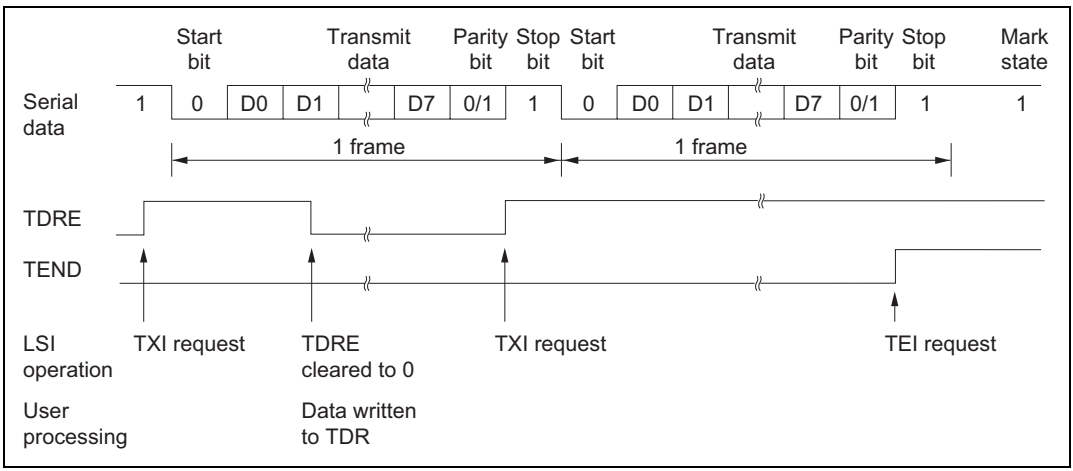


Figure 10.7 Example of Operation when Transmitting in Asynchronous Mode (8-bit data, parity, 1 stop bit)

Bit 4—Display Data Control (DISP)

Bit 4 specifies whether the LCD RAM contents are displayed or blank data is displayed regardless of the LCD RAM contents.

Bit 4 DISP	Description	
0	Blank data is displayed	(initial value)
1	LCD RAM data is display	

Bits 3 to 0—Frame Frequency Select 3 to 0 (CKS3 to CKS0)

Bits 3 to 0 select the operating clock and the frame frequency. In subactive mode, watch mode, and subsleep mode, the system clock (ϕ) is halted, and therefore display operations are not performed if one of the clocks from ϕ/2 to ϕ/256 is selected. If LCD display is required in these modes, ϕw, ϕw/2, or ϕw/4 must be selected as the operating clock.

Bit 3 CKS3	Bit 2 CKS2	Bit 1 CKS1	Bit 0 CKS0	Operating Clock	Frame Frequency*2 ϕ = 2 MHz	Frame Frequency*2 ϕ = 250 kHz*1
0	*	0	0	ϕw	128 Hz*3 (initial value)	
0	*	0	1	ϕw/2	64 Hz*3	
0	*	1	*	ϕw/4	32 Hz*3	
1	0	0	0	ϕ/2	—	244 Hz
1	0	0	1	ϕ/4	977 Hz	122 Hz
1	0	1	0	ϕ/8	488 Hz	61 Hz
1	0	1	1	ϕ/16	244 Hz	30.5 Hz
1	1	0	0	ϕ/32	122 Hz	—
1	1	0	1	ϕ/64	61 Hz	—
1	1	1	0	ϕ/128	30.5 Hz	—
1	1	1	1	ϕ/256	—	—

*: Don't care

Notes: 1. This is the frame frequency in active (medium-speed, ϕosc/16) mode when ϕ = 2 MHz.
2. When 1/3 duty is selected, the frame frequency is 4/3 times the value shown.
3. This is the frame frequency when ϕw = 32.768 kHz.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Allowable output high current (total)	$\sum -I_{OH}$	All output pins	—	—	15.0	mA	V_{CC} = 4.0 V to 5.5 V	
			—	—	10.0		Except the above	

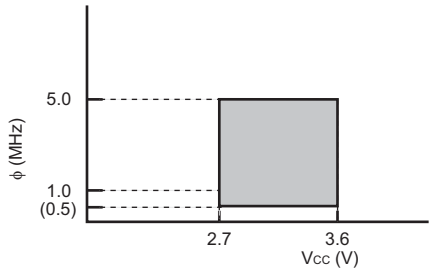
Notes: Connect the TEST pin to V_{SS}.

1. Applies to the Mask ROM products.
2. Applies to the HD64738024.
3. Pin states during current measurement.

Mode	$\overline{RES}$ Pin	Internal State	Other Pins	LCD Power Supply	Oscillator Pins
Active (high-speed) mode (I_{OPE1})	V_{CC}	Operates	V_{CC}	Halted	System clock oscillator: crystal
Active (medium-speed) mode (I_{OPE2})					Subclock oscillator: Pin X_1 = GND
Sleep mode	V_{CC}	Only timers operate	V_{CC}	Halted	
Subactive mode	V_{CC}	Operates	V_{CC}	Halted	System clock oscillator: crystal
Subsleep mode	V_{CC}	Only timers operate, CPU stops	V_{CC}	Halted	Subclock oscillator: crystal
Watch mode	V_{CC}	Only time base operates, CPU stops	V_{CC}	Halted	
Standby mode	V_{CC}	CPU and timers both stop	V_{CC}	Halted	System clock oscillator: crystal
					Subclock oscillator: Pin X_1 = GND

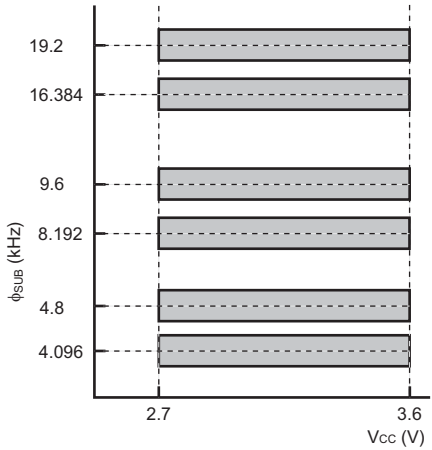
4. Excludes current in pull-up MOS transistors and output buffers.
5. When the PIOFF bit in the port mode register 9 is 0.
6. When the PIOFF bit in the port mode register 9 is 1.

Power Supply Voltage and Operating Frequency Range

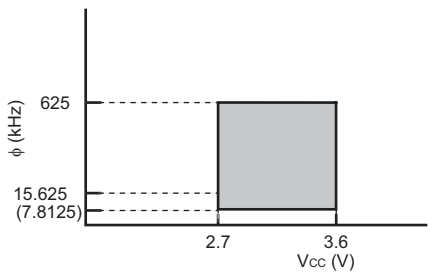


- Active (high-speed) mode
- Sleep (high-speed) mode (except CPU)

Note: 1. The figure in parentheses is the minimum operating frequency when an external clock is input. When using an oscillator, the minimum operating frequency (ϕ) is 1 MHz.



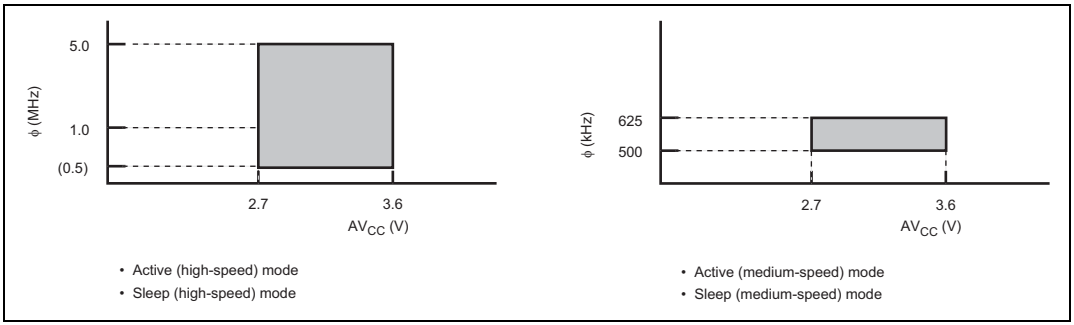
- Subactive mode
- Subsleep mode (except CPU)
- Watch mode (except CPU)



- Active (medium-speed) mode
- Sleep (medium-speed) mode (except A/D converter)

Note: 2. The figure in parentheses is the minimum operating frequency when an external clock is input. When using an oscillator, the minimum operating frequency (ϕ) is 15.625 kHz.

Analog Power Supply Voltage and A/D Converter Operating Range



Appendix A CPU Instruction Set

A.1 Instructions

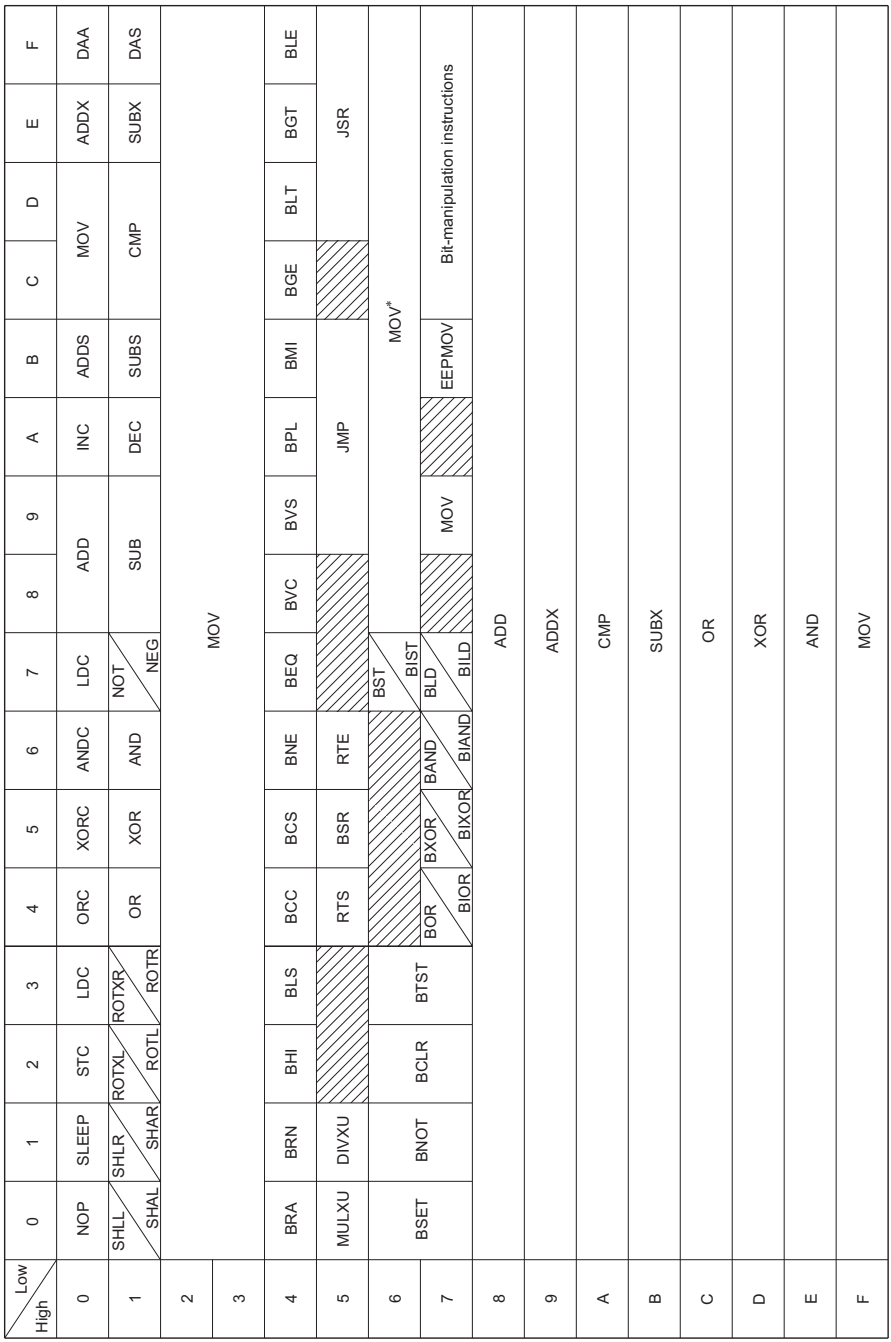
Operation Notation

Rd8/16	General register (destination) (8 or 16 bits)
Rs8/16	General register (source) (8 or 16 bits)
Rn8/16	General register (8 or 16 bits)
CCR	Condition code register
N	N (negative) flag in CCR
Z	Z (zero) flag in CCR
V	V (overflow) flag in CCR
C	C (carry) flag in CCR
PC	Program counter
SP	Stack pointer
#xx: 3/8/16	Immediate data (3, 8, or 16 bits)
d: 8/16	Displacement (8 or 16 bits)
@aa: 8/16	Absolute address (8 or 16 bits)
+	Addition
–	Subtraction
×	Multiplication
÷	Division
∧	Logical AND
∨	Logical OR
⊕	Exclusive logical OR
→	Move
¬	Logical complement

Condition Code Notation

Symbol	
↕	Modified according to the instruction result
*	Not fixed (value not guaranteed)
0	Always cleared to 0
—	Not affected by the instruction execution result

Table A.2 Operation Code Map



Note: * The PUSH and POP instructions are identical in machine language to MOV instructions.

Table A.4 Number of Cycles in Each Instruction

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
ADD	ADD.B #xx:8, Rd	1					
	ADD.B Rs, Rd	1					
	ADD.W Rs, Rd	1					
ADDS	ADDS.W #1, Rd	1					
	ADDS.W #2, Rd	1					
ADDX	ADDX.B #xx:8, Rd	1					
	ADDX.B Rs, Rd	1					
AND	AND.B #xx:8, Rd	1					
	AND.B Rs, Rd	1					
ANDC	ANDC #xx:8, CCR	1					
BAND	BAND #xx:3, Rd	1					
	BAND #xx:3, @Rd	2			1		
	BAND #xx:3, @aa:8	2			1		
Bcc	BRA d:8 (BT d:8)	2					
	BRN d:8 (BF d:8)	2					
	BHI d:8	2					
	BLS d:8	2					
	BCC d:8 (BHS d:8)	2					
	BCS d:8 (BLO d:8)	2					
	BNE d:8	2					
	BEQ d:8	2					
	BVC d:8	2					
	BVS d:8	2					
	BPL d:8	2					
	BMI d:8	2					
	BGE d:8	2					
	BLT d:8	2					
	BGT d:8	2					
	BLE d:8	2					
BCLR	BCLR #xx:3, Rd	1					
	BCLR #xx:3, @Rd	2			2		
	BCLR #xx:3, @aa:8	2			2		
	BCLR Rn, Rd	1					
	BCLR Rn, @Rd	2			2		
	BCLR Rn, @aa:8	2			2		
BIAND	BIAND #xx:3, Rd	1					
	BIAND #xx:3, @Rd	2			1		
	BIAND #xx:3, @aa:8	2			1		

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
MOV	MOV.W Rs, @Rd	1				1	
	MOV.W Rs, @(d:16, Rd)	2				1	
	MOV.W Rs, @–Rd	1				1	2
	MOV.W Rs, @aa:16	2				1	
MULXU	MULXU.B Rs, Rd	1					12
NEG	NEG.B Rd	1					
NOP	NOP	1					
NOT	NOT.B Rd	1					
OR	OR.B #xx:8, Rd	1					
	OR.B Rs, Rd	1					
ORC	ORC #xx:8, CCR	1					
ROTL	ROTL.B Rd	1					
ROTR	ROTR.B Rd	1					
ROTXL	ROTXL.B Rd	1					
ROTXR	ROTXR.B Rd	1					
RTE	RTE	2		2			2
RTS	RTS	2		1			2
SHAL	SHAL.B Rd	1					
SHAR	SHAR.B Rd	1					
SHLL	SHLL.B Rd	1					
SHLR	SHLR.B Rd	1					
SLEEP	SLEEP	1					
STC	STC CCR, Rd	1					
SUB	SUB.B Rs, Rd	1					
	SUB.W Rs, Rd	1					
SUBS	SUBS.W #1, Rd	1					
	SUBS.W #2, Rd	1					
POP	POP Rd	1		1			2
PUSH	PUSH Rs	1		1			2
SUBX	SUBX.B #xx:8, Rd	1					
	SUBX.B Rs, Rd	1					
XOR	XOR.B #xx:8, Rd	1					
	XOR.B Rs, Rd	1					
XORC	XORC #xx:8, CCR	1					

FLMCR1—Flash Memory Control Register 1 **H'F020** **Flash Memory**

Bit	7	6	5	4	3	2	1	0
	—	SWE	ESU	PSU	EV	PV	E	P
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Program

0	Program mode cleared (initial value)
1	Transition to program mode [Setting condition] When SWE = 1 and PSU = 1

Erase

0	Erase mode cleared (initial value)
1	Transition to erase mode [Setting condition] When SWE = 1 and ESU = 1

Program-Verify

0	Program-verify mode cleared (initial value)
1	Transition to program-verify mode [Setting condition] When SWE = 1

Erase-Verify

0	Erase-verify mode cleared (initial value)
1	Transition to erase-verify mode [Setting condition] When SWE = 1

Program-Setup

0	Program-setup cleared (initial value)
1	Program setup [Setting condition] When SWE = 1

Erase-Setup

0	Erase-setup cleared (initial value)
1	Erase setup [Setting condition] When SWE = 1

Software write enable bit

0	Writing/erasing disabled (initial value)
1	Writing/erasing enabled

LVDCR—Low-Voltage Detection Control Register H'86 LVDC

Note: This register is implemented on the H8/38124 Group only.

Bit	7	6	5	4	3	2	1	0
	LVDE	—	VINTDSEL	VINTUSEL	LVDSEL	LVDRE	LVDDE	LVDUE
Initial value	0*	0	0	0	0*	0*	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Voltage Rise Interrupt Enable

0	Voltage rise interrupt requests disabled (initial value)
1	Voltage rise interrupt requests enabled

Voltage Drop Interrupt Enable

0	Voltage drop interrupt requests disabled (initial value)
1	Voltage drop interrupt requests enabled

LVDR Enable

0	LVDR resets disabled	(initial value)
1	LVDR resets enabled	

LVDR Detection Level Select

0	Reset detection voltage 2.3 V (typ.)	(initial value)
1	Reset detection voltage 3.3 V (typ.)	

Power Supply Rise (LVDU) Detection Level External Input Select

0	LVDU detection level generated by on-chip ladder resistor (initial value)
1	LVDU detection level input to extU pin

Power Supply Drop (LVDD) Detection Level External Input Select

0	LVDD detection level generated by on-chip ladder resistor (initial value)
1	LVDD detection level input to extD pin

LVD Enable

0	Low-voltage detection circuit not used (standby status) (initial value)
1	Low-voltage detection circuit use

Note: * These bits are not initialized by resets trigged by LVDR. They are initialized by power-on resets and watchdog timer resets.

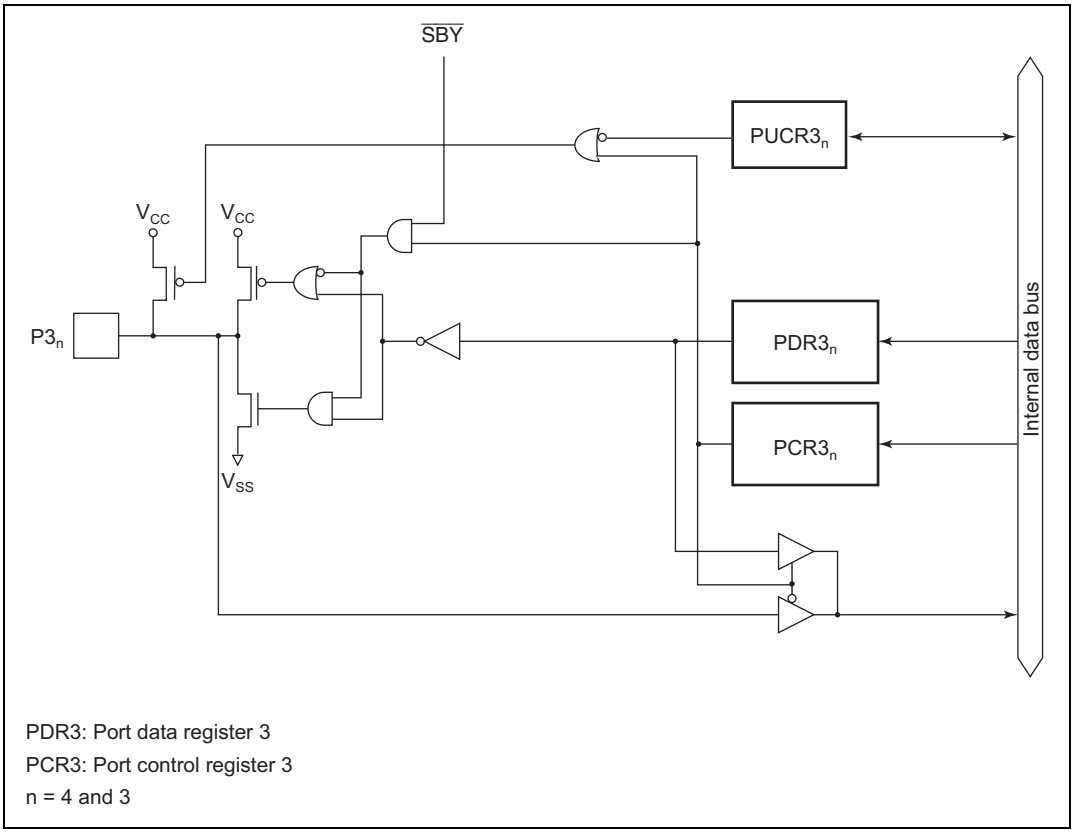


Figure C.2(c) Port 3 Block Diagram (Pins $P3_4$ and $P3_3$)

Item	Page	Revision (See Manual for Details)
Appendix F Package Dimensions	642	Figure replaced
Figure F.4 TLP-85V Package Dimensions		
Appendix I Specifications of Chip Tray	648	Figure replaced
Figure I.3 Specifications of Chip Tray for the HCD64338024S, HCD64338023S, HCD64338022S, HCD64338021S, and HCD64338020S		