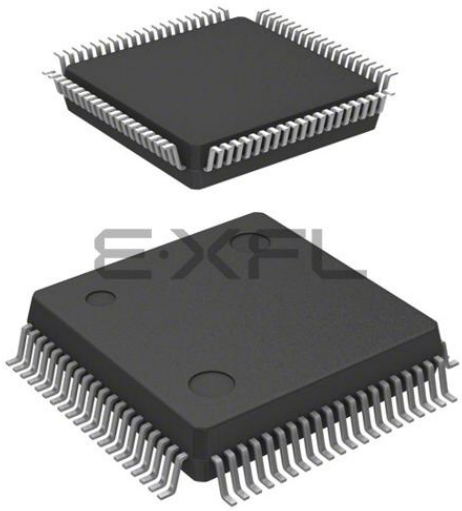

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	5MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f38024rdv

User's Manual

8

The revision list can be viewed directly by clicking the title page.
The revision list summarizes the locations of revisions and additions.
Details should always be checked by referring to the relevant text.

H8/38024, H8/38024S, H8/38024R, H8/38124 Group

Hardware Manual
Renesas 8-Bit Single-Chip Microcomputer
H8 Family/H8/300L Super Low Power Series

H8/38024 Group	H8/38024	H8/38024R Group	H8/38024R
	H8/38023		
	H8/38022	H8/38124 Group	H8/38124
	H8/38021		H8/38123
	H8/38020		H8/38122
H8/38024S Group	H8/38024S		H8/38121
	H8/38022S		H8/38120
	H8/38021S		
	H8/38020S		
	H8/38000S		

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Rev.8.00 2010.03

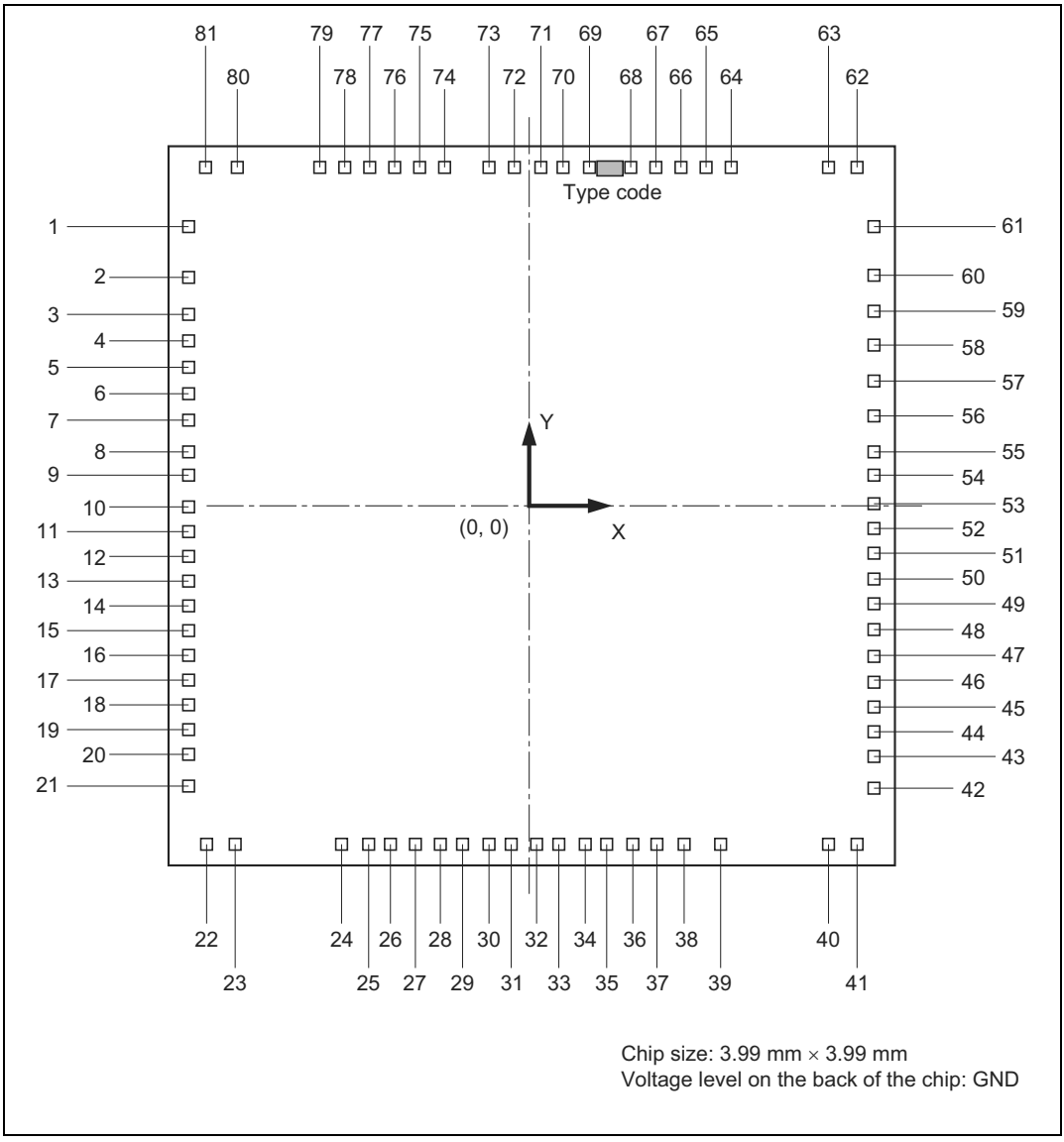


Figure 1.5 Bonding Pad Location Diagram of HCD64338024, HCD64338023, HCD64338022, HCD64338021, and HCD64338020 (Top View)

2.3.1 Data Formats in General Registers

Data of all the sizes above can be stored in general registers as shown in figure 2.3.

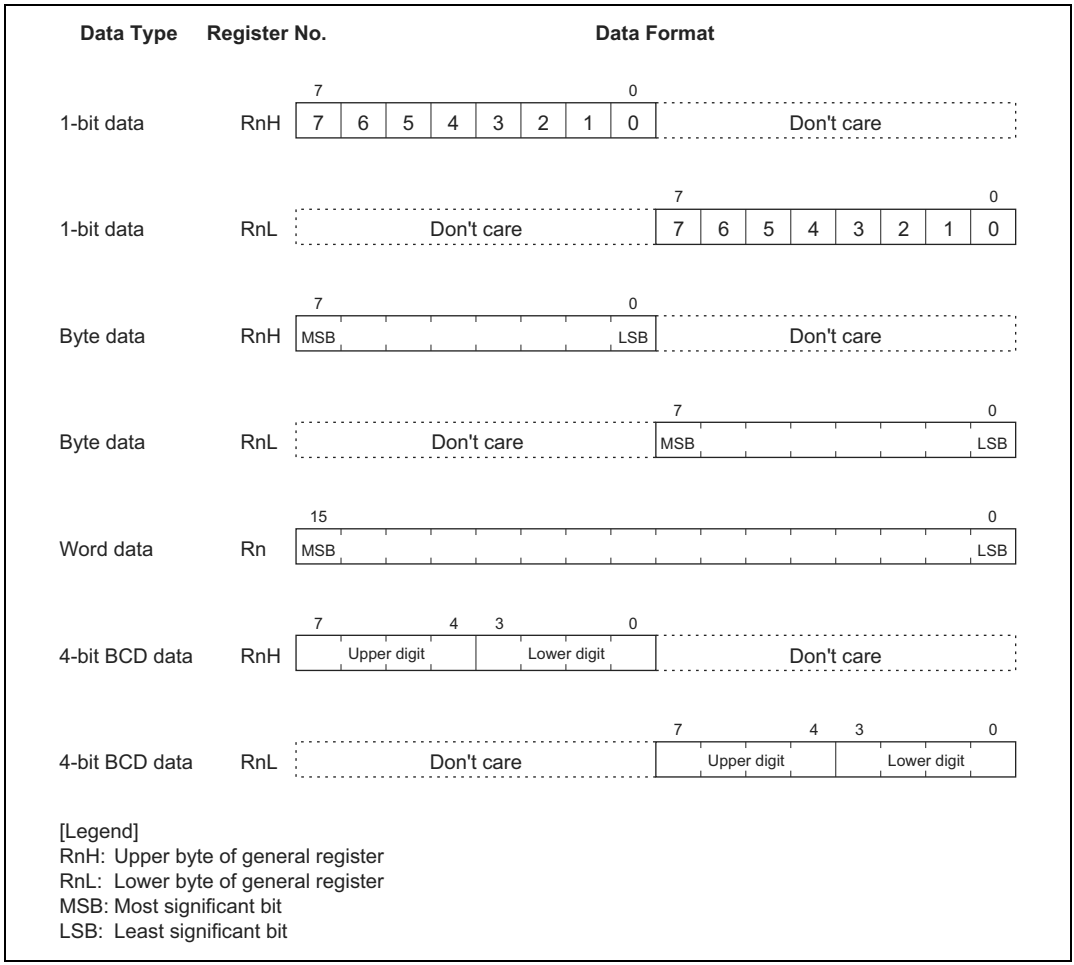


Figure 2.3 Register Data Formats

Figure 2.6 shows the instruction code format of arithmetic, logic, and shift instructions.

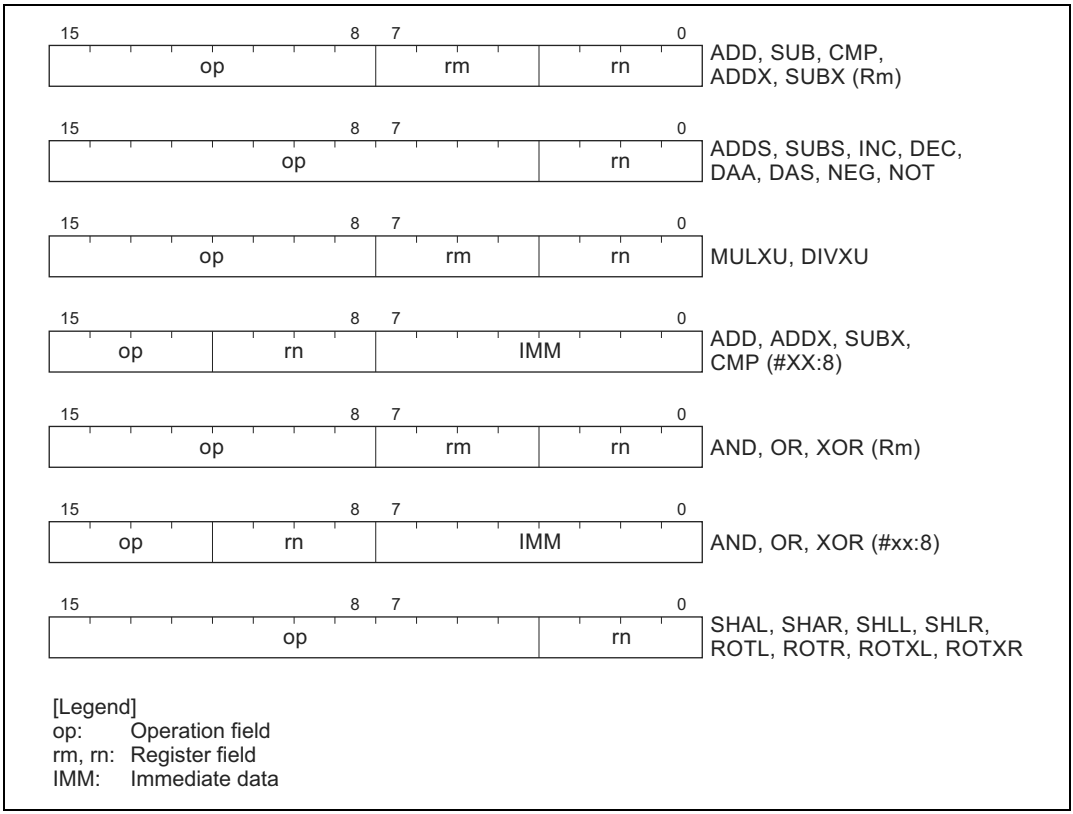


Figure 2.6 Arithmetic, Logic, and Shift Instruction Codes

External Clock Input Method

Connect an external clock signal to pin OSC_1, and leave pin OSC_2 open. Figure 4.7 shows a typical connection.

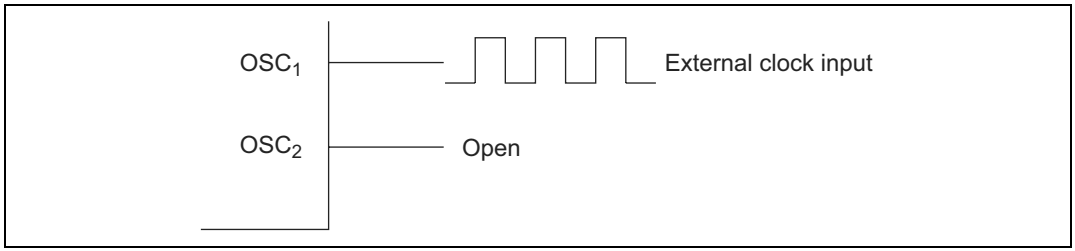


Figure 4.7 External Clock Input (Example)

Frequency	Oscillator Clock (ϕ_{osc})
Duty cycle	45% to 55%

On-Chip Oscillator Selection Method (H8/38124 Group Only)

The on-chip oscillator is selected by setting the IRQAEC pin input level during resets.* Table 4.3 lists the methods for selecting the system clock oscillator and the on-chip oscillator. The IRQAEC pin input level set during resets must be fixed at V_{CC} or GND, based on the oscillator to be selected. It is not necessary to connect an oscillator to pins OSC1 and OSC2 if the on-chip oscillator is selected. In this case, pin OSC1 should be fixed at V_{CC} or GND.

Note: The system clock oscillator must be selected in order to program or erase flash memory as part of operations such as on-board programming. Also, when using the on-chip emulator, an oscillator should be connected, or an external clock input, even if the on-chip oscillator is selected.

* Other than watchdog timer or low-voltage detect circuit reset.

Table 4.3 System Clock Oscillator and On-Chip Oscillator Selection Methods

IRQAEC pin input level (during resets)	0	1
System clock oscillator	Enabled	Disabled
On-chip oscillator	Disabled	Enabled

11. On the H8/38124 Group, operates only when the on-chip oscillator is selected; otherwise stops and stands by. On the H8/38024, H8/38024S, and H8/38024R Group, stops and stands by.

5.1.1 System Control Registers

The operation mode is selected using the system control registers described in table 5.3.

Table 5.3 System Control Registers

Name	Abbreviation	R/W	Initial Value	Address
System control register 1	SYSCR1	R/W	H'07	H'FFF0
System control register 2	SYSCR2	R/W	H'F0	H'FFF1

System Control Register 1 (SYSCR1)

Bit	7	6	5	4	3	2	1	0
	SSBY	STS2	STS1	STS0	LSON	—	MA1	MA0
Initial value	0	0	0	0	0	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	—	R/W	R/W

SYSCR1 is an 8-bit read/write register for control of the power-down modes.

Upon reset, SYSCR1 is initialized to H'07.

Bit 7—Software Standby (SSBY)

This bit designates transition to standby mode or watch mode.

Bit 7 SSBY	Description
0	• When a SLEEP instruction is executed in active mode, a transition is made to sleep mode (initial value) • When a SLEEP instruction is executed in subactive mode, a transition is made to subsleep mode
1	• When a SLEEP instruction is executed in active mode, a transition is made to standby mode or watch mode • When a SLEEP instruction is executed in subactive mode, a transition is made to watch mode

Bit 2 MSON	Description	
0	Operation in active (high-speed) mode	(initial value)
1	Operation in active (medium-speed) mode	

Bits 1 and 0—Subactive Mode Clock Select (SA1, SA0)

These bits select the CPU clock rate ($\phi_W/2$, $\phi_W/4$, or $\phi_W/8$) in subactive mode. SA1 and SA0 cannot be modified in subactive mode.

Bit 1 SA1	Bit 0 SA0	Description	
0	0	$\phi_W/8$	(initial value)
0	1	$\phi_W/4$	
1	*	$\phi_W/2$	

*: Don't care

5.2 Sleep Mode

5.2.1 Transition to Sleep Mode

1. Transition to sleep (high-speed) mode

   The system goes from active mode to sleep (high-speed) mode when a SLEEP instruction is executed while the SSBY and LSON bits in SYSCR1 are cleared to 0, the MSON and DTON bits in SYSCR2 are cleared to 0. In sleep mode CPU operation is halted but the on-chip peripheral functions. CPU register contents are retained.

2. Transition to sleep (medium-speed) mode

   The system goes from active mode to sleep (medium-speed) mode when a SLEEP instruction is executed while the SSBY and LSON bits in SYSCR1 are cleared to 0, the MSON bit in SYSCR2 is set to 1, and the DTON bit in SYSCR2 is cleared to 0. In sleep (medium-speed) mode, as in sleep (high-speed) mode, CPU operation is halted but the on-chip peripheral functions are operational. The clock frequency in sleep (medium-speed) mode is determined by the MA1 and MA0 bits in SYSCR1. CPU register contents are retained.

   Furthermore, it sometimes acts with half state early timing at the time of transition to sleep (medium-speed) mode.

5.5 Subsleep Mode

5.5.1 Transition to Subsleep Mode

The system goes from subactive mode to subsleep mode when a SLEEP instruction is executed while the SSBY bit in SYSCR1 is cleared to 0, LSON bit in SYSCR1 is set to 1, and TMA3 bit in TMA is set to 1. In subsleep mode, operation of on-chip peripheral modules other than the A/D converter and PWM is in active state. As long as a minimum required voltage is applied, the contents of CPU registers, the on-chip RAM and some registers of the on-chip peripheral modules are retained. I/O ports keep the same states as before the transition.

5.5.2 Clearing Subsleep Mode

Subsleep mode is cleared by an interrupt (timer A, timer C, timer F, timer G, asynchronous event counter, SCI3, IRQAEC, IRQ_4, IRQ_3, IRQ_1, IRQ_0, WKP_7 to WKP_0) or by a low input at the $\overline{RES}$ pin.

- Clearing by interrupt

  When an interrupt is requested, subsleep mode is cleared and interrupt exception handling starts. Subsleep mode is not cleared if the I bit of CCR is set to 1 or the particular interrupt is disabled in the interrupt enable register.

  To synchronize the interrupt request signal with the system clock, up to $2/\phi_{SUB}$(s) delay may occur after the interrupt request signal occurrence, before the interrupt exception handling start.

- Clearing by $\overline{RES}$ input

  Clearing by $\overline{RES}$ pin is the same as for standby mode; see Clearing by $\overline{RES}$ pin in section 5.3.2, Clearing Standby Mode.

<table>
<tr><th>Pin</th><th>Pin Functions and Selection Method</th></tr>
<tr><td>PB₁/AN₁/extU</td><td>Switching is accomplished by combining CH3 to CH0 in AMR and VINTUSEL in LVDCR as shown below. Note that VINTUSEL is implemented on the H8/38124 Group only.
<table>
<tr><td>VINTUSEL</td><td colspan="2">0</td><td>1</td></tr>
<tr><td>CH3 to CH0</td><td>Not B'0101</td><td>B'0101</td><td>*</td></tr>
<tr><td>Pin function</td><td>PB₁ input pin</td><td>AN₁ input pin</td><td>extU input pin</td></tr>
</table>
Note: The extU pin is implemented on the H8/38124 Group only.</td></tr>
<tr><td>PB₀/AN₀/extD</td><td>Switching is accomplished by combining CH3 to CH0 in AMR and VINTDSEL in LVDCR as shown below. Note that VINTDSEL is implemented on the H8/38124 Group only.
<table>
<tr><td>VINTDSEL</td><td colspan="2">0</td><td>1</td></tr>
<tr><td>CH3 to CH0</td><td>Not B'0100</td><td>B'0100</td><td>*</td></tr>
<tr><td>Pin function</td><td>PB₀ input pin</td><td>AN₀ input pin</td><td>extD input pin</td></tr>
</table>
Note: The extD pin is implemented on the H8/38124 Group only.</td></tr>
</table>

*: Don't care

8.12 Input/Output Data Inversion Function

8.12.1 Overview

With input pin RXD_{32} and output pin TXD_{32}, the data can be handled in inverted form.

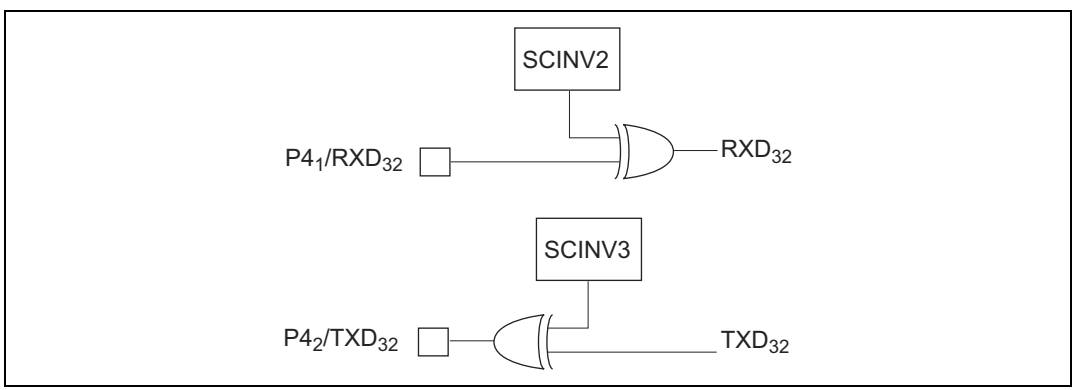


Figure 8.11 Input/Output Data Inversion Function

9.2.4 Timer A Operation States

Table 9.3 summarizes the timer A operation states.

Table 9.3 Timer A Operation States

Operation Mode		Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	Module Standby
TCA	Interval	Reset	Functions	Functions	Halted	Halted	Halted	Halted	Halted
	Clock time base	Reset	Functions	Functions	Functions	Functions	Functions	Halted	Halted
TMA		Reset	Functions	Retained	Retained	Functions	Retained	Retained	Retained

Note: When the real-time clock time base function is selected as the internal clock of TCA in active mode or sleep mode, the internal clock is not synchronous with the system clock, so it is synchronized by a synchronizing circuit. This may result in a maximum error of 1/ϕ (s) in the count cycle.

9.2.5 Application Note

When bit 0 (TACKSTP) of the clock stop register 1 (CKSTPR1) is cleared to 0, bit 3 (TMA3) of the timer mode register A (TMA) cannot be rewritten.

Set bit 0 (TACKSTP) of the clock stop register 1 (CKSTPR1) to 1 before rewriting bit 3 (TMA3) of the timer mode register A (TMA).

10.1.3 Pin Configuration

Table 10.1 shows the SCI3 pin configuration.

Table 10.1 Pin Configuration

Name	Abbr.	I/O	Function
SCI3 clock	SCK_{32}	I/O	SCI3 clock input/output
SCI3 receive data input	RXD_{32}	Input	SCI3 receive data input
SCI3 transmit data output	TXD_{32}	Output	SCI3 transmit data output

10.1.4 Register Configuration

Table 10.2 shows the SCI3 register configuration.

Table 10.2 Registers

Name	Abbr.	R/W	Initial Value	Address
Serial mode register	SMR	R/W	H'00	H'FFA8
Bit rate register	BRR	R/W	H'FF	H'FFA9
Serial control register 3	SCR3	R/W	H'00	H'FFAA
Transmit data register	TDR	R/W	H'FF	H'FFAB
Serial status register	SSR	R/W	H'84	H'FFAC
Receive data register	RDR	R	H'00	H'FFAD
Transmit shift register	TSR	Protected	—	—
Receive shift register	RSR	Protected	—	—
Bit rate counter	BRC	Protected	—	—
Clock stop register 1	CKSTPR1	R/W	H'FF	H'FFFA
Serial port control register	SPCR	R/W	—	H'FF91

SCI3 operates as follows when transmitting data.

SCI3 monitors bit TDRE in SSR, and when it is cleared to 0, recognizes that data has been written to TDR and transfers data from TDR to TSR. It then sets bit TDRE to 1 and starts transmitting. If bit TIE in SCR3 is set to 1 at this time, a TXI request is made.

Serial data is transmitted from the TXD_{32} pin using the relevant data transfer format in table 10.11. When the stop bit is sent, SCI3 checks bit TDRE. If bit TDRE is cleared to 0, SCI3 transfers data from TDR to TSR, and when the stop bit has been sent, starts transmission of the next frame. If bit TDRE is set to 1, bit TEND in SSR bit is set to 1the mark state, in which 1s are transmitted, is established after the stop bit has been sent. If bit TEIE in SCR3 is set to 1 at this time, a TEI request is made.

Figure 10.7 shows an example of the operation when transmitting in asynchronous mode.

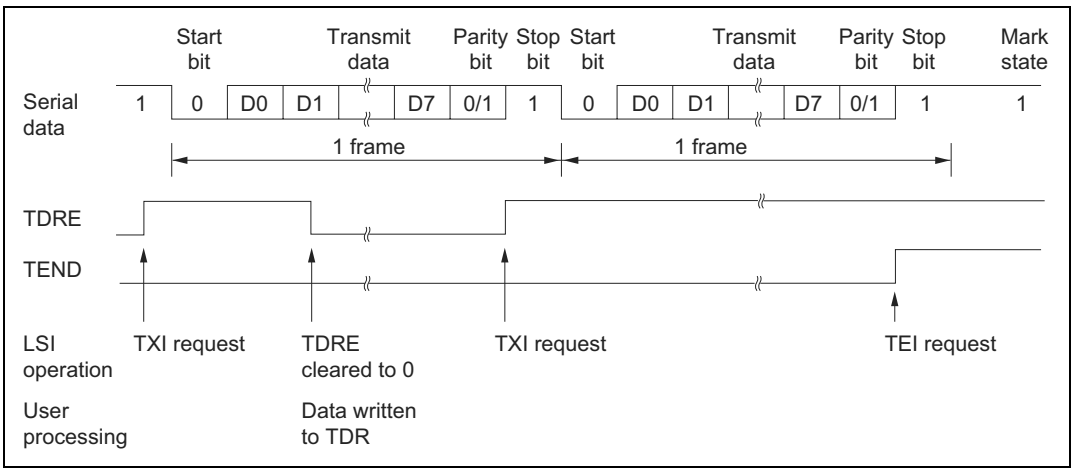


Figure 10.7 Example of Operation when Transmitting in Asynchronous Mode (8-bit data, parity, 1 stop bit)

SCI3 operates as follows when receiving data.

SCI3 performs internal synchronization and begins reception in synchronization with the serial clock input or output.

The received data is placed in RSR in LSB-to-MSB order.

After the data has been received, SCI3 checks that bit RDRF is set to 0, indicating that the receive data can be transferred from RSR to RDR.

If this check shows that there is no overrun error, bit RDRF is set to 1, and the receive data is stored in RDR. If bit RIE is set to 1 in SCR3, an RXI interrupt is requested. If the check identifies an overrun error, bit OER is set to 1.

Bit RDRF remains set to 1. If bit RIE is set to 1 in SCR3, an ERI interrupt is requested.

See table 10.12 for the conditions for detecting a receive error, and receive data processing.

Note: No further receive operations are possible while a receive error flag is set. Bits OER, FER, PER, and RDRF must therefore be cleared to 0 before resuming reception.

Figure 10.14 shows an example of the operation when receiving in synchronous mode.

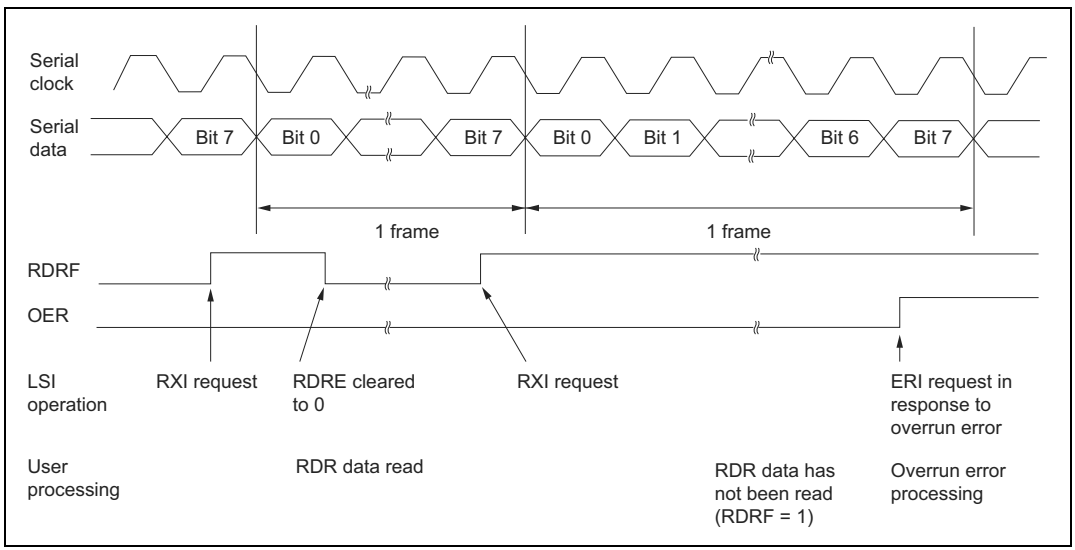


Figure 10.14 Example of Operation when Receiving in Synchronous Mode

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Allowable output high current (total)	$\sum -I_{OH}$	All output pins	—	—	15.0	mA	V_{CC} = 4.0 V to 5.5 V	
			—	—	10.0		Except the above	

Notes: Connect the TEST pin to V_{SS}.

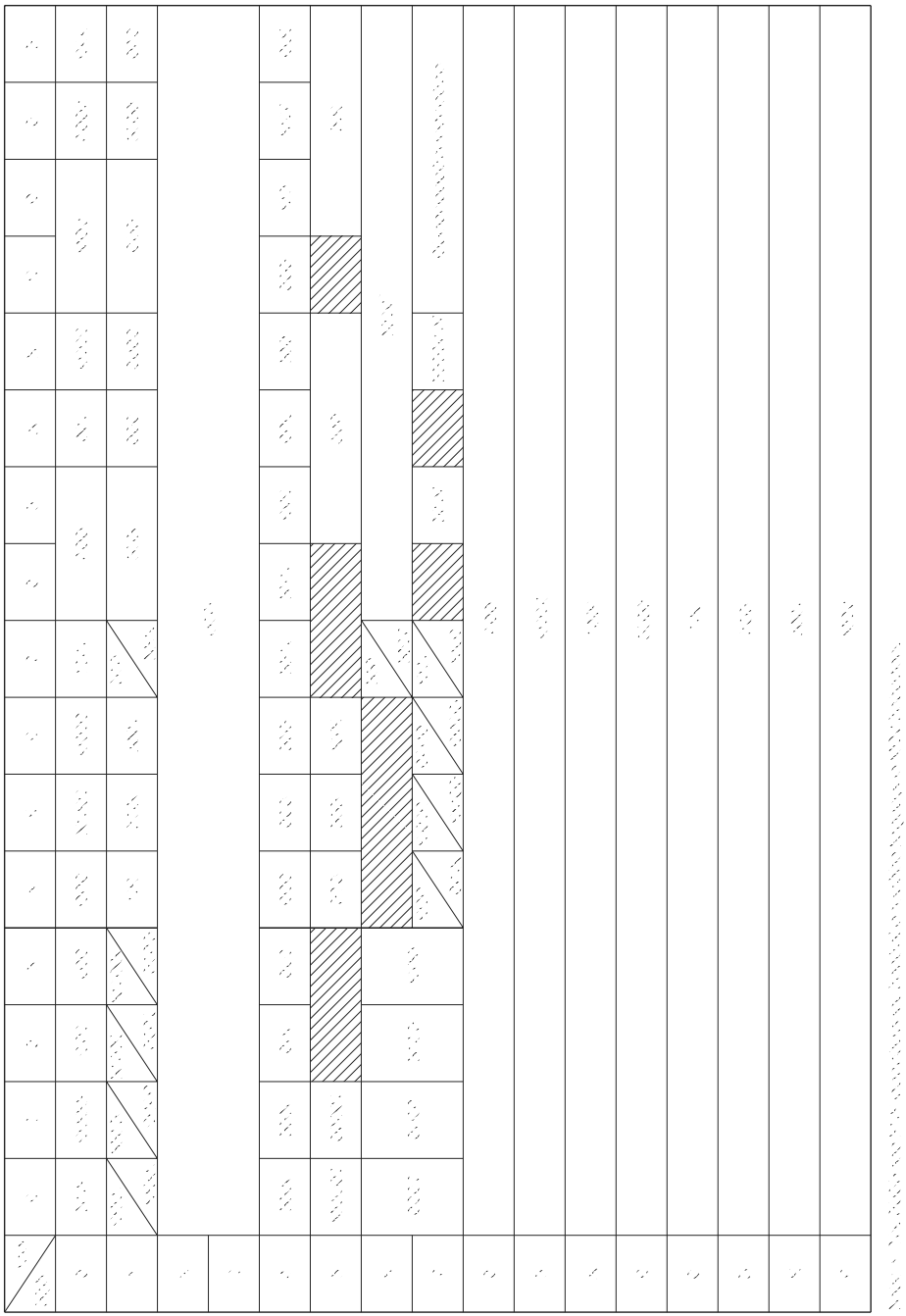
1. Applies to the Mask ROM products.
2. Applies to the HD64738024.
3. Pin states during current measurement.

Mode	$\overline{RES}$ Pin	Internal State	Other Pins	LCD Power Supply	Oscillator Pins
Active (high-speed) mode (I_{OPE1})	V_{CC}	Operates	V_{CC}	Halted	System clock oscillator: crystal
Active (medium-speed) mode (I_{OPE2})					Subclock oscillator: Pin X_1 = GND
Sleep mode	V_{CC}	Only timers operate	V_{CC}	Halted	
Subactive mode	V_{CC}	Operates	V_{CC}	Halted	System clock oscillator: crystal
Subsleep mode	V_{CC}	Only timers operate, CPU stops	V_{CC}	Halted	Subclock oscillator: crystal
Watch mode	V_{CC}	Only time base operates, CPU stops	V_{CC}	Halted	
Standby mode	V_{CC}	CPU and timers both stop	V_{CC}	Halted	System clock oscillator: crystal
					Subclock oscillator: Pin X_1 = GND

4. Excludes current in pull-up MOS transistors and output buffers.
5. When the PIOFF bit in the port mode register 9 is 0.
6. When the PIOFF bit in the port mode register 9 is 1.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Output low voltage	V_{OL}	$P1_3$, $P1_4$, $P1_6$, $P1_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_2$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, PA_0 to PA_3	—	—	0.5	V	I_{OL} = 0.4 mA	
		$P9_0$ to $P9_2$	—	—	0.5	V	I_{OL} = 25 mA	*1
							I_{OL} = 10 mA	*2
		$P9_3$ to $P9_5$	—	—	0.5	V	I_{OL} = 10 mA	
Input/output leakage current	$\lvert I_{IL} \rvert$	$\overline{RES}$, $P4_3$, OSC_1, X_1, $P1_3$, $P1_4$, $P1_6$, $P1_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_2$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, IRQAEC, $P9_0$ to $P9_5$, PA_0 to PA_3	—	—	1.0	µA	V_{IN} = 0.5 V to V_{CC} – 0.5 V	
		PB_0 to PB_7	—	—	1.0	µA	V_{IN} = 0.5 V to AV_{CC} – 0.5 V	
Pull-up MOS current	$-I_p$	$P1_3$, $P1_4$, $P1_6$, $P1_7$, $P3_0$ to $P3_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$	30	—	180	µA	V_{CC} = 3 V, V_{IN} = 0 V	
Input capacitance	C_{IN}	All input pins except power supply and IRQAEC	—	—	15.0	pF	f = 1 MHz, V_{IN} =0 V, T_a = 25°C	
		IRQAEC	—	—	30.0	pF		

Table A.2 Operation Code Map



Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
MOV	MOV.W Rs, @Rd	1				1	
	MOV.W Rs, @(d:16, Rd)	2				1	
	MOV.W Rs, @–Rd	1				1	2
	MOV.W Rs, @aa:16	2				1	
MULXU	MULXU.B Rs, Rd	1					12
NEG	NEG.B Rd	1					
NOP	NOP	1					
NOT	NOT.B Rd	1					
OR	OR.B #xx:8, Rd	1					
	OR.B Rs, Rd	1					
ORC	ORC #xx:8, CCR	1					
ROTL	ROTL.B Rd	1					
ROTR	ROTR.B Rd	1					
ROTXL	ROTXL.B Rd	1					
ROTXR	ROTXR.B Rd	1					
RTE	RTE	2		2			2
RTS	RTS	2		1			2
SHAL	SHAL.B Rd	1					
SHAR	SHAR.B Rd	1					
SHLL	SHLL.B Rd	1					
SHLR	SHLR.B Rd	1					
SLEEP	SLEEP	1					
STC	STC CCR, Rd	1					
SUB	SUB.B Rs, Rd	1					
	SUB.W Rs, Rd	1					
SUBS	SUBS.W #1, Rd	1					
	SUBS.W #2, Rd	1					
POP	POP Rd	1		1			2
PUSH	PUSH Rs	1		1			2
SUBX	SUBX.B #xx:8, Rd	1					
	SUBX.B Rs, Rd	1					
XOR	XOR.B #xx:8, Rd	1					
	XOR.B Rs, Rd	1					
XORC	XORC #xx:8, CCR	1					

Appendix B Internal I/O Registers

B.1 Addresses

Upper Address: H'F0

Lower Address	Register Name	Bit Names								Module Name
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'20	FLMCR1	—	SWE	ESU	PSU	EV	PV	E	P	ROM
H'21	FLMCR2	FLER	—	—	—	—	—	—	—	
H'22	FLPWCR	PDWND	—	—	—	—	—	—	—	
H'23	EBR	—	—	—	EB4	EB3	EB2	EB1	EB0	
H'24										
H'25										
H'26										
H'27										
H'28										
H'29										
H'2A										
H'2B	FENR	FLSHE	—	—	—	—	—	—	—	
H'2C										
H'2D										
H'2E										
H'2F										

Upper Address: H'FF

Lower Address	Register Name	Bit Names								
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
H'A0										
H'A1										
H'A2										
H'A3										
H'A4										
H'A5										
H'A6										
H'A7										
H'A8	SMR	COM	CHR	PE	PM	STOP	MP	CKS1	CKS0	SCI3
H'A9	BRR	BRR7	BRR6	BRR5	BRR4	BRR3	BRR2	BRR1	BRR0	
H'AA	SCR3	TIE	RIE	TE	RE	—	TEIE	CKE1	CKE0	
H'AB	TDR	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0	
H'AC	SSR	TDRE	RDRF	OER	FER	PER	TEND	—	—	
H''AD	RDR	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0	
H'AE										
H'AF										
H'B0	TMA	—	—	—	—	TMA3	TMA2	TMA1	TMA0	Timer A
H'B1	TCA	TCA7	TCA6	TCA5	TCA4	TCA3	TCA2	TCA1	TCA0	
H'B2	TCSRW	B6WI	TCWE	B4WI	TCSRWE	B2WI	WDON	BOWI	WRST	Watchdog
H'B3	TCW	TCW7	TCW6	TCW5	TCW4	TCW3	TCW2	TCW1	TCW0	timer
H'B4	TMC	TMC7	TMC6	TMC5	—	—	TMC2	TMC1	TMC0	Timer C
H'B5	TCC/TLC	TCC7/TLC7	TCC6/TLC6	TCC5/TLC5	TCC4/TLC4	TCC3/TLC3	TCC2/TLC2	TCC1/TLC1	TCC0/TLC0	
H'B6	TCRF	TOLH	CKSH2	CKSH1	CKSH0	TOLL	CKSL2	CKSL1	CKSL0	Timer F
H'B7	TCSRF	OVFH	CMFH	OVIEH	CCLRH	OVFL	CMFL	OVIEL	CCLRL	
H'B8	TCFH	TCFH7	TCFH6	TCFH5	TCFH4	TCFH3	TCFH2	TCFH1	TCFH0	
H'B9	TCFL	TCFL7	TCFL6	TCFL5	TCFL4	TCFL3	TCFL2	TCFL1	TCFL0	
H'BA	OCRFH	OCRFH7	OCRFH6	OCRFH5	OCRFH4	OCRFH3	OCRFH2	OCRFH1	OCRFH0	
H'BB	OCRFL	OCRFL7	OCRFL6	OCRFL5	OCRFL4	OCRFL3	OCRFL2	OCRFL1	OCRFL0	
H'BC	TMG	OVFH	OVFL	OVIE	IIEGS	CCLR1	CCLR0	CKS1	CKS0	Timer G
H'BD	ICRGF	ICRGF7	ICRGF6	ICRGF5	ICRGF4	ICRGF3	ICRGF2	ICRGF1	ICRGF0	
H'BE	ICRGR	ICRGR7	ICRGR6	ICRGR5	ICRGR4	ICRGR3	ICRGR2	ICRGR1	ICRGR0	
H'BF										

Appendix I Specifications of Chip Tray

The specifications of the chip tray for the HCD64338024, HCD64338023, HCD64338022, HCD64338021, and HCD64338020 are shown in figure I.1. The specifications of the chip tray for the HCD64F38024 and HCD64F38024R are shown in figure I.2. The specifications of the chip tray for the HCD64338024S, HCD64338023S, HCD64338022S, HCD64338021S, and HCD64338020S are shown in figure I.3.

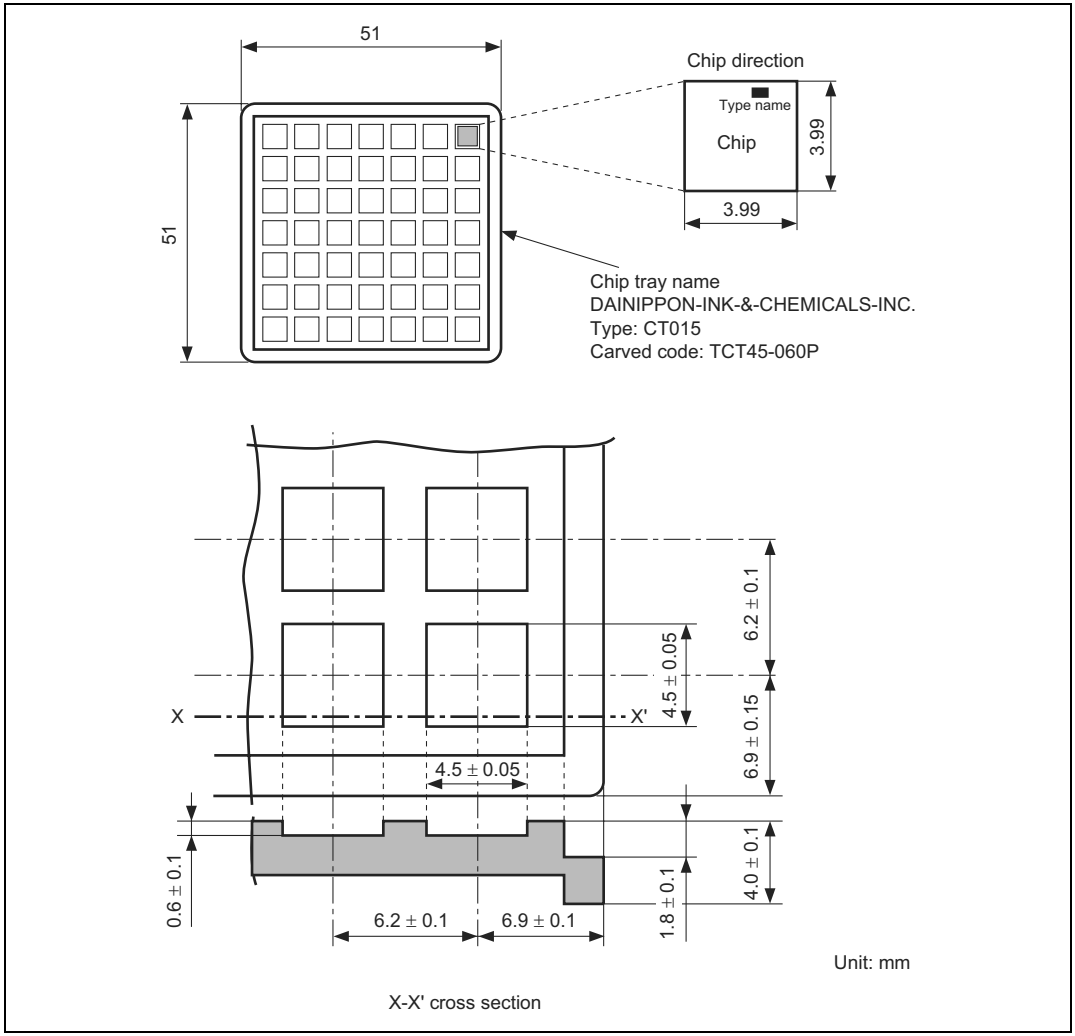


Figure I.1 Specifications of Chip Tray for the HCD64338024, HCD64338023, HCD64338022, HCD64338021, and HCD64338020