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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

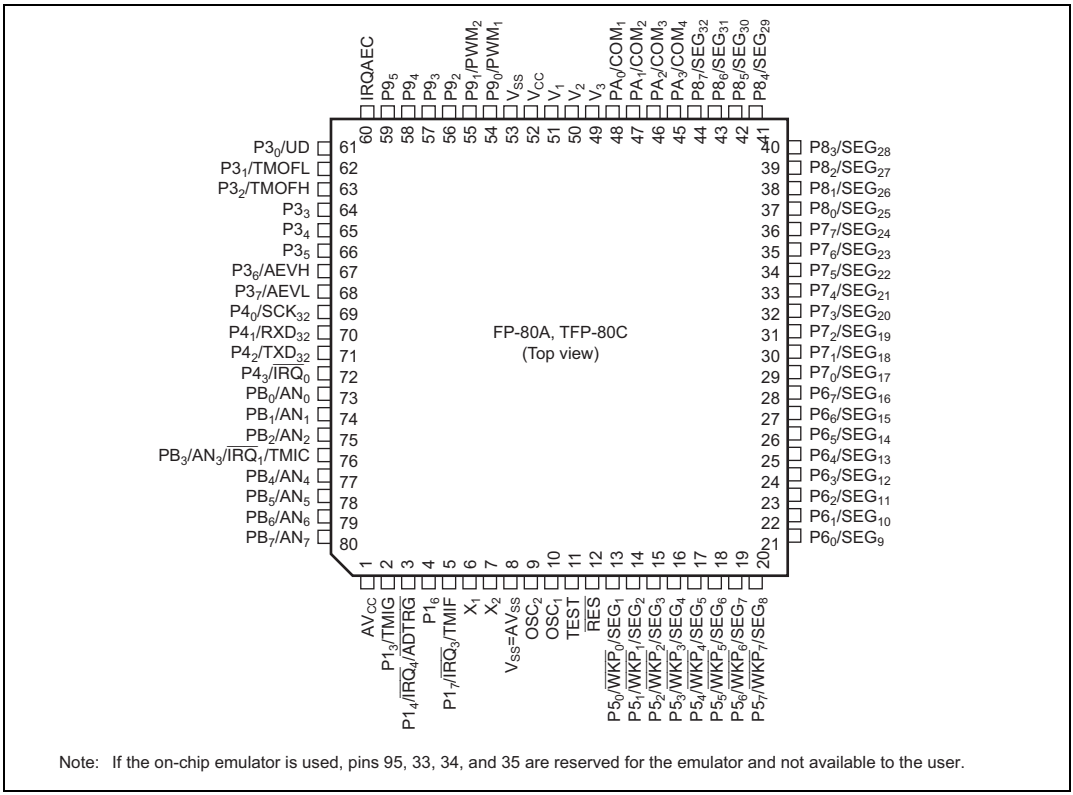
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	5MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f38024rfv

1.3 Pin Arrangement and Functions

1.3.1 Pin Arrangement

The H8/38024 Group, H8/38024R Group, H8/38024S Group, and H8/38124 Group pin arrangements are shown in figures 1.2, 1.3, and 1.4. The bonding pad location diagram of the HCD64338024, HCD64338023, HCD64338022, HCD64338021, and HCD64338020 is shown in figure 1.5. The bonding pad coordinates of the HCD64338024, HCD64338023, HCD64338022, HCD64338021, and HCD64338020 are given in table 1.2. The bonding pad location diagram of the HCD64F38024, HCD64F38024R is shown in figure 1.6. The bonding pad coordinates of the HCD64F38024 are given in table 1.3. The bonding pad location diagram of the HCD64338024S, HCD64338023S, HCD64338022S, HCD64338021S, and HCD64338020S is shown in figure 1.7. The bonding pad coordinates of the HCD64338024S, HCD64338023S, HCD64338022S, HCD64338021S, and HCD64338020S are given in table 1.4.



Note: If the on-chip emulator is used, pins 95, 33, 34, and 35 are reserved for the emulator and not available to the user.

Figure 1.2(1) Pin Arrangement (FP-80A, TFP-80C: Top View, H8/38024 Group, H8/38024R Group, H8/38024S Group)

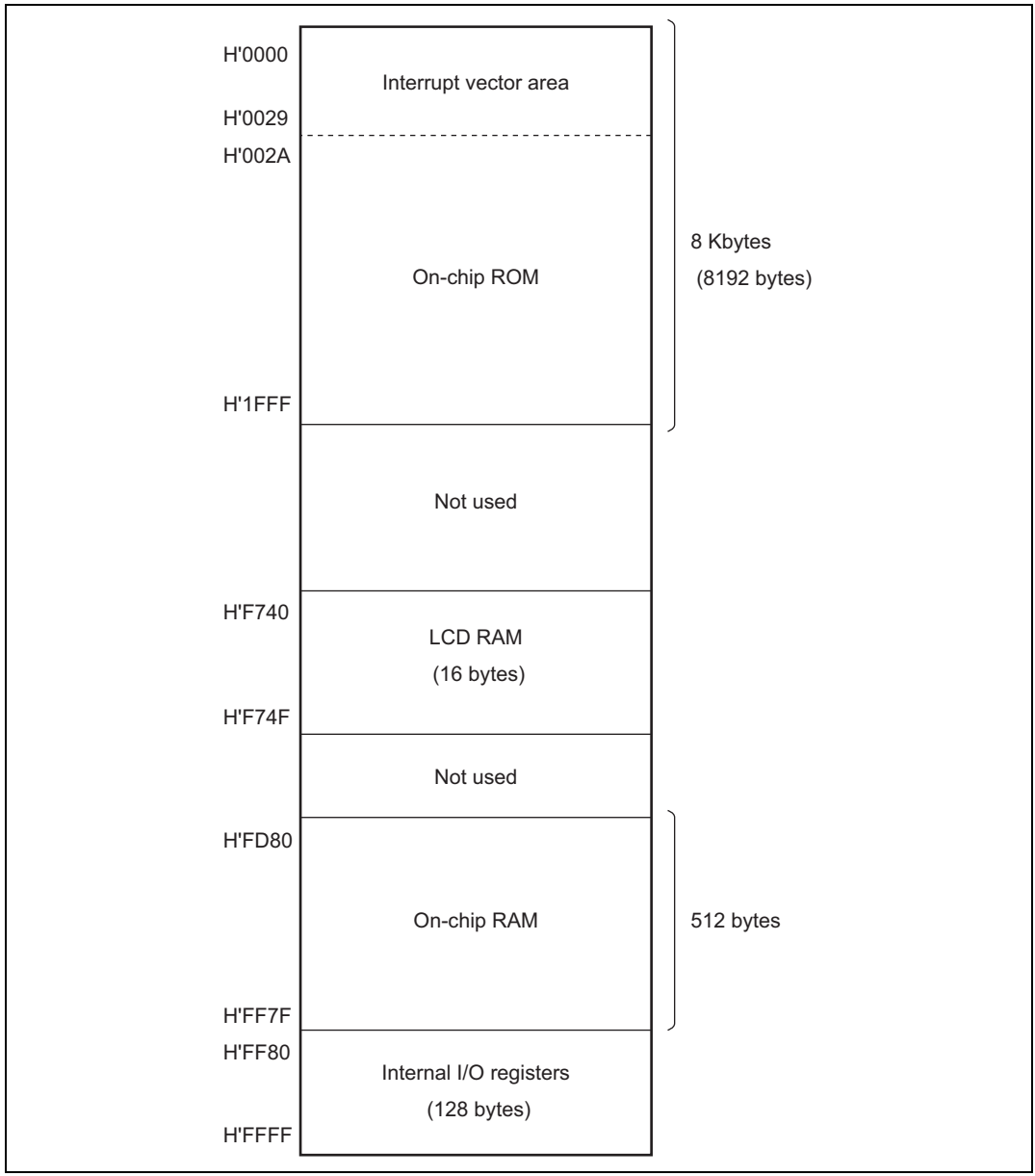


Figure 2.16(5) H8/38020, H8/38020S, and H8/38120 Memory Map

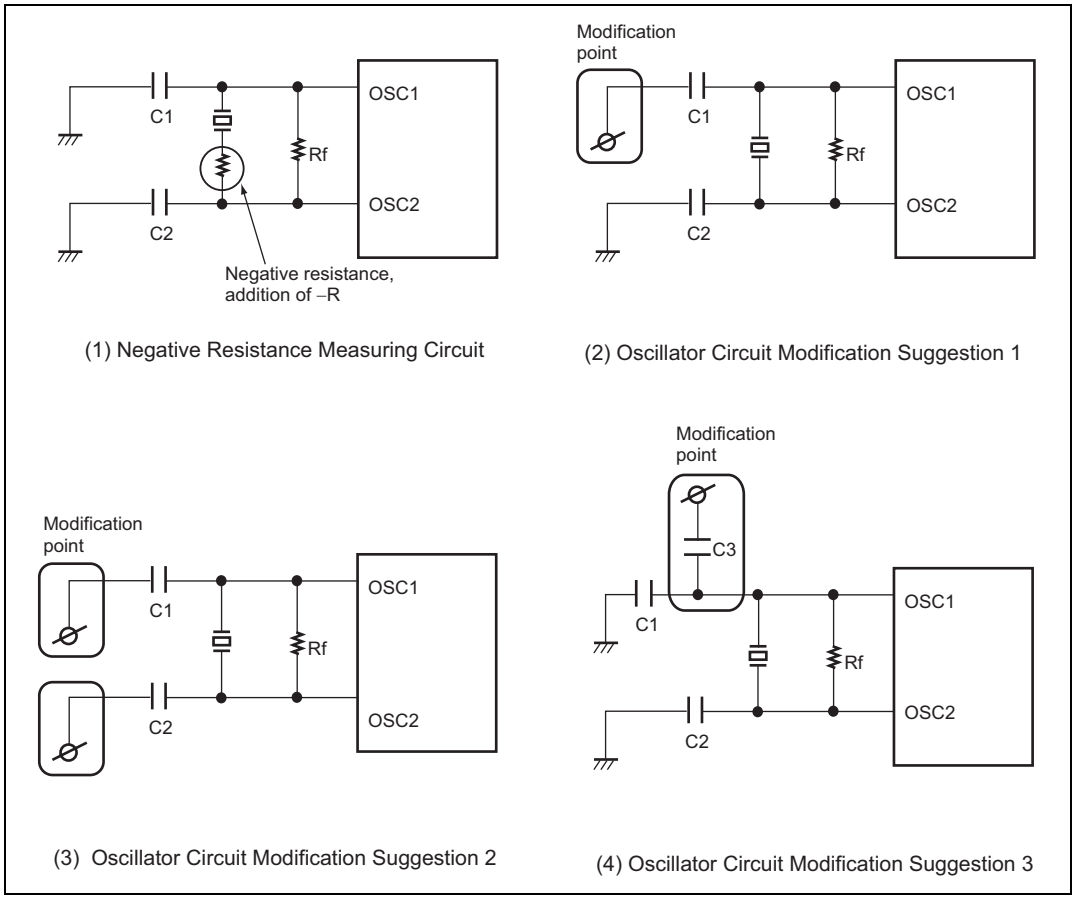


Figure 4.13 Negative Resistance Measurement and Circuit Modification Suggestions

4.5.1 Definition of Oscillation Stabilization Wait Time

Figure 4.14 shows the oscillation waveform (OSC2), system clock (ϕ), and microcomputer operating mode when a transition is made from standby mode, watch mode, or subactive mode, to active (high-speed/medium-speed) mode, with an oscillator element connected to the system clock oscillator.

As shown in figure 4.13, as the system clock oscillator is halted in standby mode, watch mode, and subactive mode, when a transition is made to active (high-speed/medium-speed) mode, the sum of the following two times (oscillation stabilization time and wait time) is required.

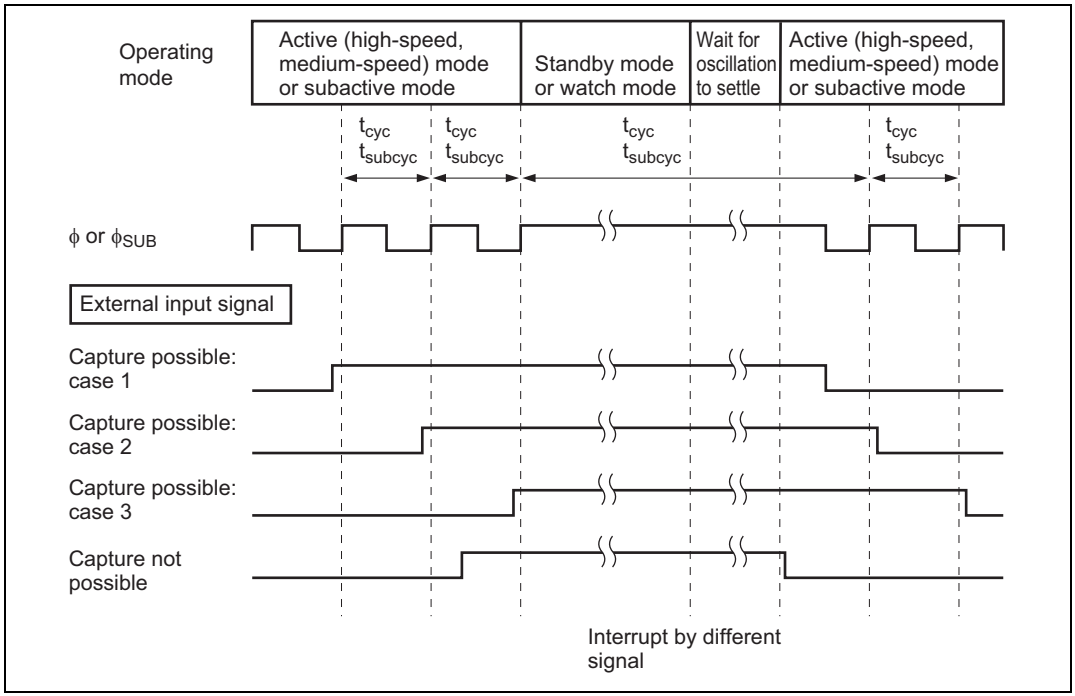


Figure 5.3 External Input Signal Capture when Signal Changes before/after Standby Mode or Watch Mode

4. Input pins to which these notes apply:
   $\overline{IRQ_4}$, $\overline{IRQ_3}$, $\overline{IRQ_1}$, $\overline{IRQ_0}$, $\overline{WKP_7}$ to $\overline{WKP_0}$, IRQAEC, TMIC, TMIF, TMIG, $\overline{ADTRG}$.

5.4 Watch Mode

5.4.1 Transition to Watch Mode

The system goes from active or subactive mode to watch mode when a SLEEP instruction is executed while the SSBY bit in SYSCR1 is set to 1 and bit TMA3 in TMA is set to 1.

In watch mode, operation of on-chip peripheral modules is halted except for timer A, timer F, timer G, AEC and the LCD controller/driver (for which operation or halting can be set) is halted. As long as a minimum required voltage is applied, the contents of CPU registers, the on-chip RAM and some registers of the on-chip peripheral modules, are retained. I/O ports keep the same states as before the transition.

Bit 3 EV	Description	
0	Erase-verify mode is cancelled	(initial value)
1	The flash memory changes to erase-verify mode	

Bit 2—Program-Verify (PV)

This bit is to set changing to or cancelling program-verify mode (do not set SWE, ESU, PSU, EV, E, and P bits at the same time).

Bit 2 PV	Description	
0	Program-verify mode is cancelled	(initial value)
1	The flash memory changes to program-verify mode	

Bit 1—Erase (E)

This bit is to set changing to or cancelling erase mode (do not set SWE, ESU, PSU, EV, PV, and P bits at the same time).

Bit 1 E	Description	
0	Erase mode is cancelled	(initial value)
1	When this bit is set to 1, while the SWE = 1 and ESU = 1, the flash memory changes to erase mode.	

Bit 0—Program (P)

This bit is to set changing to or cancelling program mode (do not set SWE, ESU, PSU, EV, PV, and E bits at the same time).

Bit 0 P	Description	
0	Program mode is cancelled	(initial value)
1	When this bit is set to 1, while the SWE = 1 and PSU = 1, the flash memory changes to program mode.	

6.7.2 Programming/Erasing in User Program Mode

The term user mode refers to the status when a user program is being executed. On-board programming/erasing of an individual flash memory block can also be performed in user program mode by branching to a user program/erase control program. The user must set branching conditions and provide on-board means of supplying programming data. The flash memory must contain the user program/erase control program or a program that provides the user program/erase control program from external memory. As the flash memory itself cannot be read during programming/erasing, transfer the user program/erase control program to on-chip RAM, as in boot mode. Figure 6.9 shows a sample procedure for programming/erasing in user program mode. Prepare a user program/erase control program in accordance with the description in section 6.8, Flash Memory Programming/Erasing.

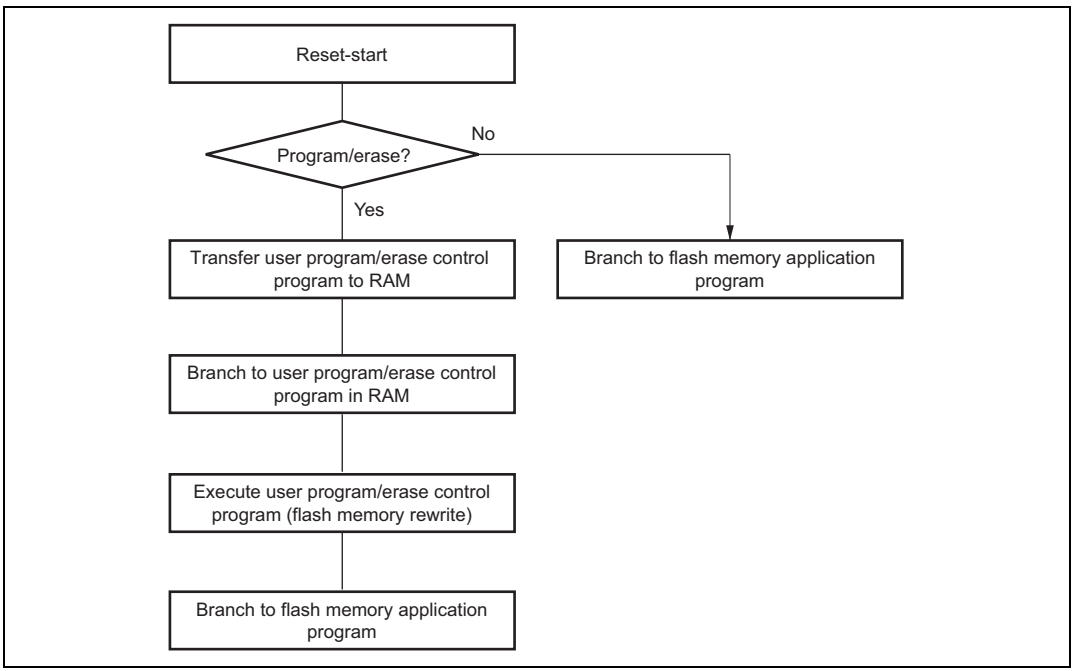


Figure 6.9 Programming/Erasing Flowchart Example in User Program Mode

8.9.2 Register Configuration and Description

Table 8.23 shows the port 9 register configuration.

Table 8.23 Port 9 Registers

Name	Abbr.	R/W	Initial Value	Address
Port data register 9	PDR9	R/W	H'FF	H'FFDC
Port mode register 9	PMR9	R/W	—	H'FFEC

Port Data Register 9 (PDR9)

Bit	7	6	5	4	3	2	1	0
	—	—	$P9_5$	$P9_4$	$P9_3$	$P9_2$	$P9_1$	$P9_0$
Initial value	1	1	1	1	1	1	1	1
Read/Write	—	—	R/W	R/W	R/W	R/W	R/W	R/W

PDR9 is an 8-bit register that stores data for port 9 pins $P9_5$ to $P9_0$.

Upon reset, PDR9 is initialized to H'FF.

Port Mode Register 9 (PMR9)

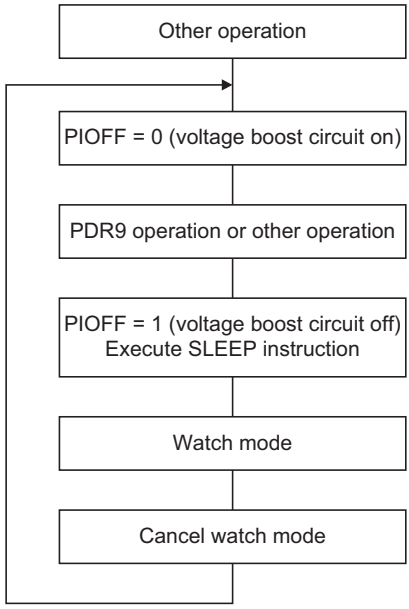
Bit	7	6	5	4	3	2	1	0
	—	—	—	—	PIOFF/—*	—	PWM_2	PWM_1
Initial value	1	1	1	1	0	—	0	0
Read/Write	—	—	—	—	R/W	W	R/W	R/W

Note: * Readable/writable reserved bit in the H8/38024S Group and H8/38124 Group.

PMR9 is an 8-bit read/write register controlling the selection of the $P9_0$ and $P9_1$ pin functions.

from 1 to 0 only when the PIOFF bit is cleared to 0. Also, if a large current flow is required, the PIOFF bit should be set to 1 and all the port data bits set to 1. Then clear PIOFF to 0 and, after allowing 30 clock cycles to permit stabilization of the voltage boost circuit, clear the port data bits to 0. If time is not provided to allow the voltage boost circuit to stabilize, it will not be possible to produce a large current flow. There are no such restrictions when setting port data bits from 0 to 1, regardless of the size of the current flow. To shut down the voltage boost circuit, set PIOFF to 1 after programming the port data bits. An example of the sequence of steps is provided below.

(Example Procedure) Shutting Down the in the Watch Mode without a Large Current Flow to Port 9



Bit 2—Reserved

This bit is reserved; it can only be written with 0.

Bits 1 and 0—$P9_n$/PWM Pin Function Switches

These pins select whether pin P9n/PWMn+1 is used as P9n or as PWMn+1.

Bit n WKPn+1	Description	
0	Functions as $P9_n$ output pin	(initial value)
1	Functions as PWM_{n+1} output pin	

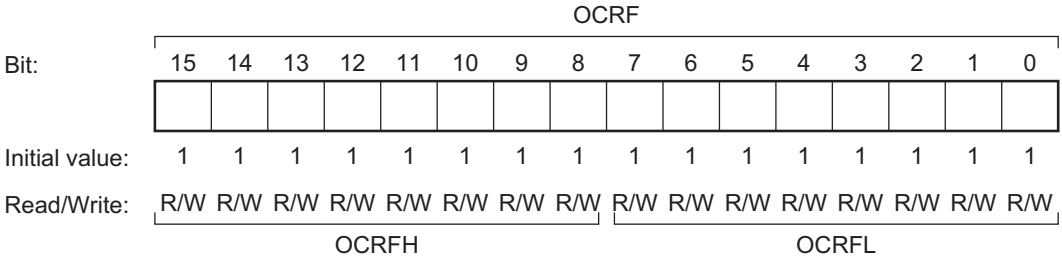
(n = 0 or 1)

Bits 3 to 0—Internal Clock Select (TMA3 to TMA0)

Bits 3 to 0 select the clock input to TCA. The selection is made as follows.

				Description	
Bit 3 TMA3	**Bit 2 TMA2**	**Bit 1 TMA1**	**Bit 0 TMA0**	**Prescaler and Divider Ratio or Overflow Period**	**Function**
0	0	0	0	PSS, ϕ/8192 (initial value)	Interval timer
			1	PSS, ϕ/4096	
		1	0	PSS, ϕ/2048	
			1	PSS, ϕ/512	
	1	0	0	PSS, ϕ/256	
			1	PSS, ϕ/128	
		1	0	PSS, ϕ/32	
			1	PSS, ϕ/8	
1	0	0	0	PSW, 1 s	Clock time
			1	PSW, 0.5 s	base
		1	0	PSW, 0.25 s	(when using
			1	PSW, 0.03125 s	32.768 kHz)
	1	0	0	PSW and TCA are reset	
			1		
		1	0		
			1		

16-bit Output Compare Register (OCRF)
8-bit Output Compare Register (OCRFH)
8-bit Output Compare Register (OCRFL)



OCRF is a 16-bit read/write register composed of the two registers OCRFH and OCRFL. In addition to the use of OCRF as a 16-bit register with OCRFH as the upper 8 bits and OCRFL as the lower 8 bits, OCRFH and OCRFL can also be used as independent 8-bit registers.

OCRFH and OCRFL can be read and written by the CPU, but when they are used in 16-bit mode, data transfer to and from the CPU is performed via a temporary register (TEMP). For details of TEMP, see section 9.4.3, CPU Interface.

OCRFH and OCRFL are each initialized to H'FF upon reset.

a. 16-bit mode (OCRF)

When CKSH2 is cleared to 0 in TCRF, OCRF operates as a 16-bit register. OCRF contents are constantly compared with TCF, and when both values match, CMFH is set to 1 in TCSRF. At the same time, IRRTFH is set to 1 in IRR2. If IENTFH in IENR2 is 1 at this time, an interrupt request is sent to the CPU.

Toggle output can be provided from the TMOFH pin by means of compare matches, and the output level can be set (high or low) by means of TOLH in TCRF.

b. 8-bit mode (OCRFH/OCRFL)

When CKSH2 is set to 1 in TCRF, OCRFH, and OCRFL operate as two independent 8-bit registers. OCRFH contents are compared with TCFH, and OCRFL contents are with TCFL. When the OCRFH (OCRFL) and TCFH (TCFL) values match, CMFH (CMFL) is set to 1 in TCSRF. At the same time, IRRTFH (IRRTFL) is set to 1 in IRR2. If IENTFH (IENTFL) in IENR2 is 1 at this time, an interrupt request is sent to the CPU.

Toggle output can be provided from the TMOFH pin (TMOFL pin) by means of compare matches, and the output level can be set (high or low) by means of TOLH (TOLL) in TCRF.

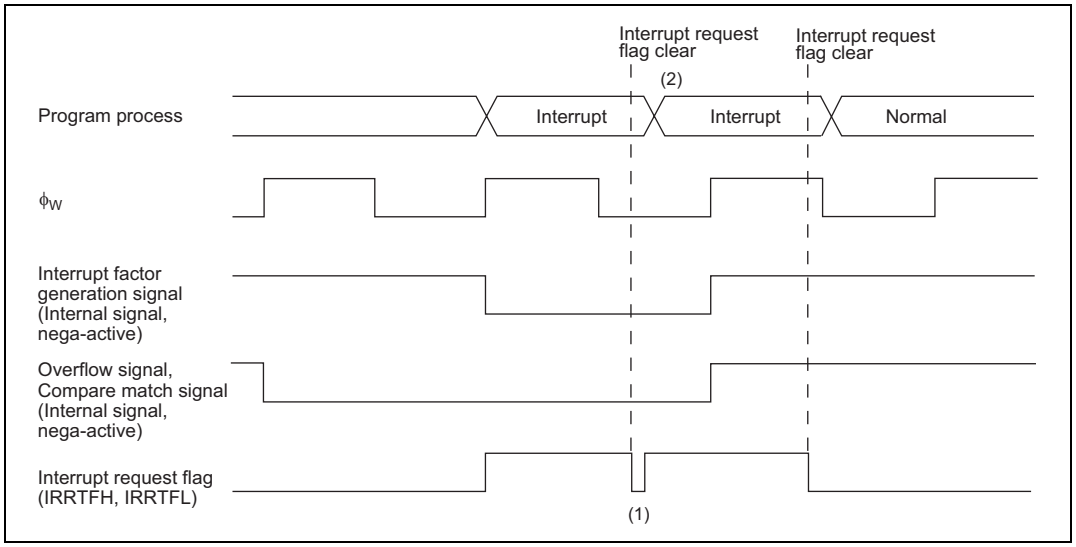


Figure 9.7 Clear Interrupt Request Flag when Interrupt Factor Generation Signal is Valid

Timer Counter (TCF) Read/Write

When ϕw/4 is selected as the internal clock in active (high-speed, medium-speed) mode, write on TCF is impossible. And, when read TCF, as the system clock and internal clock are mutually asynchronous, TCF synchronizes with synchronization circuit. This results in a maximum TCF read value error of ±1.

When read/write TCF in active (high-speed, medium-speed) mode is needed, please select internal clock except for ϕw/4 before read/write.

In subactive mode, even ϕw/4 is selected as the internal clock, normal read/write TCF is possible.

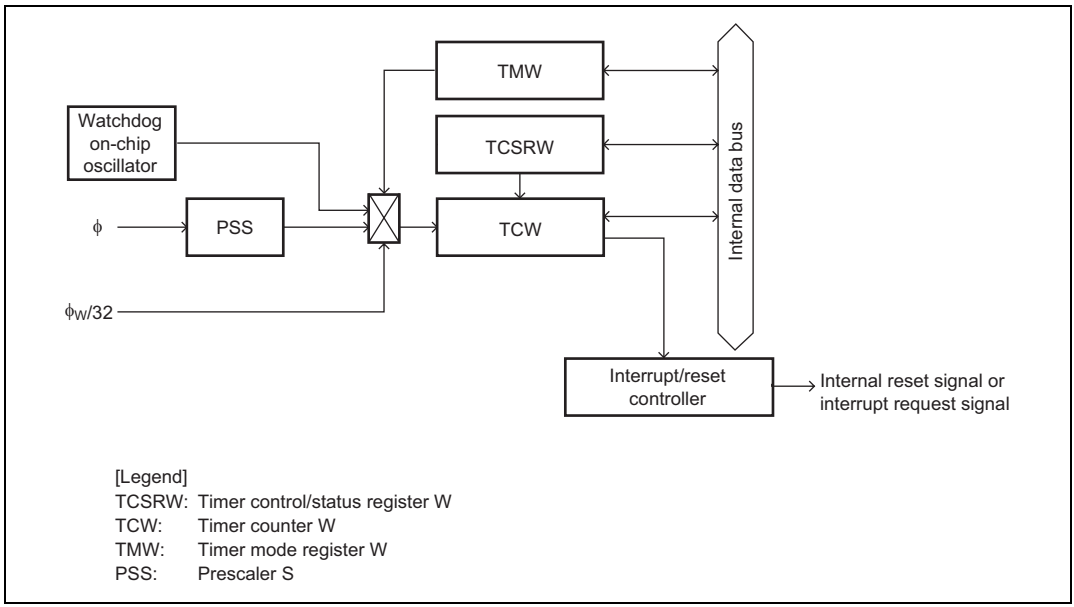


Figure 9.17(2) Block Diagram of Watchdog Timer (H8/38124 Group)

Register Configuration

Table 9.16 shows the register configuration of the watchdog timer.

Table 9.16 Watchdog Timer Registers

Name	Abbr.	R/W	Initial Value	Address
Timer control/status register W	TCSRW	R/W	H'AA	H'FFB2
Timer counter W	TCW	R/W	H'00	H'FFB3
Timer mode register W*	TMW	R/W	H'FF	H'FFF8
Clock stop register 2	CKSTPR2	R/W	H'FF	H'FFFB
Port mode register 2	PMR2	R/W	H'D8	H'FFC9

Note: * This register is implemented on the H8/38124 Group only.

Bit 7 TIE	Description	
0	Transmit data empty interrupt request (TXI) disabled	(initial value)
1	Transmit data empty interrupt request (TXI) enabled	

Bit 6—Receive Interrupt Enable (RIE)

Bit 6 selects enabling or disabling of the receive data full interrupt request (RXI) and the receive error interrupt request (ERI) when receive data is transferred from the receive shift register (RSR) to the receive data register (RDR), and bit RDRF in the serial status register (SSR) is set to 1. There are three kinds of receive error: overrun, framing, and parity.

RXI and ERI can be released by clearing bit RDRF or the FER, PER, or OER error flag to 0, or by clearing bit RIE to 0.

Bit 6 RIE	Description	
0	Receive data full interrupt request (RXI) and receive error interrupt request (ERI) disabled	(initial value)
1	Receive data full interrupt request (RXI) and receive error interrupt request (ERI) enabled	

Bit 5—Transmit Enable (TE)

Bit 5 selects enabling or disabling of the start of transmit operation.

Bit 5 TE	Description	
0	Transmit operation disabled[*1] (TXD32 pin is I/O port)	(initial value)
1	Transmit operation enabled[*2] (TXD32 pin is transmit data pin)	

Notes: 1. Bit TDRE in SSR is fixed at 1.

2. When transmit data is written to TDR in this state, bit TDRE in SSR is cleared to 0 and serial data transmission is started. Be sure to carry out serial mode register (SMR) settings, and setting of bit SPC32 in SPCR, to decide the transmission format before setting bit TE to 1.

Bits 7 to 2—Reserved/Bits 7 to 3—Reserved*

Bits 7 to 2 are reserved; they are always read as 1, and cannot be modified.

Note: * Implemented on H8/38124 Group only.

Bit 2—Output Format Select (PWCRm2)*

This bit selects the format of the output from the PWMm output pin.

This bit is write-only. Reading it always returns 1.

Bit 2 PWCRm2	Description	
0	Pulse-division PWM	(initial value)
1	Event counter PWM	

Note: * Implemented on H8/38124 Group only.

Bits 1 and 0—Clock Select 1 and 0 (PWCRm1, PWCRm0)

Bits 1 and 0 select the clock supplied to the 10-bit PWM. These bits are write-only bits; they are always read as 1.

Bit 1 PWCRm1	Bit 0 PWCRm0	Description	
0	0	The input clock is ϕ ($t\phi^* = 1/\phi$) The conversion period is 512/ϕ, with a minimum modulation width of 1/2ϕ	(initial value)
0	1	The input clock is ϕ/2 ($t\phi^* = 2/\phi$) The conversion period is 1,024/ϕ, with a minimum modulation width of 1/ϕ	
1	0	The input clock is ϕ/4 ($t\phi^* = 4/\phi$) The conversion period is 2,048/ϕ, with a minimum modulation width of 2/ϕ	
1	1	The input clock is ϕ/8 ($t\phi^* = 8/\phi$) The conversion period is 4,096/ϕ, with a minimum modulation width of 4/ϕ	

Note: * Period of PWM input clock.

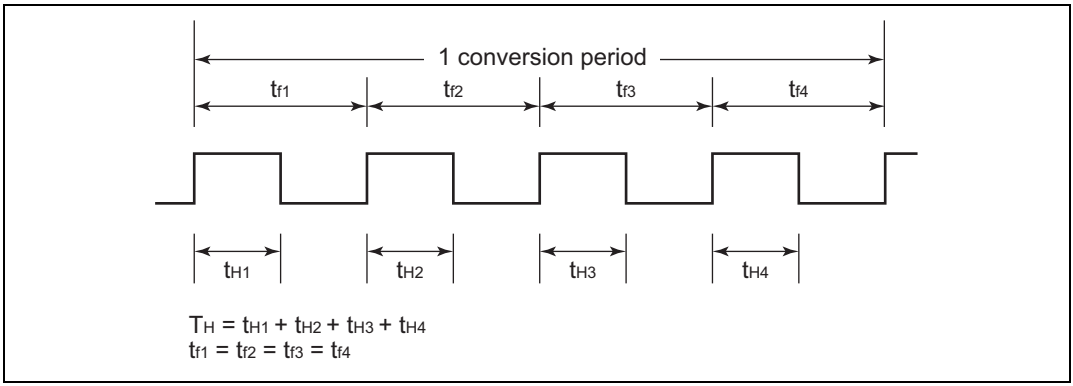


Figure 11.2 PWM Output Waveform

11.3.2 PWM Operation Modes

PWM operation modes are shown in table 11.3.

Table 11.3 PWM Operation Modes

Operation Mode	Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	Module Standby
PWCRm	Reset	Functions	Functions	Retained	Retained	Retained	Retained	Retained
PWDRUm	Reset	Functions	Functions	Retained	Retained	Retained	Retained	Retained
PWDRLm	Reset	Functions	Functions	Retained	Retained	Retained	Retained	Retained

Table 13.3 Output Levels

Data		0	0	1	1
M		**0**	**1**	**0**	**1**
Static	Common output	V_1	V_{SS}	V_1	V_{SS}
	Segment output	V_1	V_{SS}	V_{SS}	V_1
1/2 duty	Common output	V_2, V_3	V_2, V_3	V_1	V_{SS}
	Segment output	V_1	V_{SS}	V_{SS}	V_1
1/3 duty	Common output	V_3	V_2	V_1	V_{SS}
	Segment output	V_2	V_3	V_{SS}	V_1
1/4 duty	Common output	V_3	V_2	V_1	V_{SS}
	Segment output	V_2	V_3	V_{SS}	V_1

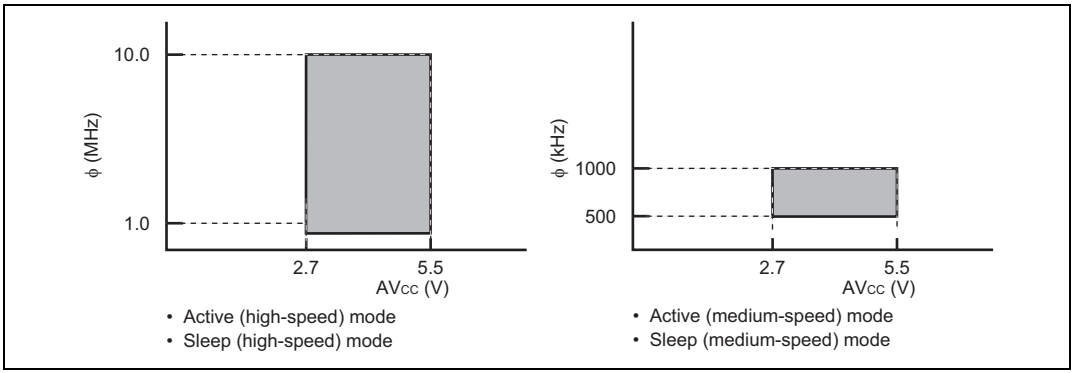
M: LCD alternation signal

13.3.3 Operation in Power-Down Modes

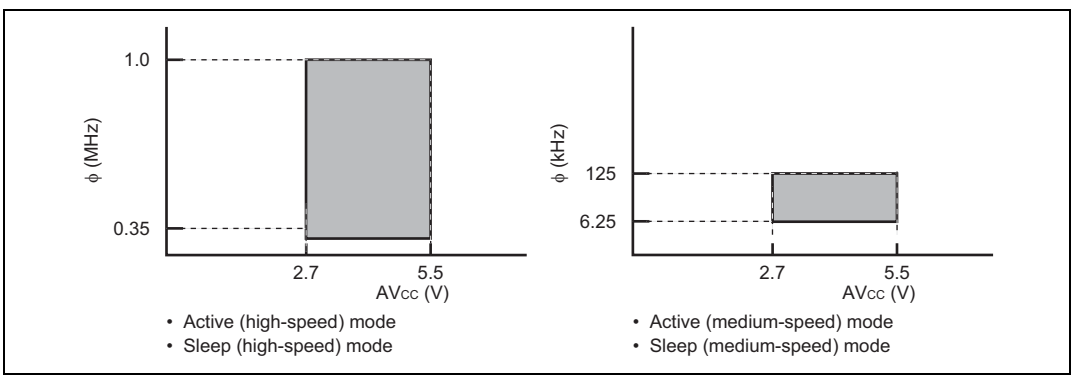
This LSI the LCD controller/driver can be operated even in the power-down modes. The operating state of the LCD controller/driver in the power-down modes is summarized in table 13.4.

In subactive mode, watch mode, and subsleep mode, the system clock oscillator stops, and therefore, unless ϕw, $\phi w/2$, or $\phi w/4$ has been selected by bits CKS3 to CKS0, the clock will not be supplied and display will halt. Since there is a possibility that a direct current will be applied to the LCD panel in this case, it is essential to ensure that ϕw, $\phi w/2$, or $\phi w/4$ is selected. In active (medium-speed) mode, the system clock is switched, and therefore CKS3 to CKS0 must be modified to ensure that the frame frequency does not change.

Analog Power Supply Voltage and A/D Converter Operating Range (System Clock Oscillator Selected)



Analog Power Supply Voltage and A/D Converter Operating Range (On-Chip Oscillator Selected)



Upper Address: H'FF

Lower Address	Register Name	Bit Names								Module Name
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'E0	PUCR1	PUCR17	PUCR16	—	PUCR14	PUCR13	—	—	—	I/O port
H'E1	PUCR3	PUCR37	PUCR36	PUCR35	PUCR34	PUCR33	PUCR32	PUCR31	PUCR30	
H'E2	PUCR5	PUCR57	PUCR56	PUCR55	PUCR54	PUCR53	PUCR52	PUCR51	PUCR50	
H'E3	PUCR6	PUCR67	PUCR66	PUCR65	PUCR64	PUCR63	PUCR62	PUCR61	PUCR60	
H'E4	PCR1	PCR17	PCR16	—	PCR14	PCR13	—	—	—	
H'E5										
H'E6	PCR3	PCR37	PCR36	PCR35	PCR34	PCR33	PCR32	PCR31	PCR30	
H'E7	PCR4	—	—	—	—	—	PCR42	PCR41	PCR40	
H'E8	PCR5	PCR57	PCR56	PCR55	PCR54	PCR53	PCR52	PCR51	PCR50	
H'E9	PCR6	PCR67	PCR66	PCR65	PCR64	PCR63	PCR62	PCR61	PCR60	
H'EA	PCR7	PCR77	PCR76	PCR75	PCR74	PCR73	PCR72	PCR71	PCR70	
H'EB	PCR8	PCR87	PCR86	PCR85	PCR84	PCR83	PCR82	PCR81	PCR80	
H'EC	PMR9	—	—	—	—	PIOFF	—	PWM2	PWM1	
H'ED	PCRA	—	—	—	—	PCRA3	PCRA2	PCRA1	PCRA0	
H'EE	PMRB	—	—	—	—	IRQ1	—	—	—	
H'EF										
H'F0	SYSCR1	SSBY	STS2	STS1	STS0	LSON	—	MA1	MA0	System control
H'F1	SYSCR2	—	—	—	NESEL	DTON	MSON	SA1	SA0	
H'F2	IEGR	—	—	—	IEG4	IEG3	—	IEG1	IEG0	
H'F3	IENR1	IENTA	—	IENWP	IEN4	IEN3	IENEC2	IEN1	IEN0	
H'F4	IENR2	IENDT	IENAD	—	IENTG	IENTFH	IENTFL	IENTC	IENEC	
H'F5	OSCCR*	SUBSTP	—	—	—	—	IRQAECF	OSCF	—	
H'F6	IRR1	IRRTA	—	—	IRRI4	IRRI3	IRREC2	IRRI1	IRRI0	
H'F7	IRR2	IRRDT	IRRAD	—	IRRTG	IRRTFH	IRRTFL	IRRTC	IRREC	
H'F8	TMW*	—	—	—	—	CKS3	CKS2	CKS1	CKS0	Watchdog timer
H'F9	IWPR	IWPF7	IWPF6	IWPF5	IWPF4	IWPF3	IWPF2	IWPF1	IWPF0	System control
H'FA	CKSTPR1	—	—	S32CKSTP	ADCKSTP	TGCKSTP	TFCKSTP	TCCKSTP	TACKSTP	
H'FB	CKSTPR2	—	—	—	PW2CKSTP	AECKSTP	WDCKSTP	PW1CKSTP	LDCKSTP	
H'FC										
H'FD										
H'FE										
H'FF										

[Legend]
SCI: Serial Communication Interface

Note: * H8/38124 only

PMR5—Port Mode Register 5 **H'CC** **I/O Port**

Bit	7	6	5	4	3	2	1	0
	WKP_7	WKP_6	WKP_5	WKP_4	WKP_3	WKP_2	WKP_1	WKP_0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

$P5_n/\overline{WKP}_n/SEG_{n+1}$ Pin Function Switch

0	Functions as $P5_n$ I/O pin
1	Functions as $\overline{WKP}_n$ input pin

(n = 7 to 0)

PWCR2—PWM2 Control Register **H'CD** **10-Bit PWM**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	PWCR22	PWCR21	PWCR20
Initial value	1	1	1	1	1	0*2	0	0
Read/Write	—	—	—	—	—	R/W	W	W

Clock Select

0	0	The input clock is ϕ ($t\phi$*1 = 1/ϕ) The conversion period is 512/ϕ, with a minimum modulation width of 1/2ϕ
	1	The input clock is ϕ/2 ($t\phi$*1 = 2/ϕ) The conversion period is 1,024/ϕ, with a minimum modulation width of 1/ϕ
1	0	The input clock is ϕ/4 ($t\phi$*1 = 4/ϕ) The conversion period is 2,048/ϕ, with a minimum modulation width of 2/ϕ
	1	The input clock is ϕ/8 ($t\phi$*1 = 8/ϕ) The conversion period is 4,096/ϕ, with a minimum modulation width of 4/ϕ

PWH Output Select (H8/38124 Group only)

0	10-bit PWM
1	Event counter PWM

Notes: 1. $t\phi$: Period of PWM2 input clock
2. 1 on products other than the H8/38124 Group