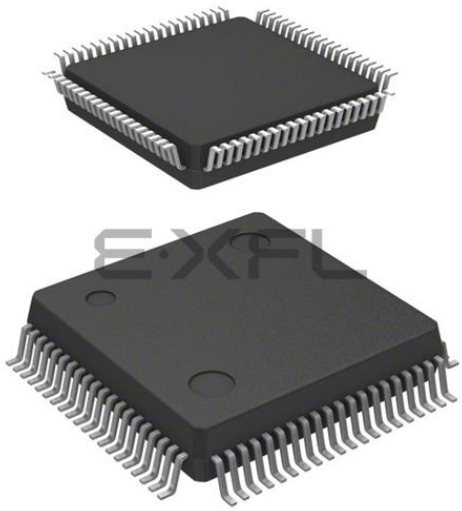

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

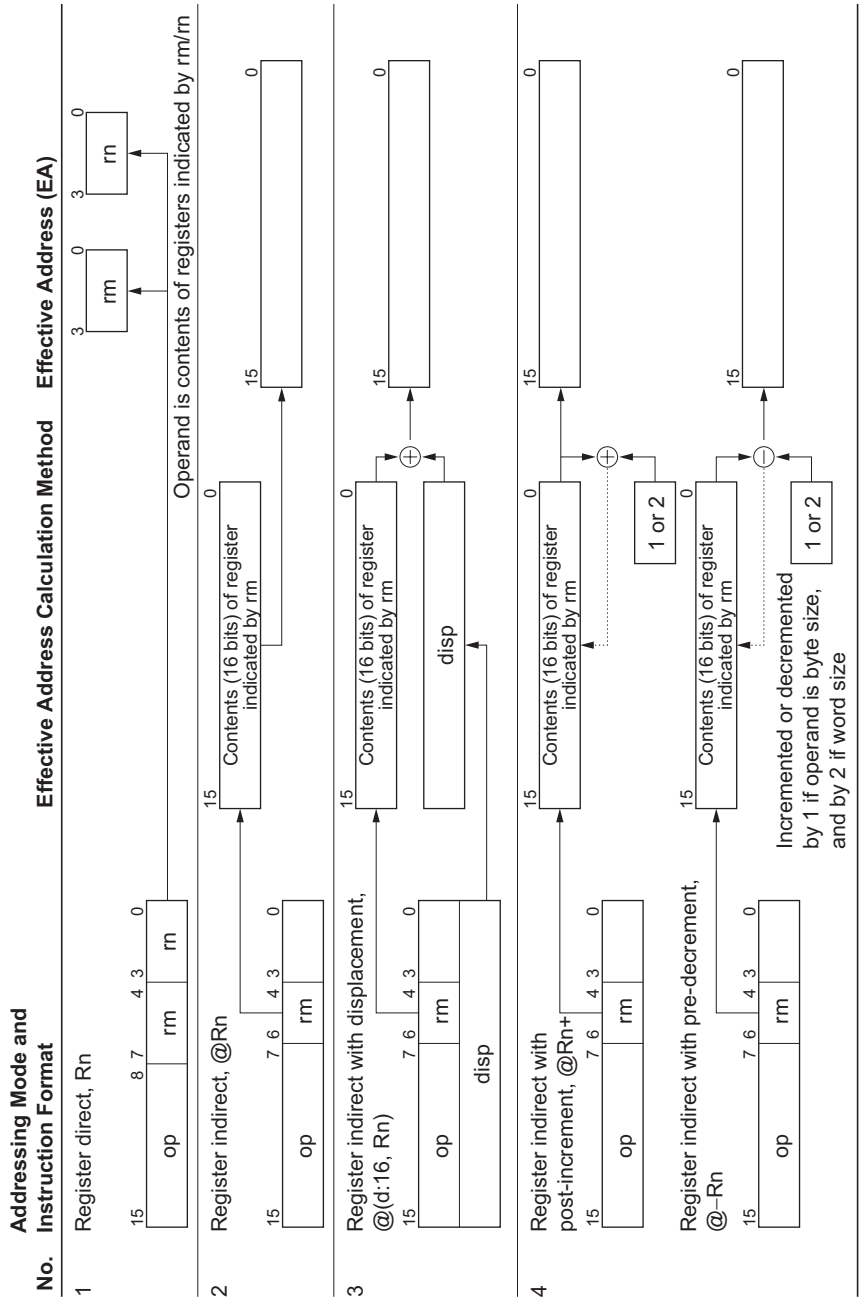
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	5MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f38024rhv

Table 1.1 Features

Item	Specification
CPU	High-speed H8/300L CPU • General-register architecture General registers: Sixteen 8-bit registers (can be used as eight 16-bit registers) • Operating speed — Max. operating speed: 8 MHz (5 MHz for HD64F38024 and H8/38024S Group) — Add/subtract: 0.25 µs (operating at 8 MHz), 0.4 µs (operating at ϕ = 5 MHz) — Multiply/divide: 1.75 µs (operating at 8 MHz), 2.8 µs (operating at ϕ = 5 MHz) — Can run on 32.768 kHz or 38.4 kHz subclock (32.768 kHz only for H8/38124 Group) • Instruction set compatible with H8/300 CPU — Instruction length of 2 bytes or 4 bytes — Basic arithmetic operations between registers — MOV instruction for data transfer between memory and registers • Typical instructions — Multiply (8 bits × 8 bits) — Divide (16 bits ÷ 8 bits) — Bit accumulator — Register-indirect designation of bit position
Interrupts	22 interrupt sources • 13 external interrupt sources (IRQ_4, IRQ_3, IRQ_1, IRQ_0, WKP_7 to WKP_0, IRQAEC) • 9 internal interrupt sources

Table 2.2 Effective Address Calculation



2.5.6 Branching Instructions

Table 2.9 describes the branching instructions. Figure 2.8 shows their object code formats.

Table 2.9 Branching Instructions

Instruction	Size	Function
Bcc	—	Branches to the designated address if condition cc is true. The branching conditions are given below.

Mnemonic	Description	Condition
BRA (BT)	Always (true)	Always
BRN (BF)	Never (false)	Never
BHI	High	$C \vee Z = 0$
BLS	Low or same	$C \vee Z = 1$
BCC (BHS)	Carry clear (high or same)	$C = 0$
BCS (BLO)	Carry set (low)	$C = 1$
BNE	Not equal	$Z = 0$
BEQ	Equal	$Z = 1$
BVC	Overflow clear	$V = 0$
BVS	Overflow set	$V = 1$
BPL	Plus	$N = 0$
BMI	Minus	$N = 1$
BGE	Greater or equal	$N \oplus V = 0$
BLT	Less than	$N \oplus V = 1$
BGT	Greater than	$Z \vee (N \oplus V) = 0$
BLE	Less or equal	$Z \vee (N \oplus V) = 1$

JMP	—	Branches unconditionally to a specified address
BSR	—	Branches to a subroutine at a specified address
JSR	—	Branches to a subroutine at a specified address
RTS	—	Returns from a subroutine

2. Bit manipulation in a register containing a write-only bit

Example 3: BCLR instruction executed designating port 3 control register PCR3

As in the examples above, $P3_7$ and $P3_6$ are input pins, with a low-level signal input at $P3_7$ and a high-level signal at $P3_6$. The remaining pins, $P3_5$ to $P3_0$, are output pins that output low-level signals. In this example, the BCLR instruction is used to change pin $P3_0$ to an input port. It is assumed that a high-level signal will be input to this input pin.

[A: Prior to executing BCLR]

	$P3_7$	**$P3_6$**	**$P3_5$**	**$P3_4$**	**$P3_3$**	**$P3_2$**	**$P3_1$**	**$P3_0$**
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	Low level
PCR3	0	0	1	1	1	1	1	1
PDR3	1	0	0	0	0	0	0	0

[B: BCLR instruction executed]

```
BCLR   #0  ,  @PCR3
```

The BCLR instruction is executed designating PCR3.

[C: After executing BCLR]

	$P3_7$	**$P3_6$**	**$P3_5$**	**$P3_4$**	**$P3_3$**	**$P3_2$**	**$P3_1$**	**$P3_0$**
Input/output	Output	Output	Output	Output	Output	Output	Output	Input
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	High level
PCR3	1	1	1	1	1	1	1	0
PDR3	1	0	0	0	0	0	0	0

[D: Explanation of how BCLR operates]

When the BCLR instruction is executed, first the CPU reads PCR3. Since PCR3 is a write-only register, the CPU reads a value of H'FF, even though the PCR3 value is actually H'3F.

Next, the CPU clears bit 0 in the read data to 0, changing the data to H'FE. Finally, this value (H'FE) is written to PCR3 and BCLR instruction execution ends.

As a result of this operation, bit 0 in PCR3 becomes 0, making $P3_0$ an input port. However, bits 7 and 6 in PCR3 change to 1, so that $P3_7$ and $P3_6$ change from input pins to output pins.

Bit 1—Timer C Interrupt Enable (IENTC)

Bit 1 enables or disables timer C overflow and underflow interrupt requests.

Bit 1 IENTC	Description	
0	Disables timer C interrupt requests	(initial value)
1	Enables timer C interrupt requests	

Bit 0—Asynchronous Event Counter Interrupt Enable (IENEC)

Bit 0 enables or disables asynchronous event counter interrupt requests.

Bit 0 IENEC	Description	
0	Disables asynchronous event counter interrupt requests	(initial value)
1	Enables asynchronous event counter interrupt requests	

For details of SCI3 interrupt control, see section 10.2.6 Serial control register 3 (SCR3).

Interrupt Request Register 1 (IRR1)

Bit	7	6	5	4	3	2	1	0
	IRRTA	—	—	IRRI4	IRRI3	IRREC2	IRRI1	IRRI0
Initial value	0	—	1	0	0	0	0	0
Read/Write	R/(W)*	W	—	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Note: * Only a write of 0 for flag clearing is possible

IRR1 is an 8-bit read/write register, in which a corresponding flag is set to 1 when a timer A, IRQAEC, IRQ_4, IRQ_3, IRQ_1, or IRQ_0 interrupt is requested. The flags are not cleared automatically when an interrupt is accepted. It is necessary to write 0 to clear each flag.

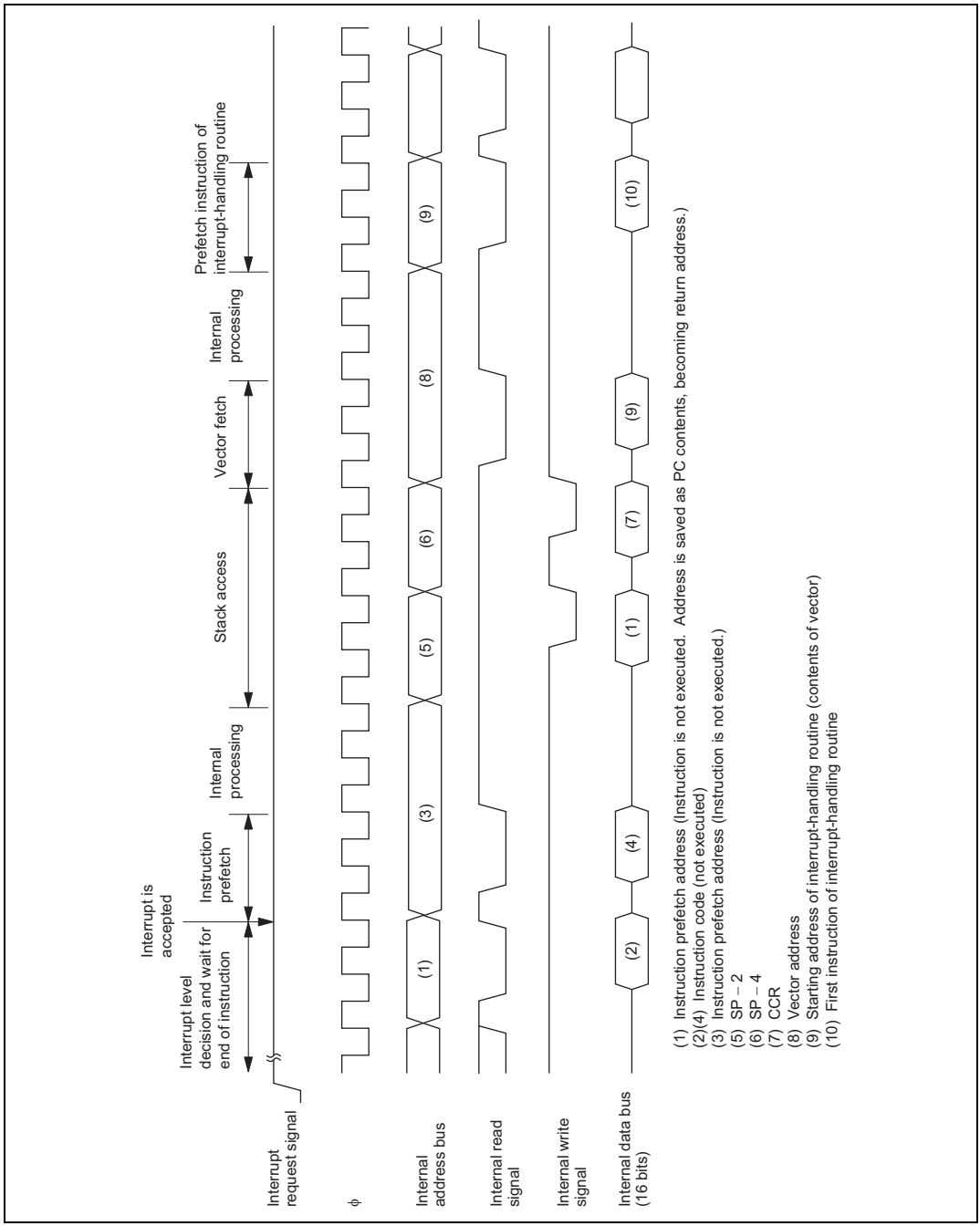


Figure 3.5 Interrupt Sequence

5.2.2 Clearing Sleep Mode

Sleep mode is cleared by any interrupt (timer A, timer C, timer F, timer G, asynchronous event counter, IRQAEC, IRQ_4, IRQ_3, IRQ_1, IRQ_0, WKP_7 to WKP_0, SCI3, A/D converter), or by input at the $\overline{RES}$ pin.

- Clearing by interrupt

  When an interrupt is requested, sleep mode is cleared and interrupt exception handling starts. A transition is made from sleep (high-speed) mode to active (high-speed) mode, or from sleep (medium-speed) mode to active (medium-speed) mode. Sleep mode is not cleared if the I bit of the condition code register (CCR) is set to 1 or the particular interrupt is disabled in the interrupt enable register.

  To synchronize the interrupt request signal with the system clock, up to 2/ϕ(s) delay may occur after the interrupt request signal occurrence, before the interrupt exception handling start.

- Clearing by $\overline{RES}$ input

  When the $\overline{RES}$ pin goes low, the CPU goes into the reset state and sleep mode is cleared.

5.2.3 Clock Frequency in Sleep (Medium-Speed) Mode

Operation in sleep (medium-speed) mode is clocked at the frequency designated by the MA1 and MA0 bits in SYSCR1.

Register Name	Bit Name		Operation
CKSTPR2	LDCKSTP	1	LCD module standby mode is cleared
		0	LCD is set to module standby mode
	PW1CKSTP	1	PWM1 module standby mode is cleared
		0	PWM1 is set to module standby mode
	WDCKSTP	1	Watchdog timer module standby mode is cleared
		0	Watchdog timer is set to module standby mode
	AECKSTP	1	Asynchronous event counter module standby mode is cleared
		0	Asynchronous event counter is set to module standby mode
	PW2CKSTP	1	PWM2 module standby mode is cleared
		0	PWM2 is set to module standby mode
	LVDCKSTP*	1	LVD module standby mode is cleared
		0	LVD is set to module standby mode

Notes: For details of module operation, see the sections on the individual modules.
* LVDCKSTP is implemented on the H8/38124 group only.

5.10 Usage Note

5.10.1 Contention Between Module Standby and Interrupts

If, due to timing with which a peripheral module issues interrupt requests, the module in question is set to module standby mode before an interrupt is processed, the module will stop with the interrupt request still pending. In this situation, interrupt processing will be repeated indefinitely unless interrupts are prohibited.

It is therefore necessary to ensure that no interrupts are generated when a module is set to module standby mode. The surest way to do this is to specify the module standby mode setting only when interrupts are prohibited (interrupts prohibited using the interrupt enable register or interrupts masked using bit CCR-1).

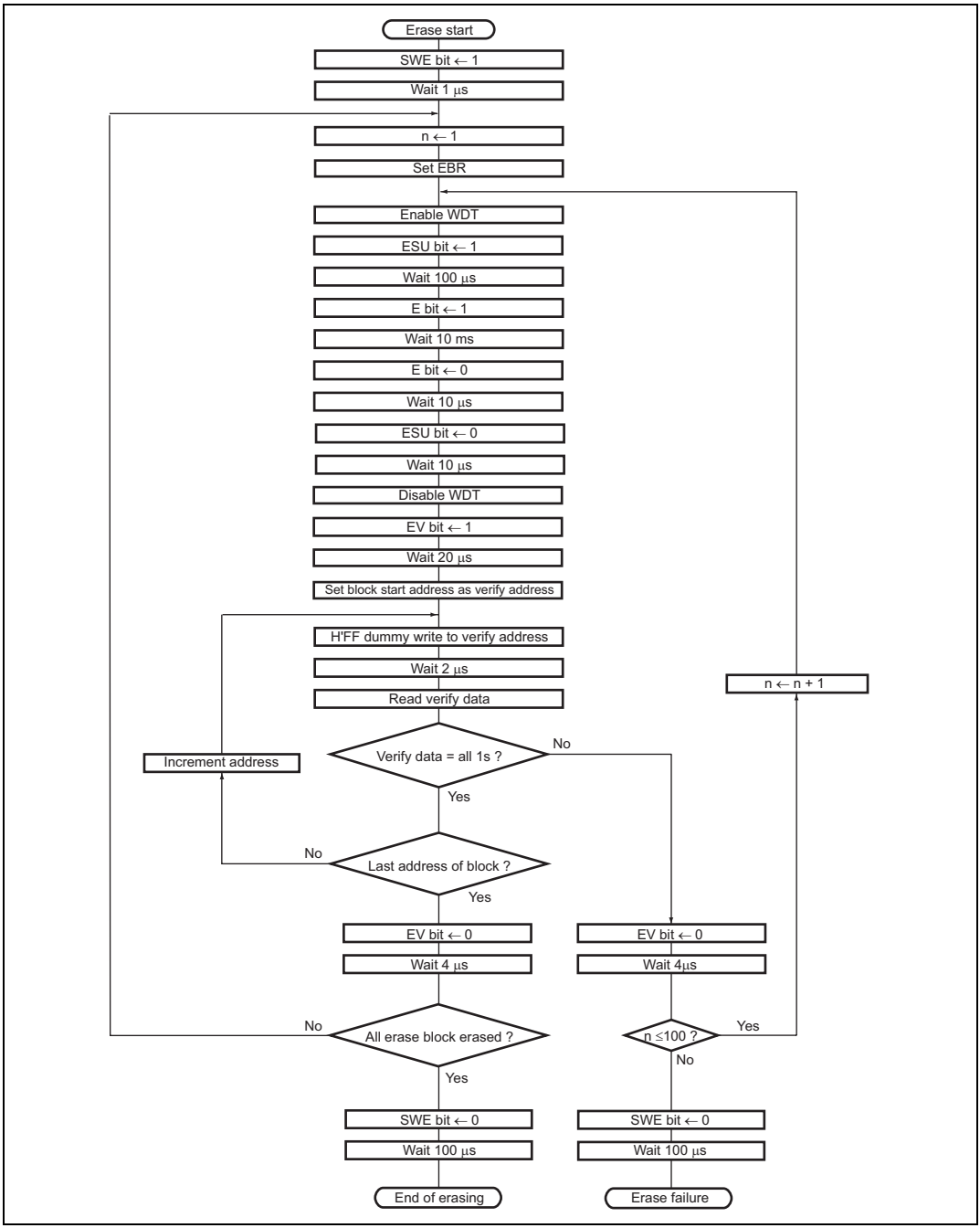


Figure 6.11 Erase/Erase-Verify Flowchart

9.4.2 Register Descriptions

16-bit Timer Counter (TCF)
8-bit Timer Counter (TCFH)
8-bit Timer Counter (TCFL)

	TCF															
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	TCFH								TCFL							

TCF is a 16-bit read/write up-counter configured by cascaded connection of 8-bit timer counters TCFH and TCFL. In addition to the use of TCF as a 16-bit counter with TCFH as the upper 8 bits and TCFL as the lower 8 bits, TCFH and TCFL can also be used as independent 8-bit counters.

TCFH and TCFL can be read and written by the CPU, but when they are used in 16-bit mode, data transfer to and from the CPU is performed via a temporary register (TEMP). For details of TEMP, see section 9.4.3, CPU Interface.

TCFH and TCFL are each initialized to H'00 upon reset.

a. 16-bit mode (TCF)

When CKSH2 is cleared to 0 in TCRF, TCF operates as a 16-bit counter. The TCF input clock is selected by bits CKSL2 to CKSL0 in TCRF.

TCF can be cleared in the event of a compare match by means of CCLRH in TCSRF.

When TCF overflows from H'FFFF to H'0000, OVFH is set to 1 in TCSRF. If OVIEH in TCSRF is 1 at this time, IRRTFH is set to 1 in IRR2, and if IENTFH in IENR2 is 1, an interrupt request is sent to the CPU.

b. 8-bit mode (TCFL/TCFH)

When CKSH2 is set to 1 in TCRF, TCFH, and TCFL operate as two independent 8-bit counters. The TCFH (TCFL) input clock is selected by bits CKSH2 to CKSH0 (CKSL2 to CKSL0) in TCRF.

TCFH (TCFL) can be cleared in the event of a compare match by means of CCLRH (CCLRL) in TCSRF.

When TCFH (TCFL) overflows from H'FF to H'00, OVFH (OVFL) is set to 1 in TCSRF. If OVIEH (OVIEL) in TCSRF is 1 at this time, IRRTFH (IRRTFL) is set to 1 in IRR2, and if IENTFH (IENTFL) in IENR2 is 1, an interrupt request is sent to the CPU.

In this example, high-level input of less than five times the width of the sampling clock at the input capture input pin is eliminated as noise.

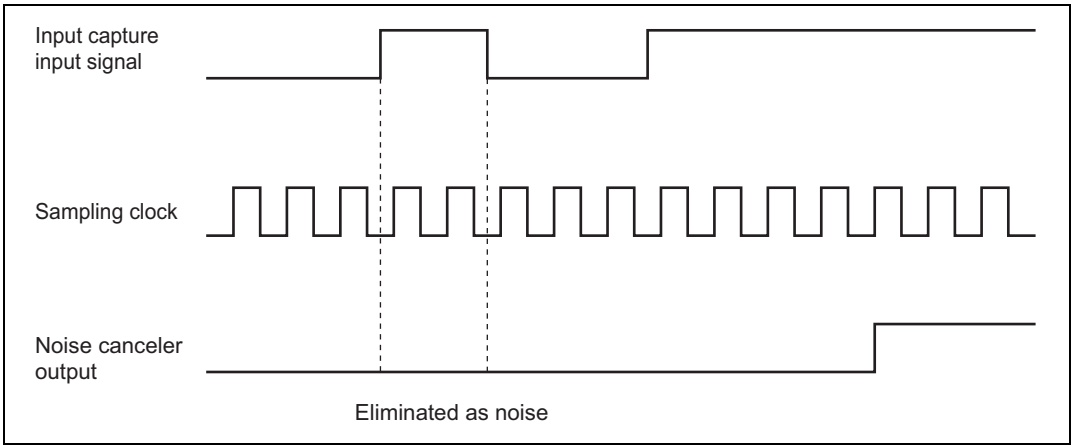


Figure 9.10 Noise Canceler Timing (Example)

Section 14 Power-On Reset and Low-Voltage Detection Circuits (H8/38124 Group Only)

14.1 Overview

This LSI can include a power-on reset circuit and low-voltage detection circuit.

The low-voltage detection circuit consists of two circuits: LVDI (interrupt by low voltage detect) and LVDR (reset by low voltage detect) circuits.

This circuit is used to prevent abnormal operation (runaway execution) from occurring due to the power supply voltage fall and to recreate the state before the power supply voltage fall when the power supply voltage rises again.

Even if the power supply voltage falls, the unstable state when the power supply voltage falls below the guaranteed operating voltage can be removed by entering standby mode* when exceeding the guaranteed operating voltage and during normal operation. Thus, system stability can be improved. If the power supply voltage falls more, the reset state is automatically entered. If the power supply voltage rises again, the reset state is held for a specified period, then active mode is automatically entered.

Figure 14.1 is a block diagram of the power-on reset circuit and the low-voltage detection circuit.

Note: * The voltage maintained in standby mode is the same as the RAM data retaining voltage (V_{RAM}). See section 16.8.2, DC Characteristics, for information on retaining voltage.

14.1.1 Features

The features of the power-on reset circuit and low-voltage detection circuit are described below.

- Power-on reset circuit

  Uses an external capacitor to generate an internal reset signal when power is first supplied.
- Low-voltage detection circuit

  LVDR: Monitors the power-supply voltage, and generates an internal reset signal when the voltage falls below a specified value.

  LVDI: Monitors the power-supply voltage, and generates an interrupt when the voltage falls below or rises above respective specified values.

16.4.2 DC Characteristics

Table 16.8 lists the DC characteristics of the HD64F38024 and HD64F38024R.

Table 16.8 DC Characteristics

V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V

			Values					
Item	**Symbol**	**Applicable Pins**	**Min**	**Typ**	**Max**	**Unit**	**Test Condition**	**Notes**
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{WKP_0}$ to $\overline{WKP_7}$, $\overline{IRQ_0}$, $\overline{IRQ_3}$, $\overline{IRQ_4}$, AEVL, AEVH, TMIC, TMIF, TMIG, $\overline{ADTRG}$, SCK_{32}	0.9 V_{CC}	—	V_{CC} + 0.3	V		
		$\overline{IRQ_1}$	0.9 V_{CC}	—	AV_{CC} + 0.3	V		
		RXD_{32}, UD	0.8 V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	0.9 V_{CC}	—	V_{CC} + 0.3	V		
		X_1	0.9 V_{CC}	—	V_{CC} + 0.3	V		
		$P1_3$, $P1_4$, $P1_6$, $P1_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_3$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, PA_0 to PA_3	0.8 V_{CC}	—	V_{CC} + 0.3	V		
		PB_0 to PB_7	0.8 V_{CC}	—	AV_{CC} + 0.3	V		
		IRQAEC, $P9_5$*5	0.9 V_{CC}	—	7.3	V		

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Active mode current dissipation	I_{OPE1}	V_{CC}	—	0.2	—	mA	Active (high-speed) mode V_{CC} = 1.8 V, f_{OSC} = 1 MHz	*1 *2 Max. guideline = 1.1 × typ.
			—	0.6	—	mA	Active (high-speed) mode V_{CC} = 3 V, f_{OSC} = 2 MHz	*1 *2 Max. guideline = 1.1 × typ.
			—	1.2	—	mA	Active (high-speed) mode V_{CC} = 3 V, f_{OSC} = 4 MHz	*1 *2 Max. guideline = 1.1 × typ.
			—	3.1	6.0	mA	Active (high-speed) mode V_{CC} = 3 V, f_{OSC} = 10 MHz	*1 *2
	I_{OPE2}	V_{CC}	—	0.03	—	mA	Active (medium-speed) mode V_{CC} = 1.8 V, f_{OSC} = 1 MHz ϕ_{osc}/128	*1 *2 Max. guideline = 1.1 × typ.
			—	0.1	—	mA	Active (medium-speed) mode V_{CC} = 3 V, f_{OSC} = 2 MHz ϕ_{osc}/128	*1 *2 Max. guideline = 1.1 × typ.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Output low voltage	V_{OL}	$P1_3$, $P1_4$, $P1_7$, $P4_0$ to $P4_2$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, PA_0 to PA_3	—	—	0.6	V	V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	
			—	—	0.5		I_{OL} = 0.4 mA	
		$P3_0$ to $P3_7$	—	—	1.0		V_{CC} = 4.0 V to 5.5 V I_{OL} = 10 mA	
			—	—	0.6		V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	
			—	—	0.5		I_{OL} = 0.4 mA	
		$P9_0$ to $P9_5$	—	—	1.5		V_{CC} = 4.0 V to 5.5 V I_{OL} = 15 mA	
			—	—	1.0		V_{CC} = 4.0 V to 5.5 V I_{OL} = 10 mA	
			—	—	0.8		V_{CC} = 4.0 V to 5.5 V I_{OL} = 8 mA	
			—	—	1.0		I_{OL} = 5 mA	
			—	—	0.6		I_{OL} = 1.6 mA	
			—	—	0.5		I_{OL} = 0.4 mA	
Input/ output leakage current	$\lvert I_{IL} \rvert$	$\overline{RES}$, $P4_3$, $P1_3$, $P1_4$, $P1_7$, OSC_1, X_1, $P3_0$ to $P3_7$, $P4_0$ to $P4_2$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, IRQAEC, PA_0 to PA_3, $P9_0$ to $P9_5$	—	—	1.0	µA	V_{IN} = 0.5 V to V_{CC} – 0.5 V	
		PB_0 to PB_7	—	—	1.0		V_{IN} = 0.5 V to AV_{CC} – 0.5 V	
Pull-up MOS current	$-I_p$	$P1_3$, $P1_4$, $P1_7$, $P3_0$ to $P3_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$	20	—	200	µA	V_{CC} = 5.0 V, V_{IN} = 0.0 V	
			—	40	—		V_{CC} = 2.7 V, V_{IN} = 0.0 V	Reference value

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Subsleep mode current consumption	I_{SUBSP}	V_{CC}	—	4.0	16	µA	V_{CC} = 2.7 V, LCD on, 32-kHz crystal resonator used ($\phi_{SUB} = \phi_W/2$)	*3 *4
Watch mode current consumption	I_{WATCH}	V_{CC}	—	1.4	—	µA	V_{CC} = 2.7 V, T_a = 25°C, 32-kHz crystal resonator used, LCD not used	*1 *3 *4 Reference value
			—	1.8	—			*2 *3 *4 Reference value
			—	1.8	6.0		V_{CC} = 2.7 V, 32-kHz crystal resonator used, LCD not used	*3 *4
Standby mode current consumption	I_{STBY}	V_{CC}	—	0.3	—	µA	V_{CC} = 2.7 V, T_a = 25°C, 32-kHz crystal resonator not used	*1 *3 *4 Reference value
			—	0.5	—		V_{CC} = 2.7 V, T_a = 25°C, 32-kHz crystal resonator not used	*2 *3 *4 Reference value
			—	0.05	—		V_{CC} = 2.7 V, T_a = 25°C, SUBSTP (subclock oscillator control register) setting = 1	*2 *4 Reference value
			—	0.6	—		V_{CC} = 5.0 V, T_a = 25°C, 32-kHz crystal resonator not used	*2 *3 *4 Reference value
			—	0.16	—		V_{CC} = 5.0 V, T_a = 25°C, SUBSTP (subclock oscillator control register) setting = 1	*2 *4 Reference value
			—	1.0	5.0		32-kHz crystal resonator not used	*3 *4
RAM data retaining voltage	V_{RAM}	V_{CC}	2.0	—	—	V		*6

TMG—Timer Mode Register G

H'BC

Timer G

Bit	7	6	5	4	3	2	1	0
	OVFH	OVFL	OVIE	IIEGS	CCLR1	CCLR0	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select

0	0	Internal clock: counting on ϕ/64
	1	Internal clock: counting on ϕ/32
1	0	Internal clock: counting on ϕ/2
	1	Internal clock: counting on ϕ_W/4

Counter Clear

0	0	TCG clearing is disabled
	1	TCG cleared by falling edge of input capture input signal
1	0	TCG cleared by rising edge of input capture input signal
	1	TCG cleared by both edges of input capture input signal

Input Capture Interrupt Edge Select

0	Interrupt generated on rising edge of input capture input signal
1	Interrupt generated on falling edge of input capture input signal

Timer Overflow Interrupt Enable

0	TCG overflow interrupt request is disabled
1	TCG overflow interrupt request is enabled

Timer Overflow Flag L

0	Clearing condition: After reading OVFL = 1, cleared by writing 0 to OVFL
1	Setting condition: Set when TCG overflows from H'FF to H'00

Timer Overflow Flag H

0	Clearing condition: After reading OVFH = 1, cleared by writing 0 to OVFH
1	Setting condition: Set when TCG overflows from H'FF to H'00

Note: * Bits 7 and 6 can only be written with 0, for flag clearing.

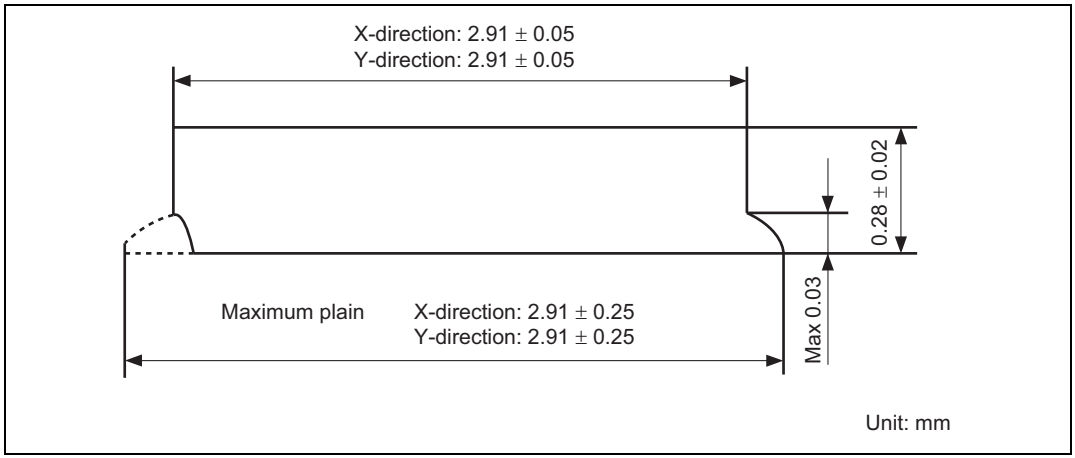


Figure G.3 Chip Sectional Figure of the HCD64338024S, HCD64338023S, HCD64338022S, HCD64338021S, and HCD64338020S