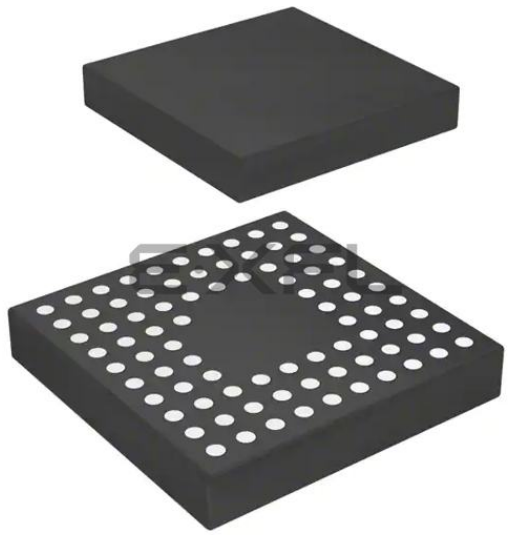

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Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
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User's Manual

8

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H8/38024, H8/38024S, H8/38024R, H8/38124 Group

Hardware Manual
Renesas 8-Bit Single-Chip Microcomputer
H8 Family/H8/300L Super Low Power Series

H8/38024 Group	H8/38024	H8/38024R Group	H8/38024R
	H8/38023		
	H8/38022	H8/38124 Group	H8/38124
	H8/38021		H8/38123
	H8/38020		H8/38122
H8/38024S Group	H8/38024S		H8/38121
	H8/38022S		H8/38120
	H8/38021S		
	H8/38020S		
	H8/38000S		

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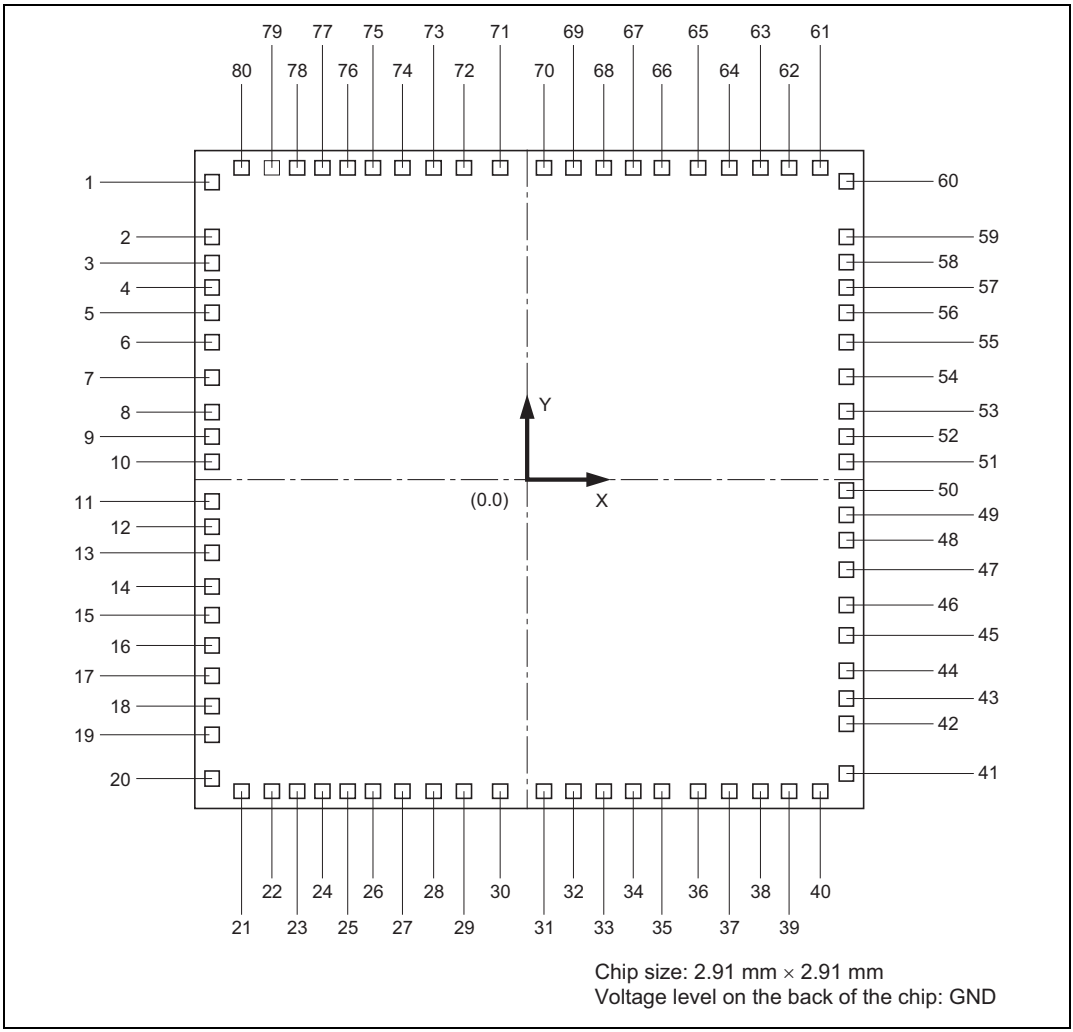


Figure 1.7 Bonding Pad Location Diagram of HCD64338024S, HCD64338023S, HCD64338022S, HCD64338021S, and HCD64338020S (Top View)

1.3.2 Pin Functions

Table 1.5 outlines the pin functions of the H8/38024 Group.

Table 1.5 Pin Functions

		Pin No.							
Type	**Symbol**	**FP-80A TFP-80C**	**FP-80B**	**TLP-85V**	**Pad No.*1**	**Pad No.*2**	**Pad No.*3**	**I/O**	**Name and Functions**
Power source pins	V_{CC}	52	54	E8	53	54	52	Input	**Power supply:** All V_{CC} pins should be connected to the system power supply.
	V_{SS}	8 (= AV_{SS}) 53	10 (= AV_{SS}) 55	D8 E1 (= AV_{SS})	9 54	10 55	8 53	Input	**Ground:** All V_{SS} pins should be connected to the system power supply (0 V).
	AV_{CC}	1	3	B1	1	2	1	Input	**Analog power supply:** This is the power supply pin for the A/D converter. When the A/D converter is not used, connect this pin to the system power supply.
	AV_{SS}	8 (= V_{SS})	10 (= V_{SS})	E1 (= V_{SS})	8	9	8	Input	**Analog ground:** This is the A/D converter ground pin. It should be connected to the system power supply (0V).
	V_1 V_2 V_3	51 50 49	53 52 51	F9 E9 F8	52 51 50	53 52 51	51 50 49	Input	**LCD power supply:** These are the power supply pins for the LCD controller/driver.
	CV_{CC}*4	4	—	—	—	—	—	Input	**Power supply:** This is the internal step-down power supply pin. To ensure stability, a capacitor with a rating of about 0.1 µF should be connected between this pin and the V_{SS} pin.

Register Indirect with Post-Increment or Pre-Decrement—@Rn+ or @–Rn:

- Register indirect with post-increment—@Rn+

  The @Rn+ mode is used with MOV instructions that load registers from memory.

  The register field of the instruction specifies a 16-bit general register containing the address of the operand. After the operand is accessed, the register is incremented by 1 for MOV.B or 2 for MOV.W. For MOV.W, the original contents of the 16-bit general register must be even.
- Register indirect with pre-decrement—@–Rn

  The @–Rn mode is used with MOV instructions that store register contents to memory.

  The register field of the instruction specifies a 16-bit general register which is decremented by 1 or 2 to obtain the address of the operand in memory. The register retains the decremented value. The size of the decrement is 1 for MOV.B or 2 for MOV.W. For MOV.W, the original contents of the register must be even.

Absolute Address—@aa:8 or @aa:16: The instruction specifies the absolute address of the operand in memory.

The absolute address may be 8 bits long (@aa:8) or 16 bits long (@aa:16). The MOV.B and bit manipulation instructions can use 8-bit absolute addresses. The MOV.B, MOV.W, JMP, and JSR instructions can use 16-bit absolute addresses.

For an 8-bit absolute address, the upper 8 bits are assumed to be 1 (H'FF). The address range is H'FF00 to H'FFFF (65280 to 65535).

Immediate—#xx:8 or #xx:16: The instruction contains an 8-bit operand (#xx:8) in its second byte, or a 16-bit operand (#xx:16) in its third and fourth bytes. Only MOV.W instructions can contain 16-bit immediate values.

The ADDS and SUBS instructions implicitly contain the value 1 or 2 as immediate data. Some bit manipulation instructions contain 3-bit immediate data in the second or fourth byte of the instruction, specifying a bit number.

Program-Counter Relative—@(d:8, PC): This mode is used in the Bcc and BSR instructions. An 8-bit displacement in byte 2 of the instruction code is sign-extended to 16 bits and added to the program counter contents to generate a branch destination address. The possible branching range is –126 to +128 bytes (–63 to +64 words) from the current address. The displacement should be an even number.

Memory Indirect—@@aa:8: This mode can be used by the JMP and JSR instructions. The second byte of the instruction code specifies an 8-bit absolute address. The word located at this address contains the branch destination address.

8.10.4 Pin States

Table 8.28 shows the port A pin states in each operating mode.

Table 8.28 Port A Pin States

Pins	Reset	Sleep	Subsleep	Standby	Watch	Subactive	Active
PA_3/COM_4 PA_2/COM_3 PA_1/COM_2 PA_0/COM_1	High-impedance	Retains previous state	Retains previous state	High-impedance	Retains previous state	Functional	Functional

Bits 3 to 0—Internal Clock Select (TMA3 to TMA0)

Bits 3 to 0 select the clock input to TCA. The selection is made as follows.

				Description	
Bit 3 TMA3	**Bit 2 TMA2**	**Bit 1 TMA1**	**Bit 0 TMA0**	**Prescaler and Divider Ratio or Overflow Period**	**Function**
0	0	0	0	PSS, ϕ/8192 (initial value)	Interval timer
			1	PSS, ϕ/4096	
		1	0	PSS, ϕ/2048	
			1	PSS, ϕ/512	
	1	0	0	PSS, ϕ/256	
			1	PSS, ϕ/128	
		1	0	PSS, ϕ/32	
			1	PSS, ϕ/8	
1	0	0	0	PSW, 1 s	Clock time
			1	PSW, 0.5 s	base
		1	0	PSW, 0.25 s	(when using
			1	PSW, 0.03125 s	32.768 kHz)
	1	0	0	PSW and TCA are reset	
			1		
		1	0		
			1		

10.1.2 Block Diagram

Figure 10.1 shows a block diagram of SCI3.

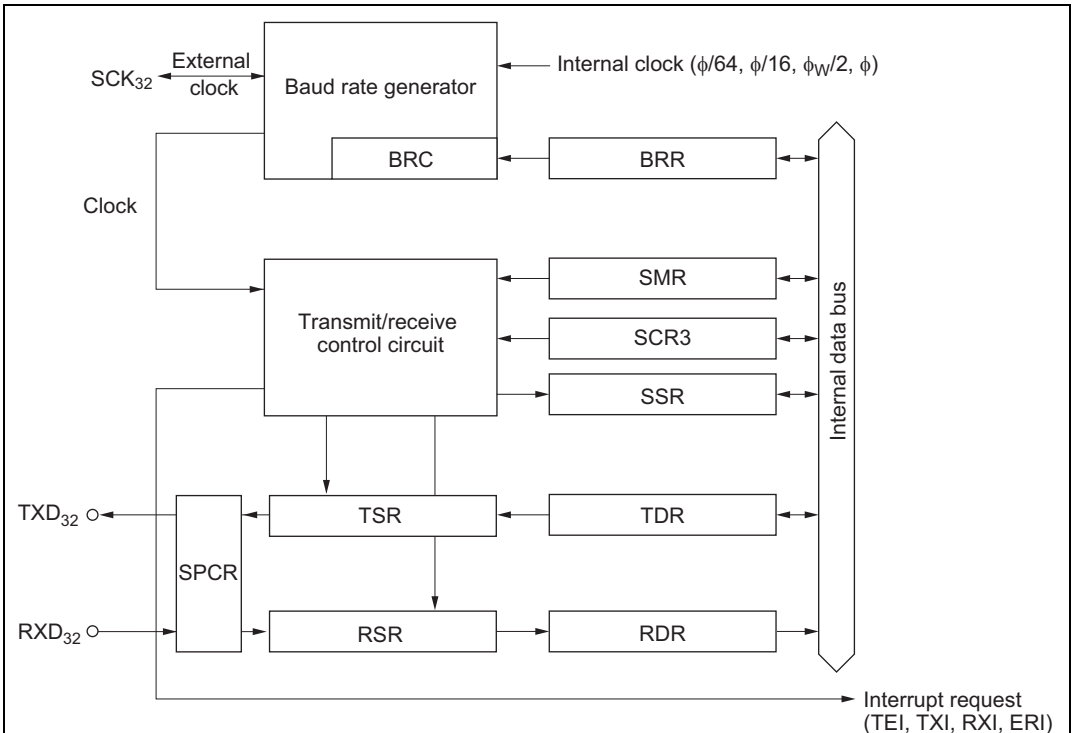


Figure 10.1 SCI3 Block Diagram

- Simultaneous transmit/receive

Figure 10.15 shows an example of a flowchart for a simultaneous transmit/receive operation. This procedure should be followed for simultaneous transmission/reception after initializing SCI3.

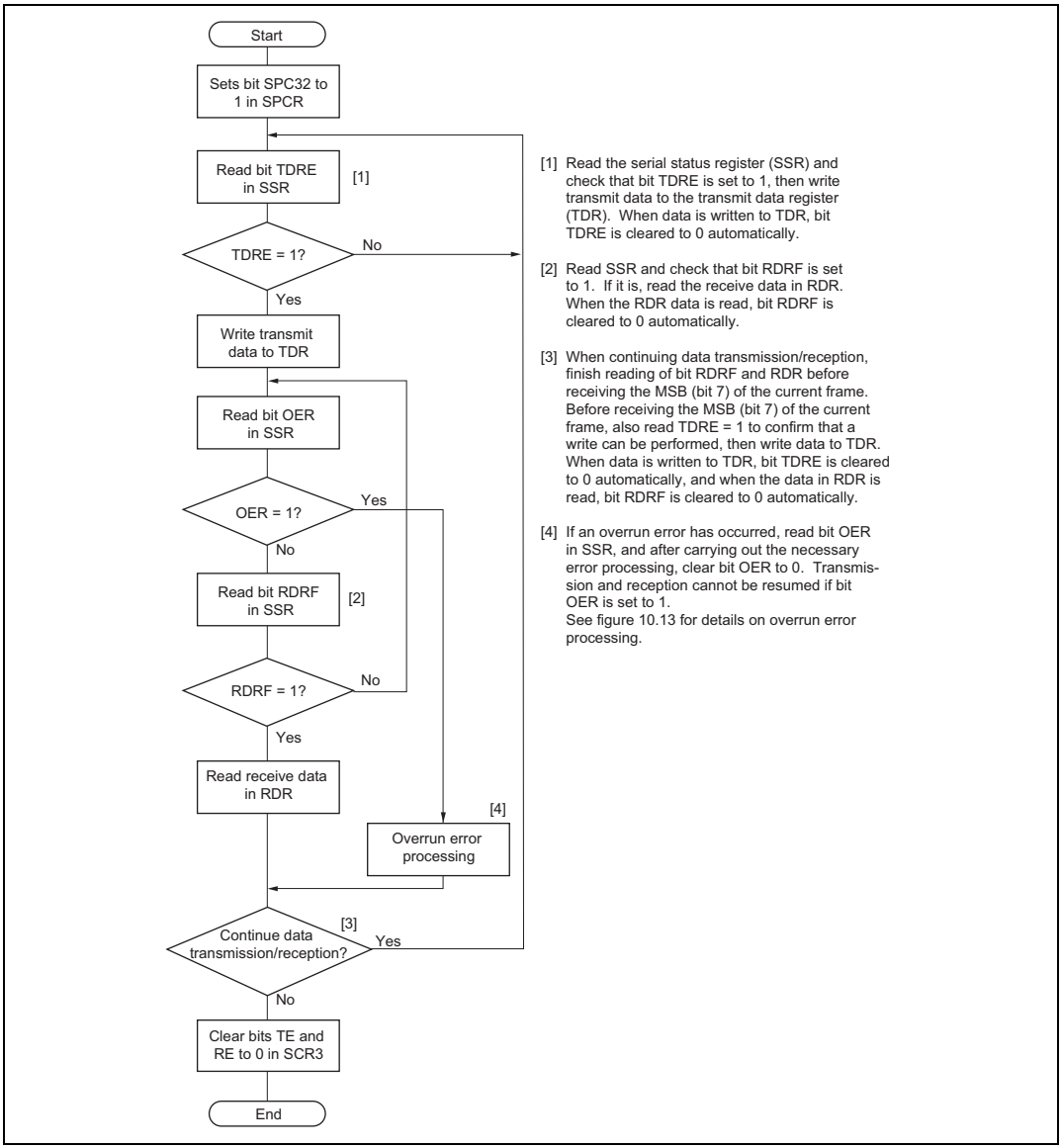


Figure 10.15 Example of Simultaneous Data Transmission/Reception Flowchart (Synchronous Mode)

15.2 When Not Using Internal Power Supply Step-Down Circuit

When the internal power supply step-down circuit is not used, connect the external power supply to the CV_{CC} pin and V_{CC} pin, as shown in figure 15.2. The external power supply is then input directly to the internal power supply. The permissible range for the power supply voltage is 2.7 V to 3.6 V. Operation cannot be guaranteed if a voltage outside this range (less than 3.0 V or more than 3.6 V) is input.

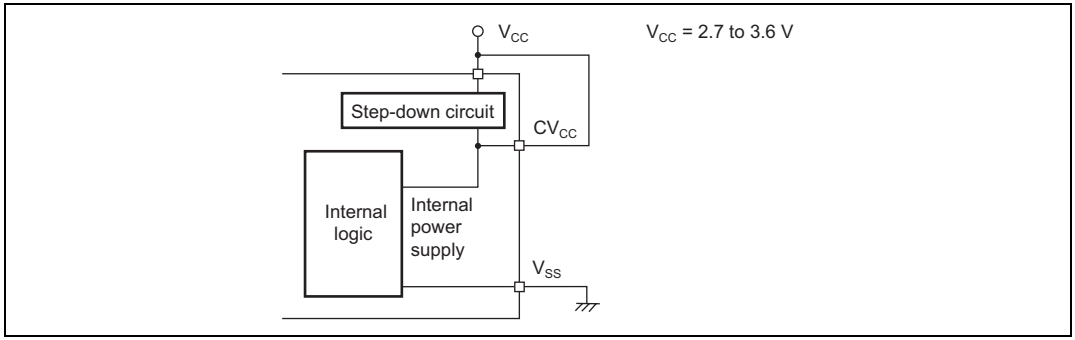
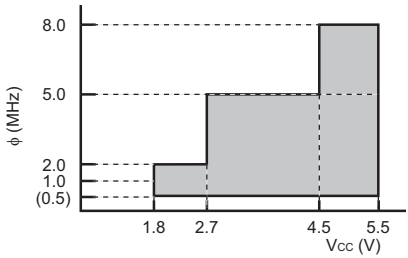


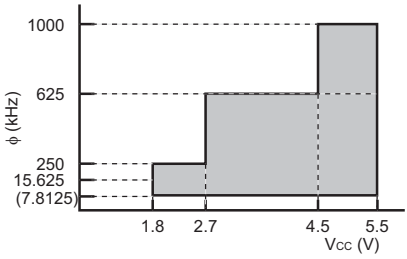
Figure 15.2 Power Supply Connection when Internal Step-Down Circuit is Not Used

Power Supply Voltage and Operating Frequency Range



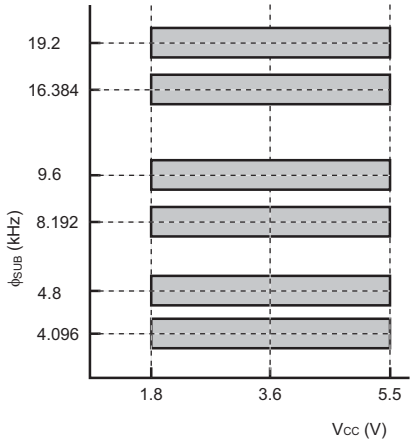
- Active (high-speed) mode
- Sleep (high-speed) mode (except CPU)

Note: 1. The figure in parentheses is the minimum operating frequency when an external clock is input. When using an oscillator, the minimum operating frequency (ϕ) is 1 MHz.



- Active (medium-speed) mode
- Sleep (medium-speed) mode (except A/D converter)

Note: 2. The figure in parentheses is the minimum operating frequency when an external clock is input. When using an oscillator, the minimum operating frequency (ϕ) is 15.625 kHz.



- Subactive mode
- Subsleep mode (except CPU)
- Watch mode (except CPU)

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Output low voltage	V_{OL}	$P1_3$, $P1_4$, $P1_6$, $P1_7$, $P4_0$ to $P4_2$	—	—	0.6	V	V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	
			—	—	0.5		I_{OL} = 0.4 mA	
		$P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, PA_0 to PA_3	—	—	0.5		I_{OL} = 0.4 mA	
		$P3_0$ to $P3_7$	—	—	1.5		V_{CC} = 4.0 V to 5.5 V I_{OL} = 10 mA	
			—	—	0.6		V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	
			—	—	0.5		I_{OL} = 0.4 mA	
		$P9_0$ to $P9_2$	—	—	0.5		V_{CC} = 2.2 to 5.5 V I_{OL} = 25 mA	*5
							I_{OL} = 15 mA	
			—	—	0.5		I_{OL} = 10 mA	*6
		$P9_3$ to $P9_5$	—	—	0.5		I_{OL} = 10 mA	
Input/output leakage current	$\lvert I_{IL} \rvert$	$\overline{RES}$, $P4_3$	—	—	20.0	µA	V_{IN} = 0.5 V to V_{CC} – 0.5 V	*2
			—	—	1.0			*1
		OSC_1, X_1, $P1_3$, $P1_4$, $P1_6$, $P1_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_2$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, IRQAEC, $P9_0$ to $P9_5$, PA_0 to PA_3	—	—	1.0	µA	V_{IN} = 0.5 V to V_{CC} – 0.5 V	
		PB_0 to PB_7	—	—	1.0		V_{IN} = 0.5 V to AV_{CC} – 0.5 V	

16.4.3 AC Characteristics

Table 16.9 lists the control signal timing, and tables 16.10 lists the serial interface timing of the H8/38024F.

Table 16.9 Control Signal Timing

V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Reference Figure
System clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	2.0	—	10.0	MHz		
OSC clock (ϕ_{OSC}) cycle time	t_{OSC}	OSC_1, OSC_2	100	—	500 (1000)	ns		Figure 16.2 *2
System clock (ϕ) cycle time	t_{cyc}		2	—	128	t_{OSC}		
			—	—	128	µs		
Subclock oscillation frequency	f_W	X_1, X_2	—	32.768 or 38.4	—	kHz		
Watch clock (ϕ_W) cycle time	t_W	X_1, X_2	—	30.5 or 26.0	—	µs		Figure 16.2
Subclock (ϕ_{SUB}) cycle time	t_{subcyc}		2	—	8	t_W		*1
Instruction cycle time			2	—	—	t_{cyc} t_{subcyc}		
Oscillation stabilization time	t_{rc}	OSC_1, OSC_2	—	0.8	2.0	ms	Figure 16.10 (crystal oscillator)	Figure 16.10 *3
			—	2.0	6.0	ms	Figure 16.9 (crystal oscillator)	Figure 16.9 *4
			—	20	45	µs	Figure 16.10 (ceramic oscillator)	Figure 16.10 *3
			—	20	45	µs	Figure 16.9 (ceramic oscillator)	Figure 16.9 *4
			—	—	50	ms	Except the above	
		X_1, X_2	—	—	2.0	s		

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Active mode current dissipation	I_{OPE1}	V_{CC}	—	0.2	—	mA	Active (high-speed) mode V_{CC} = 1.8 V, f_{OSC} = 1 MHz	*1 *2 Max. guideline = 1.1 × typ.
			—	0.6	—	mA	Active (high-speed) mode V_{CC} = 3 V, f_{OSC} = 2 MHz	*1 *2 Max. guideline = 1.1 × typ.
			—	1.2	—	mA	Active (high-speed) mode V_{CC} = 3 V, f_{OSC} = 4 MHz	*1 *2 Max. guideline = 1.1 × typ.
			—	3.1	6.0	mA	Active (high-speed) mode V_{CC} = 3 V, f_{OSC} = 10 MHz	*1 *2
	I_{OPE2}	V_{CC}	—	0.03	—	mA	Active (medium-speed) mode V_{CC} = 1.8 V, f_{OSC} = 1 MHz ϕ_{osc}/128	*1 *2 Max. guideline = 1.1 × typ.
			—	0.1	—	mA	Active (medium-speed) mode V_{CC} = 3 V, f_{OSC} = 2 MHz ϕ_{osc}/128	*1 *2 Max. guideline = 1.1 × typ.

Table 16.18 Serial Interface (SCI3) Timing

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V

Item		Symbol	Values			Unit	Test Conditions	Reference Figure
			Min	Typ	Max			
Input clock cycle	Asynchronous	t_{scyc}	4	—	—	t_{cyc} or t_{subcyc}		Figure 16.5
	Synchronous		6	—	—			
Input clock pulse width		t_{SCKW}	0.4	—	0.6	t_{scyc}		Figure 16.5
Transmit data delay time (synchronous)		t_{TXD}	—	—	1	t_{cyc} or t_{subcyc}		Figure 16.6
Receive data setup time (synchronous)		t_{RXS}	400.0	—	—	ns		Figure 16.6
Receive data hold time (synchronous)		t_{RXH}	400.0	—	—	ns		Figure 16.6

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
MOV	MOV.W Rs, @Rd	1				1	
	MOV.W Rs, @(d:16, Rd)	2				1	
	MOV.W Rs, @–Rd	1				1	2
	MOV.W Rs, @aa:16	2				1	
MULXU	MULXU.B Rs, Rd	1					12
NEG	NEG.B Rd	1					
NOP	NOP	1					
NOT	NOT.B Rd	1					
OR	OR.B #xx:8, Rd	1					
	OR.B Rs, Rd	1					
ORC	ORC #xx:8, CCR	1					
ROTL	ROTL.B Rd	1					
ROTR	ROTR.B Rd	1					
ROTXL	ROTXL.B Rd	1					
ROTXR	ROTXR.B Rd	1					
RTE	RTE	2		2			2
RTS	RTS	2		1			2
SHAL	SHAL.B Rd	1					
SHAR	SHAR.B Rd	1					
SHLL	SHLL.B Rd	1					
SHLR	SHLR.B Rd	1					
SLEEP	SLEEP	1					
STC	STC CCR, Rd	1					
SUB	SUB.B Rs, Rd	1					
	SUB.W Rs, Rd	1					
SUBS	SUBS.W #1, Rd	1					
	SUBS.W #2, Rd	1					
POP	POP Rd	1		1			2
PUSH	PUSH Rs	1		1			2
SUBX	SUBX.B #xx:8, Rd	1					
	SUBX.B Rs, Rd	1					
XOR	XOR.B #xx:8, Rd	1					
	XOR.B Rs, Rd	1					
XORC	XORC #xx:8, CCR	1					

TCSRF—Timer Control/Status Register F H'B7 Timer F

Bit	7	6	5	4	3	2	1	0
	OVFH	CMFH	OVIEH	CCLRH	OVFL	CMFL	OVIEL	CCLRL
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/W	R/W	R/(W)*	R/(W)*	R/W	R/W

Counter Clear L

0	TCFL clearing by compare match is disabled
1	TCFL clearing by compare match is enabled

Timer Overflow Interrupt Enable L

0	TCFL overflow interrupt request is disabled
1	TCFL overflow interrupt request is enabled

Compare Match Flag L

0	Clearing condition: After reading CMFL = 1, cleared by writing 0 to CMFL
1	Setting condition: Set when the TCFL value matches the OCRFL value

Timer Overflow Flag L

0	Clearing condition: After reading OVFL = 1, cleared by writing 0 to OVFL
1	Setting condition: Set when TCFL overflows from H'FF to H'00

Counter Clear H

0	16-bit mode: TCF clearing by compare match is disabled 8-bit mode: TCFH clearing by compare match is disabled
1	16-bit mode: TCF clearing by compare match is enabled 8-bit mode: TCFH clearing by compare match is enabled

Timer Overflow Interrupt Enable H

0	TCFH overflow interrupt request is disabled
1	TCFH overflow interrupt request is enabled

Compare Match Flag H

0	Clearing condition: After reading CMFH = 1, cleared by writing 0 to CMFH
1	Setting condition: Set when the TCFH value matches the OCRFH value

Timer Overflow Flag H

0	Clearing condition: After reading OVFH = 1, cleared by writing 0 to OVFH
1	Setting condition: Set when TCFH overflows from H'FF to H'00

Note: * Bits 7, 6, 3, and 2 can only be written with 0, for flag clearing.

Appendix D Port States in the Different Processing States

Table D.1 Port States Overview

Port	Reset	Sleep	Subsleep	Standby	Watch	Subactive	Active
$P1_7$, $P1_6$*3, $P1_4$, $P1_3$	High impedance	Retained	Retained	High impedance*1	Retained	Functions	Functions
$P3_7$ to $P3_0$	High impedance	Retained	Retained	High impedance*1	Retained	Functions	Functions
$P4_3$ to $P4_0$	High impedance	Retained	Retained	High impedance	Retained	Functions	Functions
$P5_7$ to $P5_0$	High impedance	Retained	Retained	High impedance*1 *2	Retained	Functions	Functions
$P6_7$ to $P6_0$	High impedance	Retained	Retained	High impedance*1	Retained	Functions	Functions
$P7_7$ to $P7_0$	High impedance	Retained	Retained	High impedance	Retained	Functions	Functions
$P8_7$ to $P8_0$	High impedance	Retained	Retained	High impedance	Retained	Functions	Functions
$P9_5$ to $P9_0$	High impedance	Retained	Retained	High impedance*1	Retained	Functions	Functions
PA_3 to PA_0	High impedance	Retained	Retained	High impedance	Retained	Functions	Functions
PB_7 to PB_0	High impedance	High impedance	High impedance	High impedance	High impedance	High impedance	High impedance

Notes: 1. High level output when MOS pull-up is in on state.
2. In the HD64F38024 the previous pin state is retained.
3. Not implemented on H8/38124 Group.

Product Type				Part No.	Mark Code	Package (Package Code)
H8/38024 Group	H8/38023	Mask ROM versions	Regular specifications	HD64338023H	HD64338023(***)H	80-pin QFP (FP-80A)
				HD64338023F	HD64338023(***)F	80-pin QFP (FP-80B)
				HD64338023W	HD64338023(***)W	80-pin TQFP (TFP-80C)
				HCD64338023	—	Die
			Wide-range specifications	HD64338023D	HD64338023(***)H	80-pin QFP (FP-80A)
				HD64338023E	HD64338023(***)F	80-pin QFP (FP-80B)
				HD64338023WI	HD64338023(***)W	80-pin TQFP (TFP-80C)
	H8/38022	Mask ROM versions	Regular specifications	HD64338022H	HD64338022(***)H	80-pin QFP (FP-80A)
				HD64338022F	HD64338022(***)F	80-pin QFP (FP-80B)
				HD64338022W	HD64338022(***)W	80-pin TQFP (TFP-80C)
				HCD64338022	—	Die
			Wide-range specifications	HD64338022D	HD64338022(***)H	80-pin QFP (FP-80A)
				HD64338022E	HD64338022(***)F	80-pin QFP (FP-80B)
				HD64338022WI	HD64338022(***)W	80-pin TQFP (TFP-80C)
	H8/38021	Mask ROM versions	Regular specifications	HD64338021H	HD64338021(***)H	80-pin QFP (FP-80A)
				HD64338021F	HD64338021(***)F	80-pin QFP (FP-80B)
				HD64338021W	HD64338021(***)W	80-pin TQFP (TFP-80C)
				HCD64338021	—	Die
			Wide-range specifications	HD64338021D	HD64338021(***)H	80-pin QFP (FP-80A)
				HD64338021E	HD64338021(***)F	80-pin QFP (FP-80B)
				HD64338021WI	HD64338021(***)W	80-pin TQFP (TFP-80C)
	H8/38020	Mask ROM versions	Regular specifications	HD64338020H	HD64338020(***)H	80-pin QFP (FP-80A)
				HD64338020F	HD64338020(***)F	80-pin QFP (FP-80B)
				HD64338020W	HD64338020(***)W	80-pin TQFP (TFP-80C)
				HCD64338020	—	Die
			Wide-range specifications	HD64338020D	HD64338020(***)H	80-pin QFP (FP-80A)
				HD64338020E	HD64338020(***)F	80-pin QFP (FP-80B)
				HD64338020WI	HD64338020(***)W	80-pin TQFP (TFP-80C)