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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	5MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f38024rwiv

Section 1 Overview

1.1 Overview

The H8/300L Series is a series of single-chip microcomputers (MCU: microcomputer unit), built around the high-speed H8/300L CPU and equipped with peripheral system functions on-chip.

Within the H8/300L Series, the H8/38024 Group, H8/38024S Group, and H8/38124 Group comprise single-chip microcomputers equipped with a LCD (Liquid Crystal Display) controller/driver. Other on-chip peripheral functions include six timers, a two-channel 10-bit pulse width modulator (PWM), a serial communication interface, and an A/D converter. Together, these functions make the H8/38024 Group, H8/38024S Group, and H8/38124 Group ideally suited for embedded applications in systems requiring low power consumption and LCD display. Models in the H8/38024 Group, H8/38024S Group, and H8/38124 Group are the H8/38024, H8/38024S, and H8/38124 with on-chip 32-Kbyte ROM and 1-Kbyte RAM, the H8/38023, H8/38023S, and H8/38123 with on-chip 24-Kbyte ROM and 1-Kbyte RAM, the H8/38022, H8/38022S, and H8/38122 with on-chip 16-Kbyte ROM and 1-Kbyte RAM, the H8/38021, H8/38021S, and H8/38121 with 12-Kbyte ROM and 512 byte RAM, and the H8/38020, H8/38020S, and H8/38120 with 8-Kbyte ROM and 512 byte RAM.

The H8/38024 is also available in a ZTAT™*1 version with on-chip PROM which can be programmed as required by the user. The H8/38024 is also available in F-ZTAT™*2 versions with on-chip flash memory which can be reprogrammed on board.

The H8/38124 is also available in an F-ZTAT™ version with on-chip flash memory that can be programmed on board.

Table 1.1 summarizes the features of the H8/38024 Group, H8/38024S Group, and H8/38124 Group.

Notes: 1. ZTAT (Zero Turn Around Time) is a trademark of Renesas Technology Corp.
2. F-ZTAT is a trademark of Renesas Technology Corp.

2.9 Application Notes

2.9.1 Notes on Data Access

1. Access to Empty Areas:

   The address space of the H8/300L CPU includes empty areas in addition to the RAM, registers, and ROM areas available to the user. If these empty areas are mistakenly accessed by an application program, the following results will occur.

   Data transfer from CPU to empty area:

   The transferred data will be lost. This action may also cause the CPU to misoperate.

   Data transfer from empty area to CPU:

   Unpredictable data is transferred.

2. Access to Internal I/O Registers:

   Internal data transfer to or from on-chip modules other than the ROM and RAM areas makes use of an 8-bit data width. If word access is attempted to these areas, the following results will occur.

   Word access from CPU to I/O register area:

   Upper byte: Will be written to I/O register.

   Lower byte: Transferred data will be lost.

   Word access from I/O register to CPU:

   Upper byte: Will be written to upper part of CPU register.

   Lower byte: Unpredictable data will be written to lower part of CPU register.

Byte size instructions should therefore be used when transferring data to or from I/O registers other than the on-chip ROM and RAM areas. Figure 2.17 shows the data size and number of states in which on-chip peripheral modules can be accessed.

- Example of a malfunction

  When flags are cleared with multiple instructions, other flags might be cleared during execution of the instructions, even though they are currently set, and this will cause a malfunction.

  Here is an example in which IRRI0 is cleared and disabled in the process of clearing IRRI1 (bit 1 of IRR1).

```
MOV.B @IRR1:8,R1L ......... IRRI0 = 0 at this time
AND.B #B'11111101,R1L ..... Here, IRRI0 = 1
MOV.B R1L,@IRR1:8 ......... IRRI0 is cleared to 0
```

  In the above example, it is assumed that an IRQ0 interrupt is generated while the AND.B instruction is executing.

  The IRQ0 interrupt is disabled because, although the original objective is clearing IRRI1, IRRI0 is also cleared.

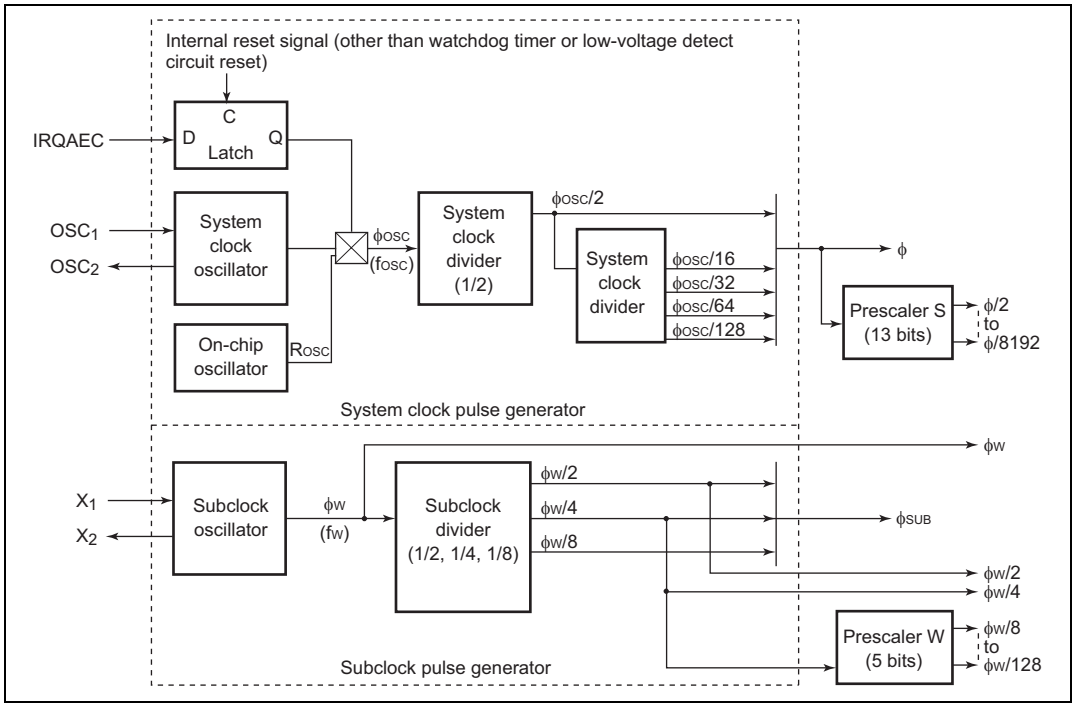

Figure 4.2 Block Diagram of Clock Pulse Generators (H8/38124 Group)

4.1.2 System Clock and Subclock

The basic clock signals that drive the CPU and on-chip peripheral modules are ϕ and ϕ_{SUB}. Four of the clock signals have names: ϕ is the system clock, ϕ_{SUB} is the subclock, ϕ_{OSC} is the oscillator clock, and ϕ_W is the watch clock.

The clock signals available for use by peripheral modules are $\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$, $\phi/32$, $\phi/64$, $\phi/128$, $\phi/256$, $\phi/512$, $\phi/1024$, $\phi/2048$, $\phi/4096$, $\phi/8192$, ϕ_W, $\phi_W/2$, $\phi_W/4$, $\phi_W/8$, $\phi_W/16$, $\phi_W/32$, $\phi_W/64$, and $\phi_W/128$. The clock requirements differ from one module to another.

5.3 Standby Mode

5.3.1 Transition to Standby Mode

The system goes from active mode to standby mode when a SLEEP instruction is executed while the SSBY bit in SYSCR1 is set to 1, the LSON bit in SYSCR1 is cleared to 0, and bit TMA3 in TMA is cleared to 0. In standby mode the clock pulse generator stops, so the CPU and on-chip peripheral modules stop functioning, but as long as the rated voltage is supplied, the contents of CPU registers, on-chip RAM, and some on-chip peripheral module registers are retained. On-chip RAM contents will be further retained down to a minimum RAM data retention voltage. The I/O ports go to the high-impedance state. Port 5 of the HD64F38024 retains the previous pin state.

5.3.2 Clearing Standby Mode

Standby mode is cleared by an interrupt (IRQ_1 or IRQ_0), WKP_7 to WKP_0 or by input at the $\overline{RES}$ pin.

- Clearing by interrupt

  When an interrupt is requested, the system clock pulse generator starts. After the time set in bits STS2 to STS0 in SYSCR1 has elapsed, a stable system clock signal is supplied to the entire chip, standby mode is cleared, and interrupt exception handling starts. Operation resumes in active (high-speed) mode if MSON = 0 in SYSCR2, or active (medium-speed) mode if MSON = 1. Standby mode is not cleared if the I bit of CCR is set to 1 or the particular interrupt is disabled in the interrupt enable register.

- Clearing by $\overline{RES}$ input

  When the $\overline{RES}$ pin goes low, the system clock pulse generator starts. After the pulse generator output has stabilized, if the $\overline{RES}$ pin is driven high, the CPU starts reset exception handling. Since system clock signals are supplied to the entire chip as soon as the system clock pulse generator starts functioning, the $\overline{RES}$ pin should be kept at the low level until the pulse generator output stabilizes.

5.3.3 Oscillator Stabilization Time after Standby Mode Is Cleared

Bits STS2 to STS0 in SYSCR1 should be set as follows.

Note that stabilization times for the H8/38024, H8/38024S, and H8/38024R Group and for the H8/38124 Group are different.

Register Name	Bit Name		Operation
CKSTPR2	LDCKSTP	1	LCD module standby mode is cleared
		0	LCD is set to module standby mode
	PW1CKSTP	1	PWM1 module standby mode is cleared
		0	PWM1 is set to module standby mode
	WDCKSTP	1	Watchdog timer module standby mode is cleared
		0	Watchdog timer is set to module standby mode
	AECKSTP	1	Asynchronous event counter module standby mode is cleared
		0	Asynchronous event counter is set to module standby mode
	PW2CKSTP	1	PWM2 module standby mode is cleared
		0	PWM2 is set to module standby mode
	LVDCKSTP*	1	LVD module standby mode is cleared
		0	LVD is set to module standby mode

Notes: For details of module operation, see the sections on the individual modules.
* LVDCKSTP is implemented on the H8/38124 group only.

5.10 Usage Note

5.10.1 Contention Between Module Standby and Interrupts

If, due to timing with which a peripheral module issues interrupt requests, the module in question is set to module standby mode before an interrupt is processed, the module will stop with the interrupt request still pending. In this situation, interrupt processing will be repeated indefinitely unless interrupts are prohibited.

It is therefore necessary to ensure that no interrupts are generated when a module is set to module standby mode. The surest way to do this is to specify the module standby mode setting only when interrupts are prohibited (interrupts prohibited using the interrupt enable register or interrupts masked using bit CCR-1).

Tables 6.3 and 6.4 give the electrical characteristics in programming mode.

Table 6.3 DC Characteristics

Conditions: V_{CC} = 6.0 V ±0.25 V, V_{PP} = 12.5 V ±0.3 V, V_{SS} = 0 V, T_a = 25°C ±5°C

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high-level voltage	EO_7 to EO_0, EA_{16} to EA_0, $\overline{OE}$, $\overline{CE}$, $\overline{PGM}$	V_{IH}	2.4	—	V_{CC} + 0.3	V	
Input low-level voltage	EO_7 to EO_0, EA_{16} to EA_0, $\overline{OE}$, $\overline{CE}$, $\overline{PGM}$	V_{IL}	–0.3	—	0.8	V	
Output high-level voltage	EO_7 to EO_0	V_{OH}	2.4	—	—	V	I_{OH} = –200 µA
Output low-level voltage	EO_7 to EO_0	V_{OL}	—	—	0.45	V	I_{OL} = 0.8 mA
Input leakage current	EO_7 to EO_0, EA_{16} to EA_0, $\overline{OE}$, $\overline{CE}$, $\overline{PGM}$	$\lvert I_{LI} \rvert$	—	—	2	µA	V_{in} = 5.25 V/ 0.5 V
V_{CC} current		I_{CC}	—	—	40	mA	
V_{PP} current		I_{PP}	—	—	40	mA	

8.10.4 Pin States

Table 8.28 shows the port A pin states in each operating mode.

Table 8.28 Port A Pin States

Pins	Reset	Sleep	Subsleep	Standby	Watch	Subactive	Active
PA_3/COM_4 PA_2/COM_3 PA_1/COM_2 PA_0/COM_1	High-impedance	Retains previous state	Retains previous state	High-impedance	Retains previous state	Functional	Functional

Read Access

In access to TCF, when the upper byte is read the upper-byte data is transferred directly to the CPU and the lower-byte data is transferred to TEMP. Next, when the lower byte is read, the lower-byte data in TEMP is transferred to the CPU.

In access to OCRF, when the upper byte is read the upper-byte data is transferred directly to the CPU. When the lower byte is read, the lower-byte data is transferred directly to the CPU.

Figure 9.5 shows an example in which TCF is read when it contains H'AAFF.

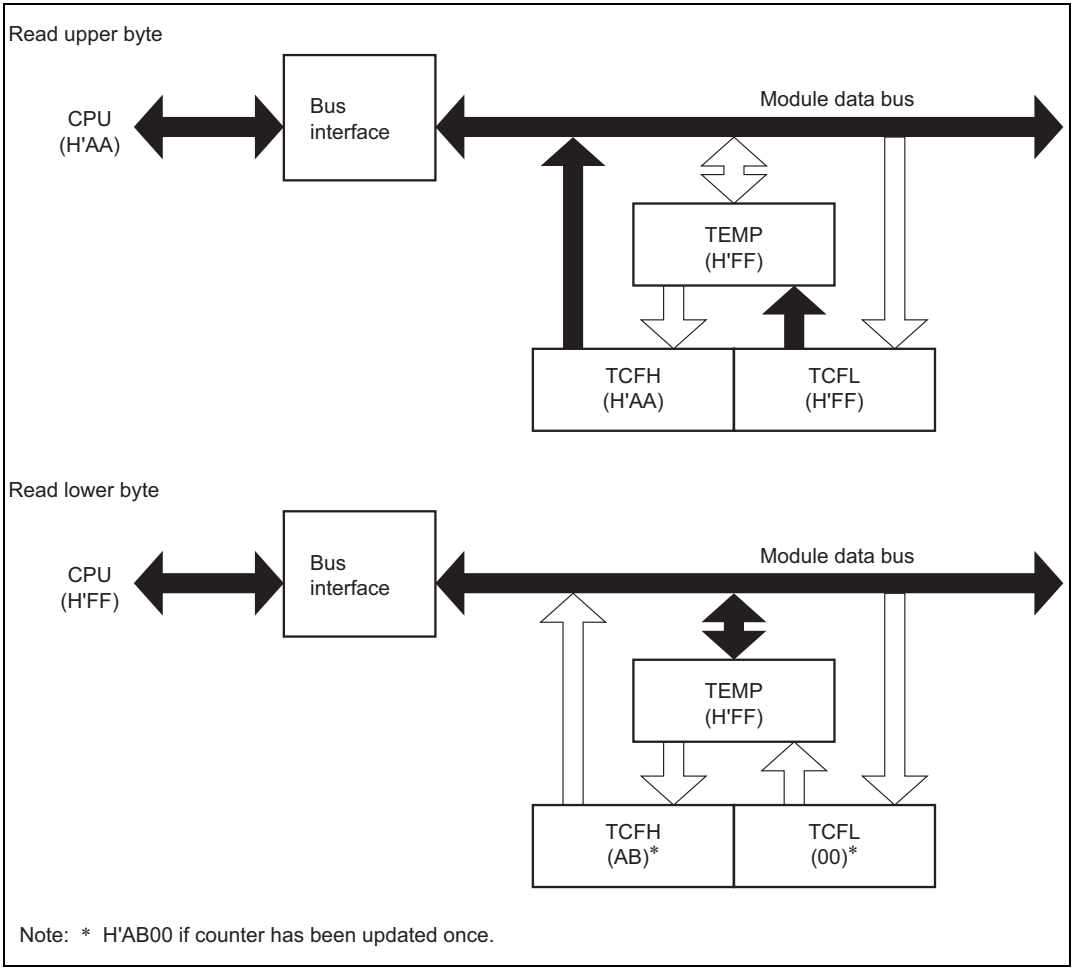

Figure 9.5 Read Access to TCF (TCF → CPU)

b. With noise cancellation function

When noise cancellation is performed on the input capture input, the passage of the input capture signal through the noise canceler results in a delay of five sampling clock cycles from the input capture input signal edge.

Figure 9.12 shows the timing in this case.

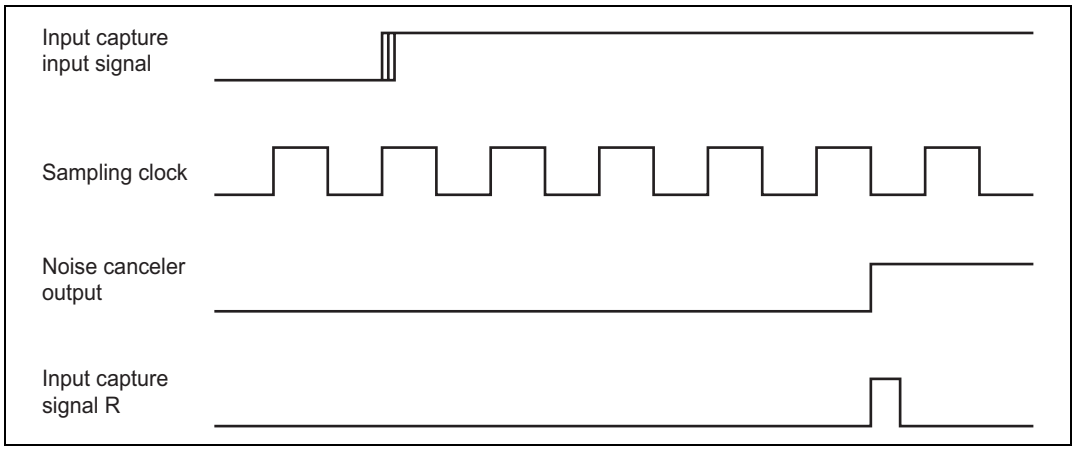

Figure 9.12 Input Capture Input Timing (with Noise Cancellation Function)

Timing of Input Capture by Input Capture Input

Figure 9.13 shows the timing of input capture by input capture input

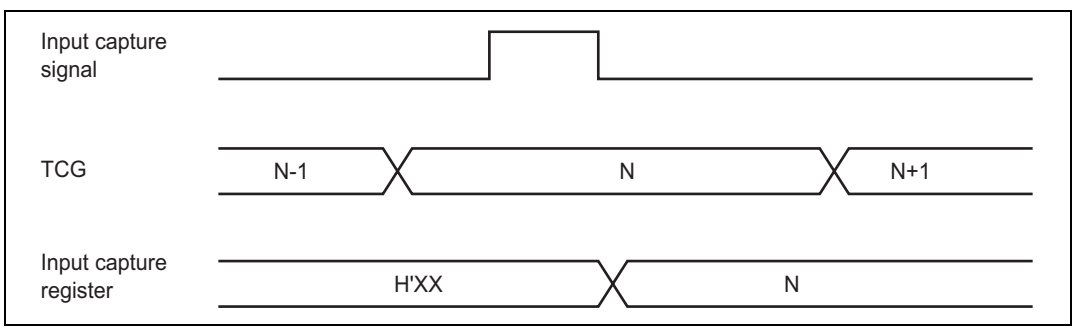

Figure 9.13 Timing of Input Capture by Input Capture Input

9.6.2 Register Descriptions

Timer Control/Status Register W (TCSRW)

Bit	7	6	5	4	3	2	1	0
	B6WI	TCWE	B4WI	TCSRWE	B2WI	WDON	B0WI	WRST
Initial value	1	0	1	0	1	0/1*2	1	0
Read/Write	R	(R/W)*1	R	(R/W)*1	R	(R/W)*1	R	(R/W)*1

Notes: 1. Write is enabled only under certain conditions, which are given in the descriptions of the individual bits.
2. Initial value is 0 on H8/38024, H8/38024S, and H8/38024R Group; initial value is 1 on H8/38124 Group.

TCSRW is an 8-bit read/write register that controls write access to TCW and TCSRW itself, controls watchdog timer operations, and indicates operating status.

Bit 7—Bit 6 Write Disable (B6WI)

Bit 7 controls the writing of data to bit 6 in TCSRW.

Bit 7 B6WI	Description	
0	Bit 6 is write-enabled	
1	Bit 6 is write-protected	(initial value)

This bit is always read as 1. Data written to this bit is not stored.

Bit 6—Timer Counter W Write Enable (TCWE)

Bit 6 controls the writing of data to TCW.

Bit 6 TCWE	Description	
0	Data cannot be written to TCW	(initial value)
1	Data can be written to TCW	

ECH is an 8-bit read-only up-counter that operates either as an independent 8-bit event counter or as the upper 8-bit up-counter of a 16-bit event counter configured in combination with ECL. The external asynchronous event AEVH pin, $\phi/2$, $\phi/4$, $\phi/8$, or the overflow signal from lower 8-bit counter ECL can be selected as the input clock source. ECH can be cleared to H'00 by software, and is also initialized to H'00 upon reset.

Event Counter L (ECL)

Bit	7	6	5	4	3	2	1	0
	ECL7	ECL6	ECL5	ECL4	ECL3	ECL2	ECL1	ECL0
Initial Value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

ECL is an 8-bit read-only up-counter that operates either as an independent 8-bit event counter or as the lower 8-bit up-counter of a 16-bit event counter configured in combination with ECH. The event clock from the external asynchronous event AEVL pin, $\phi/2$, $\phi/4$, or $\phi/8$ is used as the input clock source. ECL can be cleared to H'00 by software, and is also initialized to H'00 upon reset.

Clock Stop Register 2 (CKSTPR2)

Bit	7	6	5	4	3	2	1	0
	LVDCKSTP*	—	—	PW2CKSTP	AECKSTP	WDCKSTP	PW1CKSTP	LDCKSTP
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	—	—	R/W	R/W	R/W	R/W	R/W

Note: * Bits 6 and 5 are also reserved on products other than the H8/38124 Group.

CKSTPR2 is an 8-bit read/write register that performs module standby mode control for peripheral modules. Only the bit relating to the asynchronous event counter is described here. For details of the other bits, see the sections on the relevant modules.

Bit 3—Asynchronous Event Counter Module Standby Mode Control (AECKSTP)

Bit 3 controls setting and clearing of module standby mode for the asynchronous event counter.

AECKSTP	Description	
0	Asynchronous event counter is set to module standby mode	
1	Asynchronous event counter module standby mode is cleared	(initial value)

Bit 7 TIE	Description	
0	Transmit data empty interrupt request (TXI) disabled	(initial value)
1	Transmit data empty interrupt request (TXI) enabled	

Bit 6—Receive Interrupt Enable (RIE)

Bit 6 selects enabling or disabling of the receive data full interrupt request (RXI) and the receive error interrupt request (ERI) when receive data is transferred from the receive shift register (RSR) to the receive data register (RDR), and bit RDRF in the serial status register (SSR) is set to 1. There are three kinds of receive error: overrun, framing, and parity.

RXI and ERI can be released by clearing bit RDRF or the FER, PER, or OER error flag to 0, or by clearing bit RIE to 0.

Bit 6 RIE	Description	
0	Receive data full interrupt request (RXI) and receive error interrupt request (ERI) disabled	(initial value)
1	Receive data full interrupt request (RXI) and receive error interrupt request (ERI) enabled	

Bit 5—Transmit Enable (TE)

Bit 5 selects enabling or disabling of the start of transmit operation.

Bit 5 TE	Description	
0	Transmit operation disabled[*1] (TXD32 pin is I/O port)	(initial value)
1	Transmit operation enabled[*2] (TXD32 pin is transmit data pin)	

Notes: 1. Bit TDRE in SSR is fixed at 1.

2. When transmit data is written to TDR in this state, bit TDRE in SSR is cleared to 0 and serial data transmission is started. Be sure to carry out serial mode register (SMR) settings, and setting of bit SPC32 in SPCR, to decide the transmission format before setting bit TE to 1.

10.3.2 Operation in Asynchronous Mode

In asynchronous mode, serial communication is performed with synchronization provided character by character. A start bit indicating the start of communication and one or two stop bits indicating the end of communication are added to each character before it is sent.

SCI3 has separate transmission and reception units, allowing full-duplex communication. As the transmission and reception units are both double-buffered, data can be written during transmission and read during reception, making possible continuous transmission and reception.

Data Transfer Format

The general data transfer format in asynchronous communication is shown in figure 10.3.

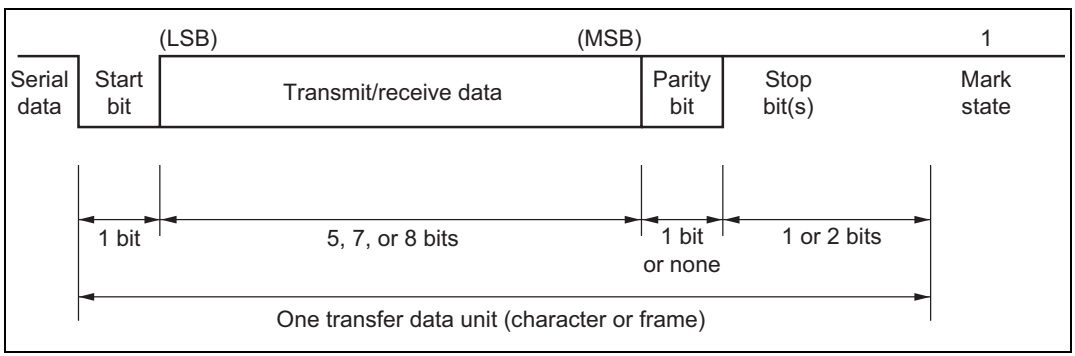

Figure 10.3 Data Format in Asynchronous Communication

In asynchronous communication, the communication line is normally in the mark state (high level). SCI3 monitors the communication line and when it detects a space (low level), identifies this as a start bit and begins serial data communication.

One transfer data character consists of a start bit (low level), followed by transmit/receive data (LSB-first format, starting from the least significant bit), a parity bit (high or low level), and finally one or two stop bits (high level).

In asynchronous mode, synchronization is performed by the falling edge of the start bit during reception. The data is sampled on the 8th pulse of a clock with a frequency 16 times the bit period, so that the transfer data is latched at the center of each bit.

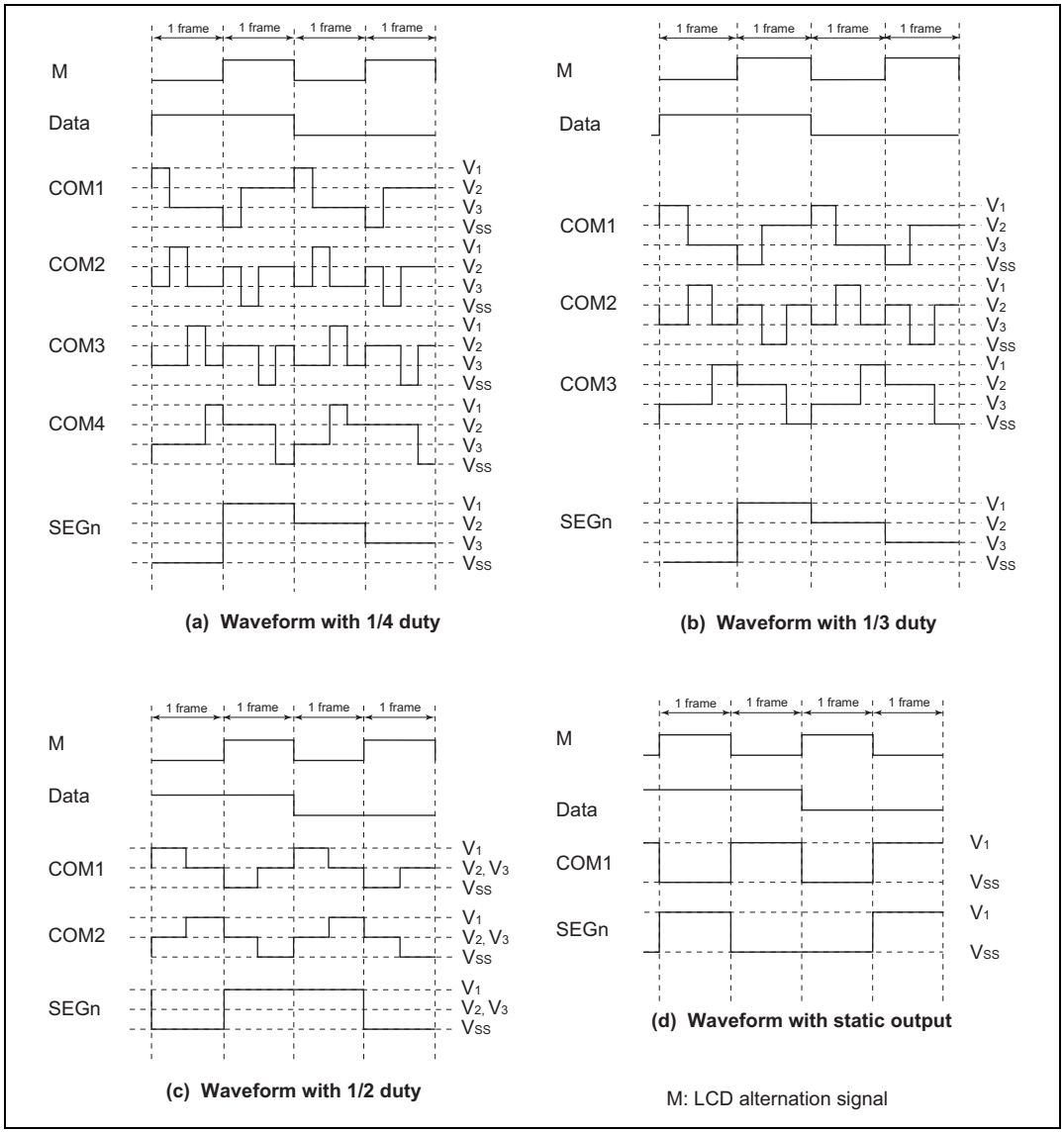

Figure 13.8 Output Waveforms for Each Duty Cycle (B Waveform)

Table 14.3 shows the relationship between LVDCR settings and function selections. Refer to table 14.3 when making settings to LVDCR.

Table 14.3 LVDCR Settings and Function Selections

LVDCR Setting Value					Power-on Reset	Low-Voltage Detection Reset	Low-Voltage Detection Voltage Drop Interrupt	Low-Voltage Detection Voltage Rise Interrupt
LVDE	LVDSEL	LVDRE	LVDDE	LVDUE				
0	*	*	*	*	○	—	—	—
1	1	1	0	0	○	○	—	—
1	0	0	1	0	○	—	○	—
1	0	0	1	1	○	—	○	○
1	0	1	1	1	○	○	○	○

Note: Setting values marked with an asterisk (*) are invalid.

14.2.2 Low-Voltage Detection Status Register (LVDSR)

Bit	7	6	5	4	3	2	1	0
	OVF	—	—	—	VREFSEL	—	LVDDF	LVDUF
Initial value	0*	0	0	0	0	0	0*	0*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * These bits initialized by resets trigged by LVDR.

LVDSR is an 8-bit read/write register. It is used to control external input selection, indicates when the reference voltage is stable, and indicates if the power supply voltage goes below or above a specified range.

Bit 7—LVD Reference Voltage Stabilized Flag (OVF)

This bit indicates when the low-voltage detection counter (LVDCNT) overflows.

Bit 7 OVF	Description	
0	[Clearing condition] When 0 is written after reading 1	(initial value)
1	[Setting condition] When the low-voltage detection counter (LVDCNT) overflows	

Section 15 Power Supply Circuit (H8/38124 Group Only)

This LSI incorporates an internal power supply step-down circuit. Use of this circuit enables the internal power supply to be fixed at a constant level of approximately 3.0 V, independently of the voltage of the power supply connected to the external V_{CC} pin. As a result, the current consumed when an external power supply is used at 3.0 V or above can be held down to virtually the same low level as when used at approximately 3.0 V. If the external power supply is 3.0 V or below, the internal voltage will be practically the same as the external voltage. It is, of course, also possible to use the same level of external power supply voltage and internal power supply voltage without using the internal power supply step-down circuit.

15.1 When Using Internal Power Supply Step-Down Circuit

Connect the external power supply to the V_{CC} pin, and connect a capacitance of approximately 0.1 µF between CV_{CC} and V_{SS}, as shown in figure 15.1. The internal step-down circuit is made effective simply by adding this external circuit. In the external circuit interface, the external power supply voltage connected to V_{CC} and the GND potential connected to V_{SS} are the reference levels. For example, for port input/output levels, the V_{CC} level is the reference for the high level, and the V_{SS} level is that for the low level. The A/D converter analog power supply is not affected by the internal step-down circuit.

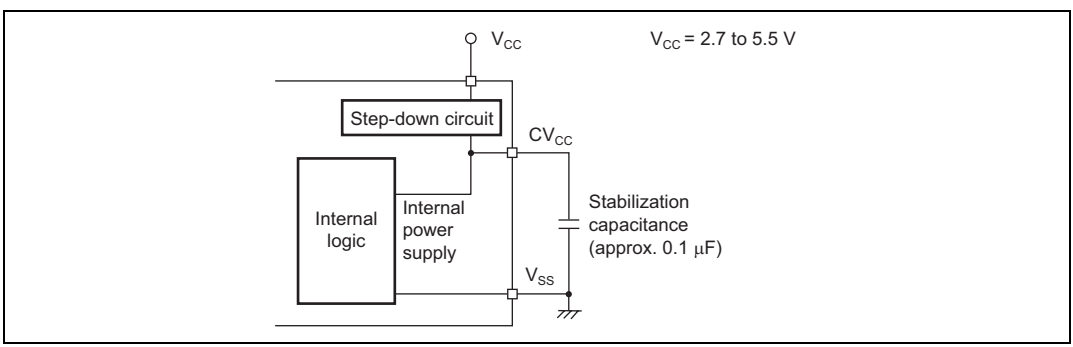

Figure 15.1 Power Supply Connection when Internal Step-Down Circuit is Used

16.8.2 DC Characteristics

Table 16.22 lists the DC characteristics.

Table 16.22 DC Characteristics

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise specified

			Values					
Item	**Symbol**	**Applicable Pins**	**Min**	**Typ**	**Max**	**Unit**	**Test Condition**	**Notes**
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{WKP_0}$ to $\overline{WKP_7}$, $\overline{IRQ_0}$, $\overline{IRQ_3}$, $\overline{IRQ_4}$, AEVL, AEVH, TMIC, TMIF, TMIG, ADTRG, SCK_{32}	$V_{CC} \times 0.8$	—	V_{CC} + 0.3	V	V_{CC} = 4.0 V to 5.5 V	
			$V_{CC} \times 0.9$	—	V_{CC} + 0.3		Other than above	
		$\overline{IRQ_1}$	$V_{CC} \times 0.8$	—	AV_{CC} + 0.3	V	V_{CC} = 4.0 V to 5.5 V	
			$V_{CC} \times 0.9$	—	AV_{CC} + 0.3		Other than above	
		RXD_{32}, UD	$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	V_{CC} = 4.0 V to 5.5 V	
			$V_{CC} \times 0.8$	—	V_{CC} + 0.3		Other than above	
		OSC_1	$V_{CC} \times 0.8$	—	V_{CC} + 0.3	V	V_{CC} = 4.0 V to 5.5 V	
			$V_{CC} \times 0.9$	—	V_{CC} + 0.3		Other than above	
		$P1_3$, $P1_4$, $P1_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_3$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, PA_0 to PA_3	$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V	V_{CC} = 4.0 V to 5.5 V	
			$V_{CC} \times 0.8$	—	V_{CC} + 0.3		Other than above	
		PB_0 to PB_7	$V_{CC} \times 0.7$	—	AV_{CC} + 0.3	V	V_{CC} = 4.0 V to 5.5 V	
			$V_{CC} \times 0.8$	—	AV_{CC} + 0.3		Other than above	
		IRQAEC, $P9_5$*5	$V_{CC} \times 0.8$	—	V_{CC} + 0.3	V	V_{CC} = 4.0 V to 5.5 V	
			$V_{CC} \times 0.9$	—	V_{CC} + 0.3		Other than above	

Note: Connect the TEST pin to V_{SS}.

OSCCR—Clock Pulse Generator Control Register H'F5 Clock Pulse Generator

Note: This register is implemented on the H8/38124 Group only.

Bit	7	6	5	4	3	2	1	0
	SUBSTP	—	—	—	—	IRQAECF	OSCF	—
Initial value	0	0	0	0	0	—	—	0
Read/Write	R/W	R	R/W	R/W	R/W	R	R	R/W

OSC Flag

0	Operation using system clock oscillator (on-chip oscillator stopped)
1	Operation using on-chip oscillator (system clock oscillator stopped)

IRQAEC Flag

0	IRQAEC pin set to GND during resets
1	IRQAEC pin set to VCC during resets

Subclock Oscillator Stop Control

0	Subclock oscillator operating (initial value)
1	Subclock oscillator stopped

C.10 Block Diagrams of Port B

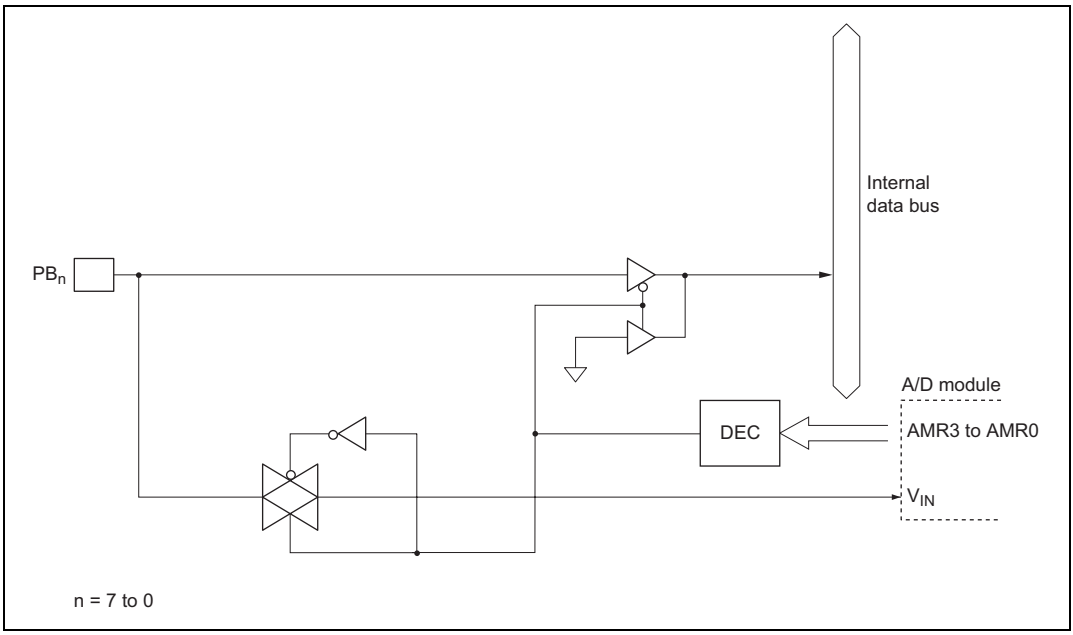

Figure C.10(a) Port B Block Diagram