Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	10MHz
Connectivity	SCI, UART/USART
Peripherals	LCD, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b SAR
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f38024rwv

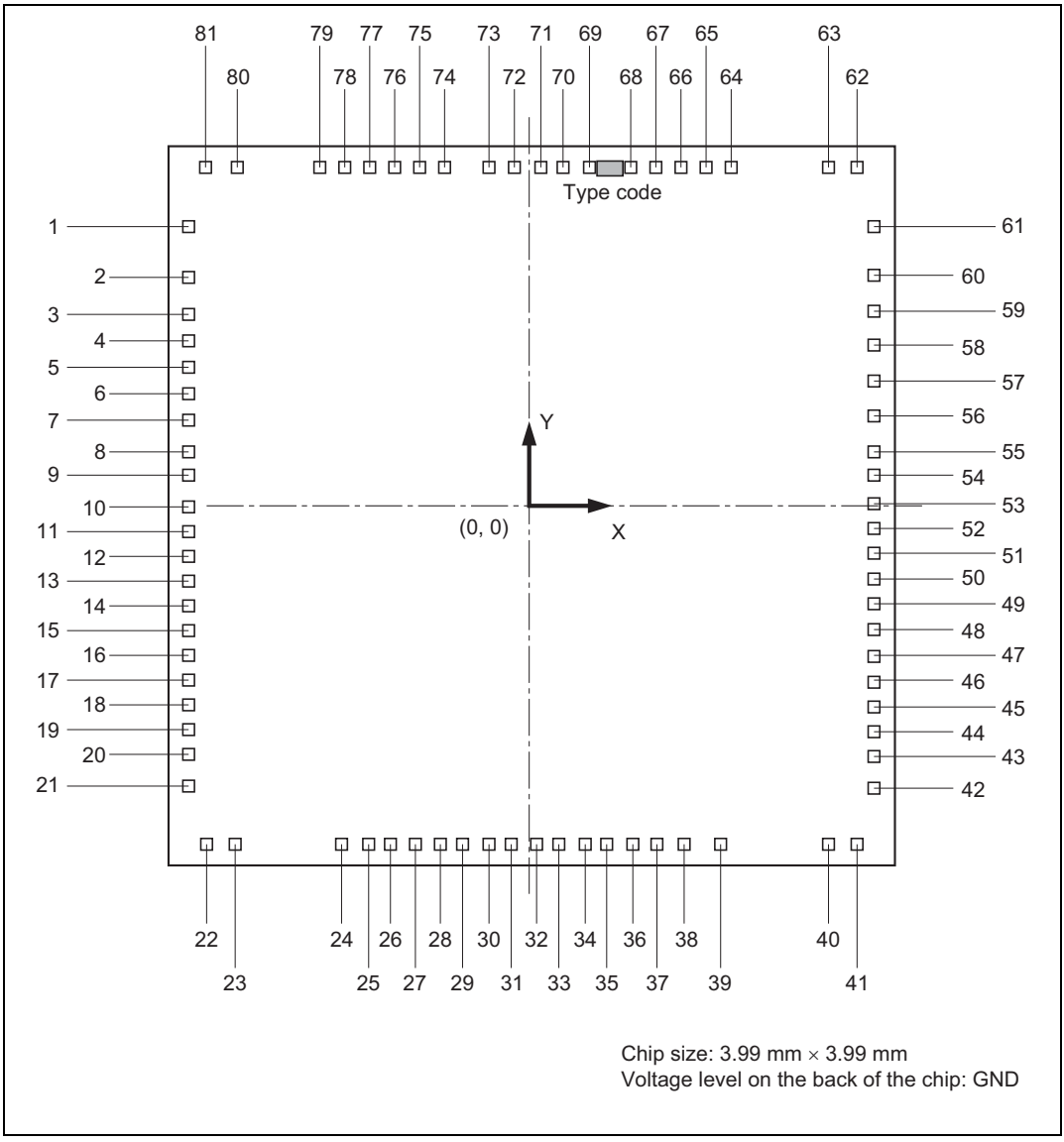

Figure 1.5 Bonding Pad Location Diagram of HCD64338024, HCD64338023, HCD64338022, HCD64338021, and HCD64338020 (Top View)

2.4 Addressing Modes

2.4.1 Addressing Modes

The H8/300L CPU supports the eight addressing modes listed in table 2.1. Each instruction uses a subset of these addressing modes.

Table 2.1 Addressing Modes

No.	Address Modes	Symbol
1	Register direct	Rn
2	Register indirect	@Rn
3	Register indirect with displacement	@(d:16, Rn)
4	Register indirect with post-increment Register indirect with pre-decrement	@Rn+ @–Rn
5	Absolute address	@aa:8 or @aa:16
6	Immediate	#xx:8 or #xx:16
7	Program-counter relative	@(d:8, PC)
8	Memory indirect	@@aa:8

Register Direct—Rn: The register field of the instruction specifies an 8- or 16-bit general register containing the operand.

Only the MOV.W, ADD.W, SUB.W, CMP.W, ADDS, SUBS, MULXU (8 bits × 8 bits), and DIVXU (16 bits ÷ 8 bits) instructions have 16-bit operands.

Register Indirect—@Rn: The register field of the instruction specifies a 16-bit general register containing the address of the operand in memory.

Register Indirect with Displacement—@(d:16, Rn): The instruction has a second word (bytes 3 and 4) containing a displacement which is added to the contents of the specified general register to obtain the operand address in memory.

This mode is used only in MOV instructions. For the MOV.W instruction, the resulting address must be even.

2.5.1 Data Transfer Instructions

Table 2.4 describes the data transfer instructions. Figure 2.5 shows their object code formats.

Table 2.4 Data Transfer Instructions

Instruction	Size*	Function
MOV	B/W	(EAs) → Rd, Rs → (EAd) Moves data between two general registers or between a general register and memory, or moves immediate data to a general register. The Rn, @Rn, @(d:16, Rn), @aa:16, #xx:16, @–Rn, and @Rn+ addressing modes are available for word data. The @aa:8 addressing mode is available for byte data only. The @–R7 and @R7+ modes require word operands. Do not specify byte size for these two modes.
POP	W	@SP+ → Rn Pops a 16-bit general register from the stack. Equivalent to MOV.W @SP+, Rn.
PUSH	W	Rn → @–SP Pushes a 16-bit general register onto the stack. Equivalent to MOV.W Rn, @–SP.

Note: * Size: Operand size
B: Byte
W: Word

Certain precautions are required in data access. See section 2.9.1, Notes on Data Access, for details.

Figure 2.7 lists the format of the bit manipulation instructions.

Figure 2.6 shows the instruction code format of arithmetic, logic, and shift instructions.

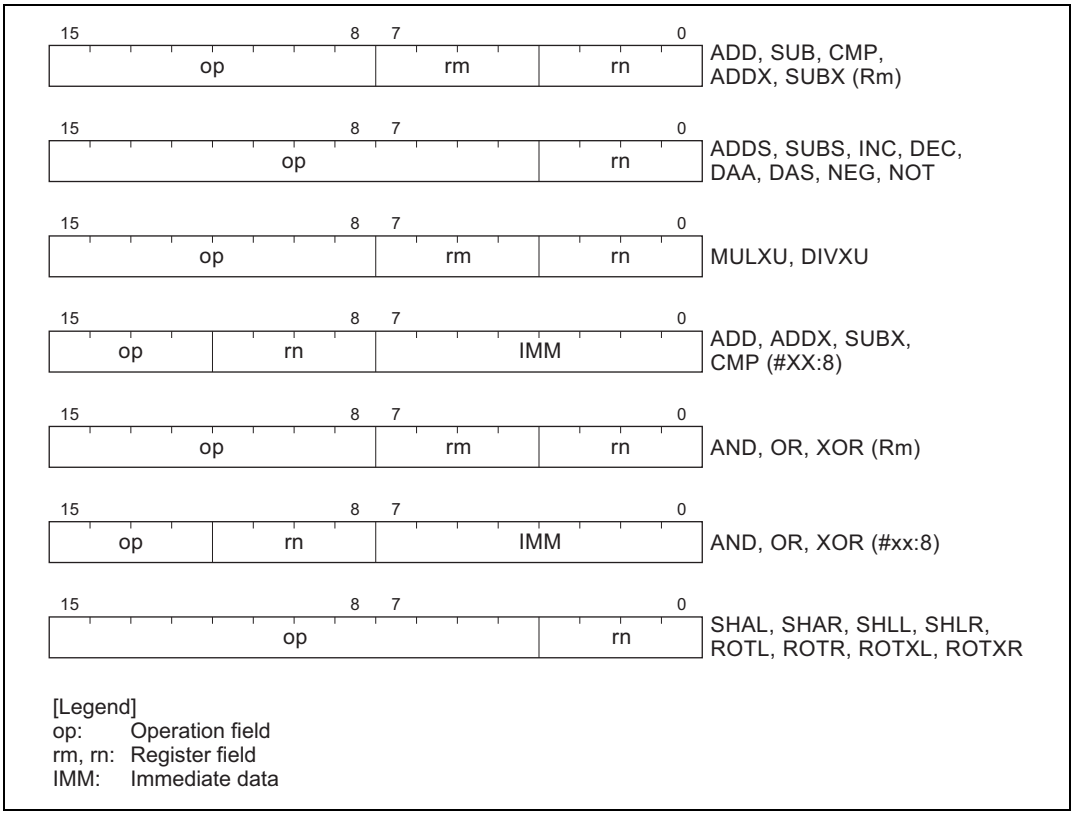

Figure 2.6 Arithmetic, Logic, and Shift Instruction Codes

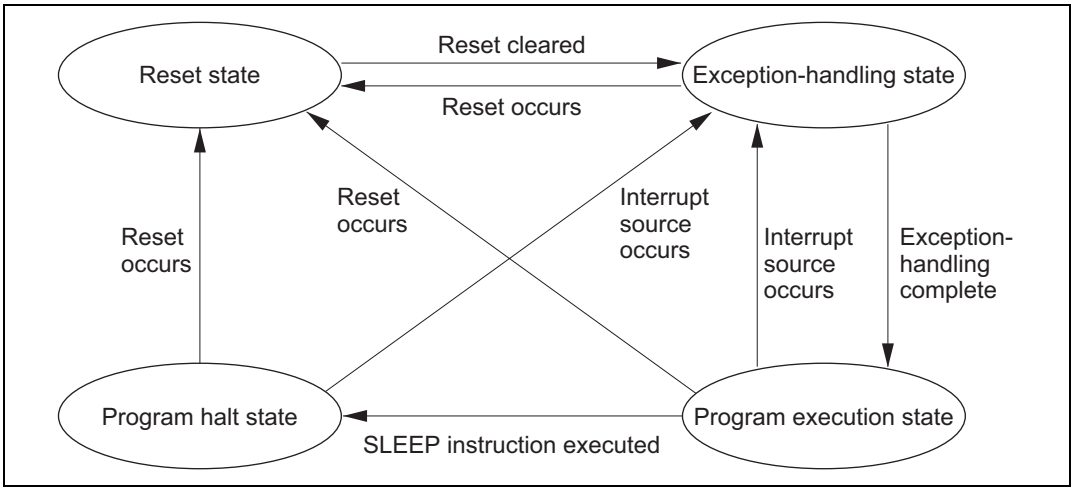

Figure 2.15 State Transitions

2.7.2 Program Execution State

In the program execution state the CPU executes program instructions in sequence.

There are three modes in this state, two active modes (high speed and medium speed) and one subactive mode. Operation is synchronized with the system clock in active mode (high speed and medium speed), and with the subclock in subactive mode. See section 5, Power-Down Modes for details on these modes.

2.7.3 Program Halt State

In the program halt state there are five modes: two sleep modes (high speed and medium speed), standby mode, watch mode, and subsleep mode. See section 5, Power-Down Modes for details on these modes.

2.7.4 Exception-Handling State

The exception-handling state is a transient state occurring when exception handling is started by a reset or interrupt and the CPU changes its normal processing flow. In exception handling caused by an interrupt, SP (R7) is referenced and the PC and CCR values are saved on the stack.

For details on interrupt handling, see section 3.3, Interrupts.

8.5.4 Pin States

Table 8.13 shows the port 5 pin states in each operating mode.

Table 8.13 Port 5 Pin States

Pins	Reset	Sleep	Subsleep	Standby	Watch	Subactive	Active
$P5_7/\overline{WKP}_7$/ $\overline{SEG}_8$ to $P5_0$/ $\overline{WKP}_0/SEG_1$	High-impedance	Retains previous state	Retains previous state	High-impedance*	Retains previous state	Functional	Functional

Note: * A high-level signal is output when the MOS pull-up is in the on state.
In the HD64F38024 the previous pin state is retained.

8.5.5 MOS Input Pull-Up

Port 5 has a built-in MOS input pull-up function that can be controlled by software. When a PCR5 bit is cleared to 0, setting the corresponding PUCR5 bit to 1 turns on the MOS pull-up for that pin. The MOS pull-up function is in the off state after a reset.

$PCR5_n$	0	0	1
$PUCR5_n$	0	1	*
MOS input pull-up	Off	On	Off

(n = 7 to 0)

*: Don't care

Port Data Register 6 (PDR6)

Bit	7	6	5	4	3	2	1	0
	$P6_7$	$P6_6$	$P6_5$	$P6_4$	$P6_3$	$P6_2$	$P6_1$	$P6_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR6 is an 8-bit register that stores data for port 6 pins $P6_7$ to $P6_0$.

If port 6 is read while PCR6 bits are set to 1, the values stored in PDR6 are read, regardless of the actual pin states. If port 6 is read while PCR6 bits are cleared to 0, the pin states are read.

Upon reset, PDR6 is initialized to H'00.

Port Control Register 6 (PCR6)

Bit	7	6	5	4	3	2	1	0
	$PCR6_7$	$PCR6_6$	$PCR6_5$	$PCR6_4$	$PCR6_3$	$PCR6_2$	$PCR6_1$	$PCR6_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PCR6 is an 8-bit register for controlling whether each of the port 6 pins $P6_7$ to $P6_0$ functions as an input pin or output pin.

Setting a PCR6 bit to 1 makes the corresponding pin ($P6_7$ to $P6_0$) an output pin, while clearing the bit to 0 makes the pin an input pin. PCR6 and PDR6 settings are valid when the corresponding pins are designated for general-purpose input/output by bits SGS3 to SGS0 in LPCR.

Upon reset, PCR6 is initialized to H'00.

PCR6 is a write-only register, which is always read as all 1s.

Table 10.4 Relation between n and Clock

		SMR Setting	
n	**Clock**	**CKS1**	**CKS0**
0	ϕ	0	0
0	$\phi w/2^{*1}$/ϕw^{*2}	0	1
2	$\phi/16$	1	0
3	$\phi/64$	1	1

Notes: 1. ϕ w/2 clock in active (medium-speed/high-speed) mode and sleep mode
2. ϕ w clock in subactive mode and subsleep mode
In subactive or subsleep mode, SCI3 can be operated when CPU clock is $\phi w/2$ only.

Table 10.5 shows the maximum bit rate for each frequency. The values shown are for active (high-speed) mode.

Table 10.5 Maximum Bit Rate for Each Frequency (Asynchronous Mode)

			Setting	
OSC (MHz)	**ϕ (MHz)**	**Maximum Bit Rate (bit/s)**	**n**	**N**
0.0384*	0.0192	600	0	0
2	1	31250	0	0
2.4576	1.2288	38400	0	0
4	2	62500	0	0
10	5	156250	0	0
16	8	250000	0	0
20	10	312500	0	0

Note: * When SMR is set up to CKS1 = 0, CKS0 = 1.

SCI3 operates as follows when receiving data.

SCI3 performs internal synchronization and begins reception in synchronization with the serial clock input or output.

The received data is placed in RSR in LSB-to-MSB order.

After the data has been received, SCI3 checks that bit RDRF is set to 0, indicating that the receive data can be transferred from RSR to RDR.

If this check shows that there is no overrun error, bit RDRF is set to 1, and the receive data is stored in RDR. If bit RIE is set to 1 in SCR3, an RXI interrupt is requested. If the check identifies an overrun error, bit OER is set to 1.

Bit RDRF remains set to 1. If bit RIE is set to 1 in SCR3, an ERI interrupt is requested.

See table 10.12 for the conditions for detecting a receive error, and receive data processing.

Note: No further receive operations are possible while a receive error flag is set. Bits OER, FER, PER, and RDRF must therefore be cleared to 0 before resuming reception.

Figure 10.14 shows an example of the operation when receiving in synchronous mode.

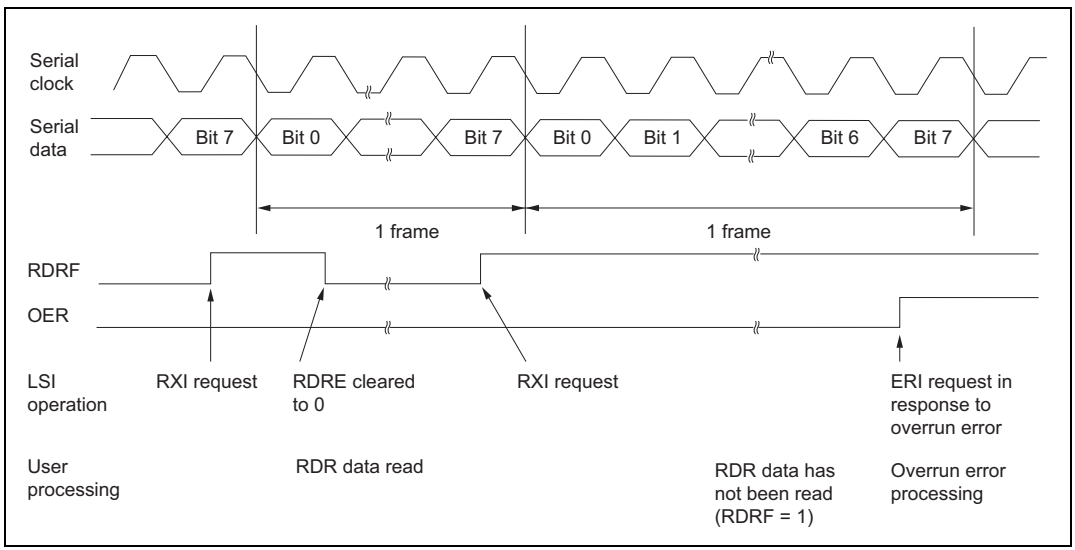

Figure 10.14 Example of Operation when Receiving in Synchronous Mode

- Simultaneous transmit/receive

Figure 10.15 shows an example of a flowchart for a simultaneous transmit/receive operation. This procedure should be followed for simultaneous transmission/reception after initializing SCI3.

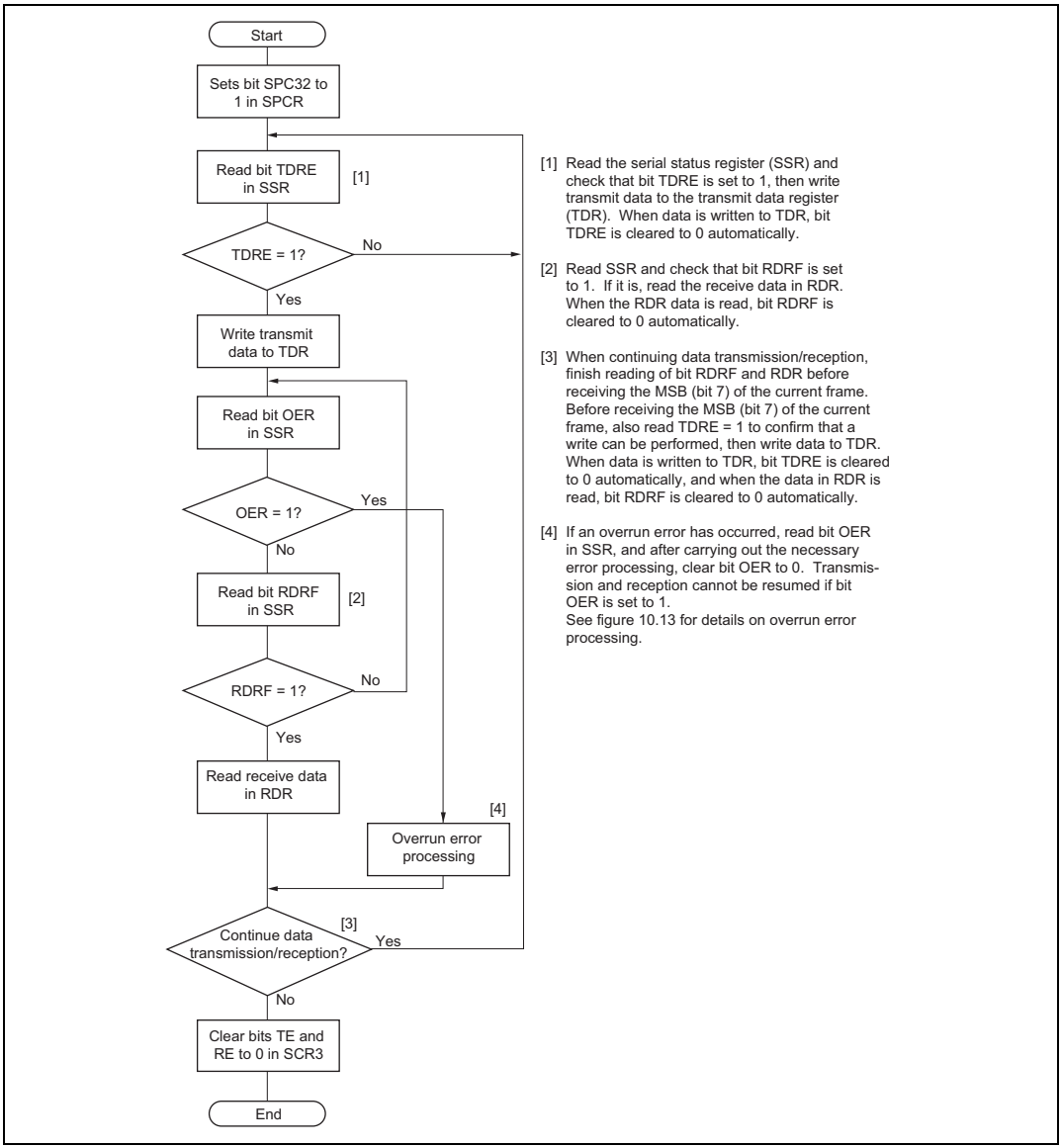

Figure 10.15 Example of Simultaneous Data Transmission/Reception Flowchart (Synchronous Mode)

Section 11 10-Bit PWM

11.1 Overview

The H8/38024 Group is provided with two on-chip 10-bit PWMs (pulse width modulators), designated PWM1 and PWM2, with identical functions. The PWMs can be used as D/A converters by connecting a low-pass filter. In this section the suffix m (m = 1 or 2) is used with register names, etc., as in PWDRLm, which denotes the PWDRL registers for each PWM.

11.1.1 Features

Features of the 10-bit PWMs are as follows.

- Choice of four conversion periods
  Any of the following conversion periods can be chosen:
  4,096/ϕ, with a minimum modulation width of 4/ϕ
  2,048/ϕ, with a minimum modulation width of 2/ϕ
  1,024/ϕ, with a minimum modulation width of 1/ϕ
  512/ϕ, with a minimum modulation width of 1/2 ϕ
- Pulse division method for less ripple
- Use of module standby mode enables this module to be placed in standby mode independently when not used.

On the H8/38124 Group it is possible to select between two types of PWM output: pulse-division PWM and event counter PWM (PWM incorporating AEC). (The H8/38024 Group, H8/38024F-ZTAT Group, and H8/38024S Group can only produce pulse-division PWM output.) Refer to section 9.7, Asynchronous Event Counter, for information on event counter PWM.

Bits 7 to 2—Reserved/Bits 7 to 3—Reserved*

Bits 7 to 2 are reserved; they are always read as 1, and cannot be modified.

Note: * Implemented on H8/38124 Group only.

Bit 2—Output Format Select (PWCRm2)*

This bit selects the format of the output from the PWMm output pin.

This bit is write-only. Reading it always returns 1.

Bit 2 PWCRm2	Description	
0	Pulse-division PWM	(initial value)
1	Event counter PWM	

Note: * Implemented on H8/38124 Group only.

Bits 1 and 0—Clock Select 1 and 0 (PWCRm1, PWCRm0)

Bits 1 and 0 select the clock supplied to the 10-bit PWM. These bits are write-only bits; they are always read as 1.

Bit 1 PWCRm1	Bit 0 PWCRm0	Description	
0	0	The input clock is ϕ ($t\phi^* = 1/\phi$) The conversion period is 512/ϕ, with a minimum modulation width of 1/2ϕ	(initial value)
0	1	The input clock is ϕ/2 ($t\phi^* = 2/\phi$) The conversion period is 1,024/ϕ, with a minimum modulation width of 1/ϕ	
1	0	The input clock is ϕ/4 ($t\phi^* = 4/\phi$) The conversion period is 2,048/ϕ, with a minimum modulation width of 2/ϕ	
1	1	The input clock is ϕ/8 ($t\phi^* = 8/\phi$) The conversion period is 4,096/ϕ, with a minimum modulation width of 4/ϕ	

Note: * Period of PWM input clock.

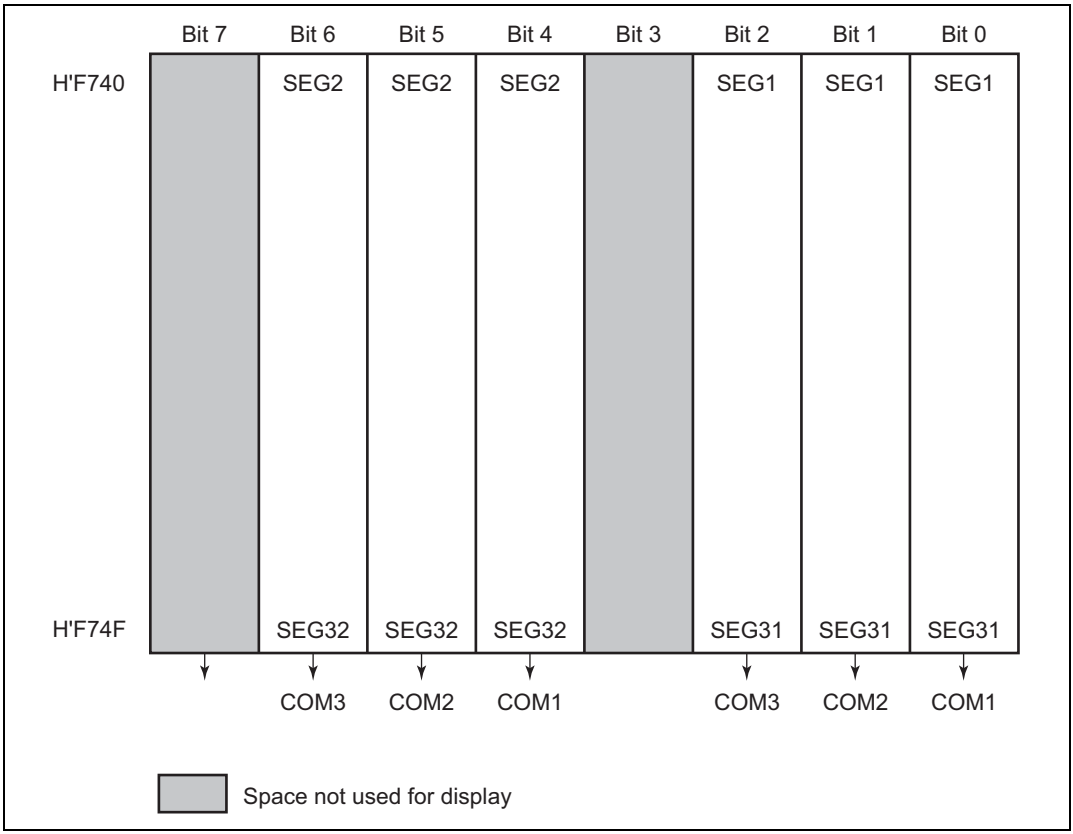

Figure 13.4 LCD RAM Map (1/3 Duty)

Table 14.3 shows the relationship between LVDCR settings and function selections. Refer to table 14.3 when making settings to LVDCR.

Table 14.3 LVDCR Settings and Function Selections

LVDCR Setting Value					Power-on Reset	Low-Voltage Detection Reset	Low-Voltage Detection Voltage Drop Interrupt	Low-Voltage Detection Voltage Rise Interrupt
LVDE	LVDSEL	LVDRE	LVDDE	LVDUE				
0	*	*	*	*	○	—	—	—
1	1	1	0	0	○	○	—	—
1	0	0	1	0	○	—	○	—
1	0	0	1	1	○	—	○	○
1	0	1	1	1	○	○	○	○

Note: Setting values marked with an asterisk (*) are invalid.

14.2.2 Low-Voltage Detection Status Register (LVDSR)

Bit	7	6	5	4	3	2	1	0
	OVF	—	—	—	VREFSEL	—	LVDDF	LVDUF
Initial value	0*	0	0	0	0	0	0*	0*
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * These bits initialized by resets trigged by LVDR.

LVDSR is an 8-bit read/write register. It is used to control external input selection, indicates when the reference voltage is stable, and indicates if the power supply voltage goes below or above a specified range.

Bit 7—LVD Reference Voltage Stabilized Flag (OVF)

This bit indicates when the low-voltage detection counter (LVDCNT) overflows.

Bit 7 OVF	Description	
0	[Clearing condition] When 0 is written after reading 1	(initial value)
1	[Setting condition] When the low-voltage detection counter (LVDCNT) overflows	

16.4.6 Flash Memory Characteristics

Table 16.13 lists the flash memory characteristics.

Table 16.13 Flash Memory Characteristics

AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, V_{CC} = 2.7 V to 3.6 V (operating voltage range in reading), V_{CC} = 3.0 V to 3.6 V (operating voltage range in programming/erasing), T_a = –20 to +75°C (operating temperature range in programming/erasing)

Item		Symbol	Values Min	Typ	Max	Unit	Test Condition
Programming time (per 128 bytes)*1 *2 *4		t_P	—	7	200	ms	
Erase time (per block) *1 *3 *6		t_E	—	100	1200	ms	
Maximum number of reprogrammings		N_{WEC}	1000 *8 *11	10000 *9	—	Times	
			100 *8 *12	10000 *9	—		
Data retention time		t_{DRP}	10*10	—	—	Years	
Programming	Wait time after SWE bit setting*1	x	1	—	—	µs	
	Wait time after PSU bit setting*1	y	50	—	—	µs	
	Wait time after P bit setting*1 *4	z1	28	30	32	µs	1 ≤ n ≤ 6
		z2	198	200	202	µs	7 ≤ n ≤ 1000
		z3	8	10	12	µs	Additional-programming
	Wait time after P bit clear*1	α	5	—	—	µs	
	Wait time after PSU bit clear*1	β	5	—	—	µs	
	Wait time after PV bit setting*1	γ	4	—	—	µs	
	Wait time after dummy write*1	ε	2	—	—	µs	
	Wait time after PV bit clear*1	η	2	—	—	µs	
	Wait time after SWE bit clear*1	θ	100	—	—	µs	
	Maximum programming count*1 *4 *5	N	—	—	1000	Times	
Erase	Wait time after SWE bit setting*1	x	1	—	—	µs	
	Wait time after ESU bit setting*1	y	100	—	—	µs	
	Wait time after E bit setting*1 *6	z	10	—	100	ms	
	Wait time after E bit clear*1	α	10	—	—	µs	
	Wait time after ESU bit clear*1	β	10	—	—	µs	
	Wait time after EV bit setting*1	γ	20	—	—	µs	
	Wait time after dummy write*1	ε	2	—	—	µs	
	Wait time after EV bit clear*1	η	4	—	—	µs	
	Wait time after SWE bit clear*1	θ	100	—	—	µs	
	Maximum erase count*1 *6 *7	N	—	—	120	Times	

Table 16.30 Power Supply Voltage Detection Circuit Characteristics (3)

Using on-chip reference voltage and detect voltage external input (VREFSEL = 0, VINTDSEL and VINTUSEL = 1)

		Rated Values				
Item	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Condition**
extD/extU interrupt detection level	Vexd	0.80	1.20	1.60	V	
extD/extU pin input voltage*2	VextD*1 VextU*1	–0.3	—	V_{CC} + 0.3 or AV_{CC} + 0.3, whichever is lower	V	V_{CC} = 2.7 to 3.3 V
		–0.3	—	3.6 or AV_{CC} + 0.3, whichever is lower	V	V_{CC} = 3.3 to 5.5 V

Notes: 1. The VextD voltage must always be greater than the VextU voltage.
2. The maximum input voltage of the extD and extU pins is 3.6 V.

PDR4—Port Data Register 4 **H'D7** **I/O Ports**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	$P4_3$	$P4_2$	$P4_1$	$P4_0$
Initial value	1	1	1	1	1	0	0	0
Read/Write	—	—	—	—	R	R/W	R/W	R/W

Data for port 4 pins

Reads $P4_3$ state

PDR5—Port Data Register 5 **H'D8** **I/O Ports**

Bit	7	6	5	4	3	2	1	0
	$P5_7$	$P5_6$	$P5_5$	$P5_4$	$P5_3$	$P5_2$	$P5_1$	$P5_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data for port 5 pins

PDR6—Port Data Register 6 **H'D9** **I/O Ports**

Bit	7	6	5	4	3	2	1	0
	$P6_7$	$P6_6$	$P6_5$	$P6_4$	$P6_3$	$P6_2$	$P6_1$	$P6_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data for port 6 pins

PDR7—Port Data Register 7 **H'DA** **I/O Ports**

Bit	7	6	5	4	3	2	1	0
	$P7_7$	$P7_6$	$P7_5$	$P7_4$	$P7_3$	$P7_2$	$P7_1$	$P7_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data for port 7 pins

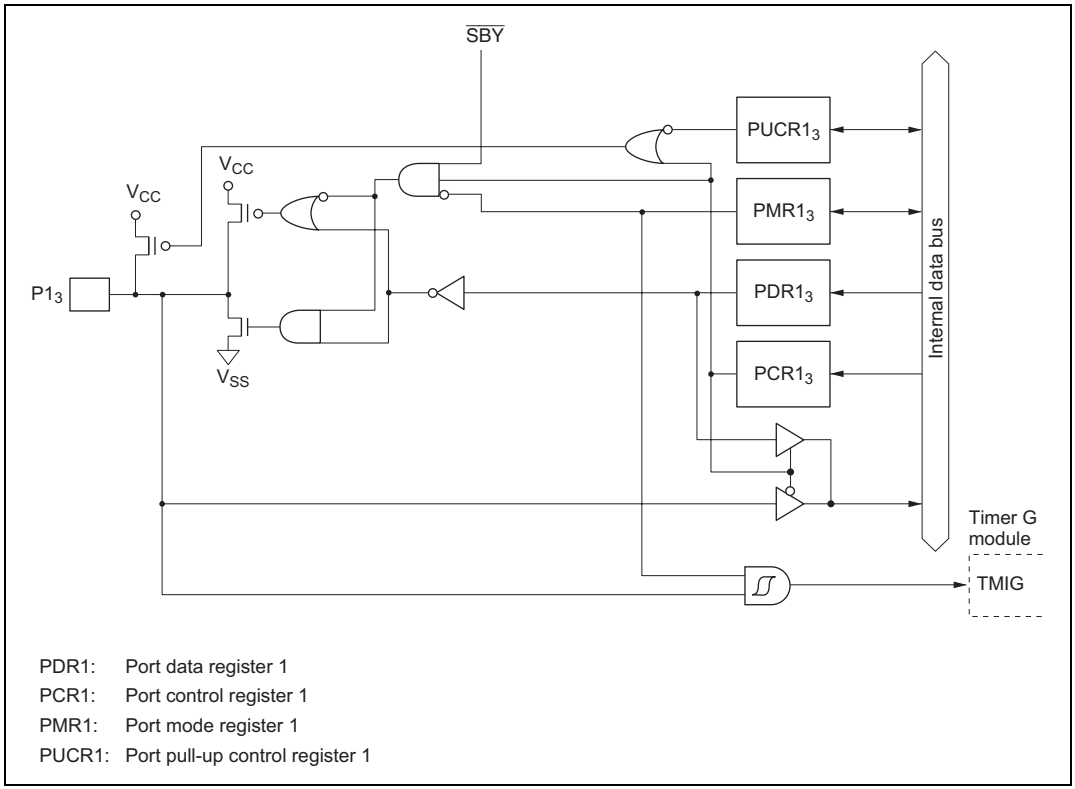

Figure C.1(c) Port 1 Block Diagram (Pin P1$_3$)

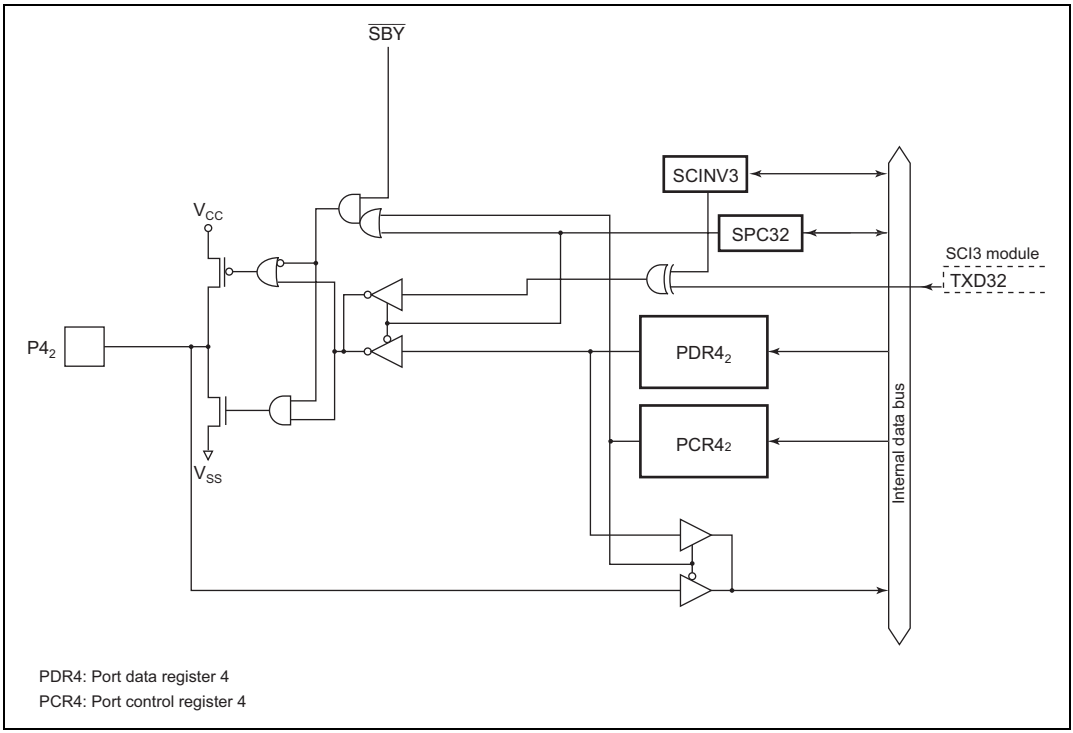

Figure C.3(b) Port 4 Block Diagram (Pin $P4_2$)