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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Xstormy16
Core Size	16-Bit
Speed	12MHz
Connectivity	SIO, UART/USART
Peripherals	PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 11x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-SQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/lc88f58b0au-sqfph

■Minimum Instruction Cycle Time (tCYC)

- 83.3 ns (12MHz) V_{DD} = 4.5 to 5.5V
- 100 ns (10MHz) V_{DD} = 3.0 to 5.5V
- 500 ns (2MHz) V_{DD} = 2.2 to 5.5V

■Ports

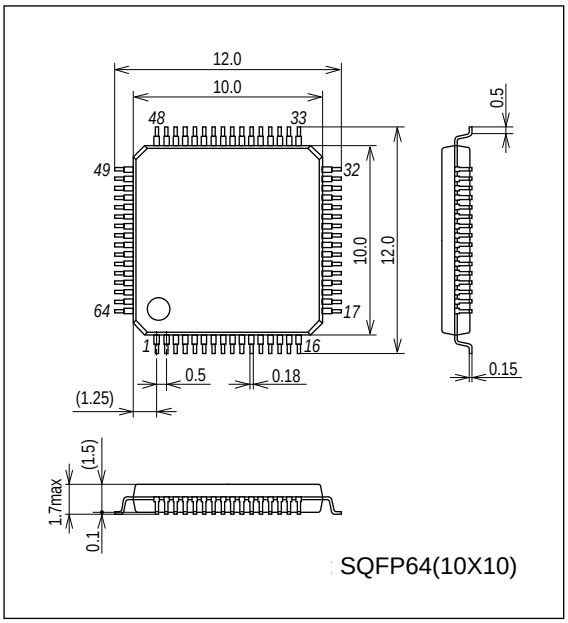
- Normal withstand voltage I/O ports
  Ports whose I/O direction can be designated in 1 bit units : 52 (P0n, P1n, P2n, P30 to P33, P4n, P6n, P70 to P72, PA0 to PA3, PC2)
- Oscillation/normal withstand voltage I/O ports : 2 (PC0, PC1)
- Oscillation dedicated ports : 2 (CF1, CF2)
- Reset pins : 1 (RESB)
- TEST pins : 1 (TEST)
- Power pins : 6 (V_{SS}1 to 3, V_{DD}1 to 3)

■Timers

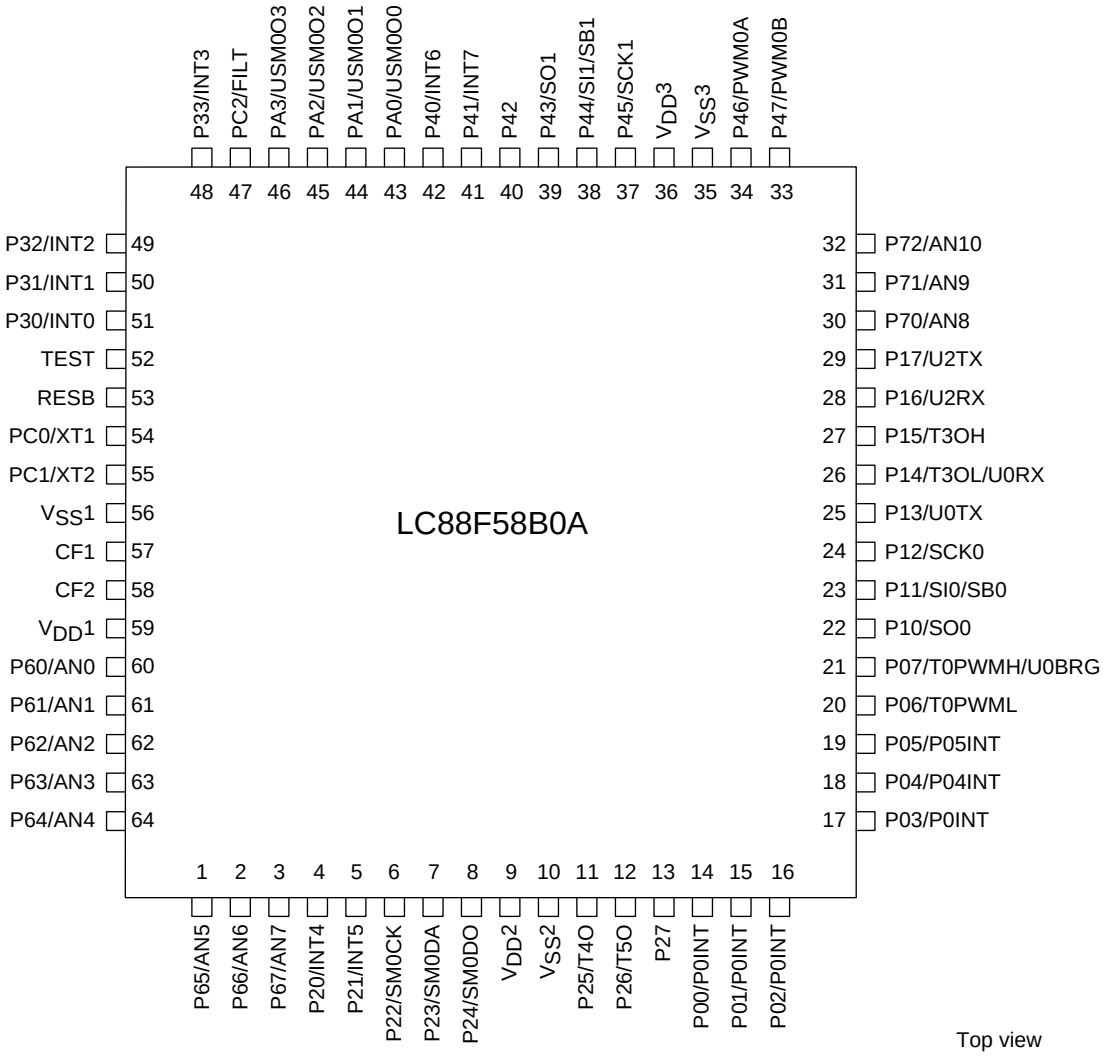
- Timer 0: 16-bit timer that supports PWM/toggle outputs
  1) 5-bit prescaler
  2) 8-bit PWM × 2, 8-bit timer + 8-bit PWM mode selectable
  3) Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
- Timer 1: 16-bit timer with capture registers
  1) 5-bit prescaler
  2) May be divided into 2 channels of 8-bit timer
  3) Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
- Timer 2: 16-bit timer with capture registers
  1) 4-bit prescaler
  2) May be divided into 2 channels of 8-bit timer
  3) Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 3: 16-bit timer that supports PWM/toggle outputs
  1) 8-bit prescaler
  2) 8-bit timer × 2ch or 8-bit timer + 8-bit PWM mode selectable
  3) Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 4: 16-bit timer that supports toggle outputs
  1) Clock source selectable from system clock and prescaler 0
- Timer 5: 16-bit timer that supports toggle outputs
  1) Clock source selectable from system clock and prescaler 0
- Base timer
  1) Clock may be selected from OSC0 (32.768kHz crystal oscillator) and frequency-divided output of system clock.
  2) Interrupts can be generated in 7 timing schemes.

Package Dimensions

unit : mm (typ)
3190A

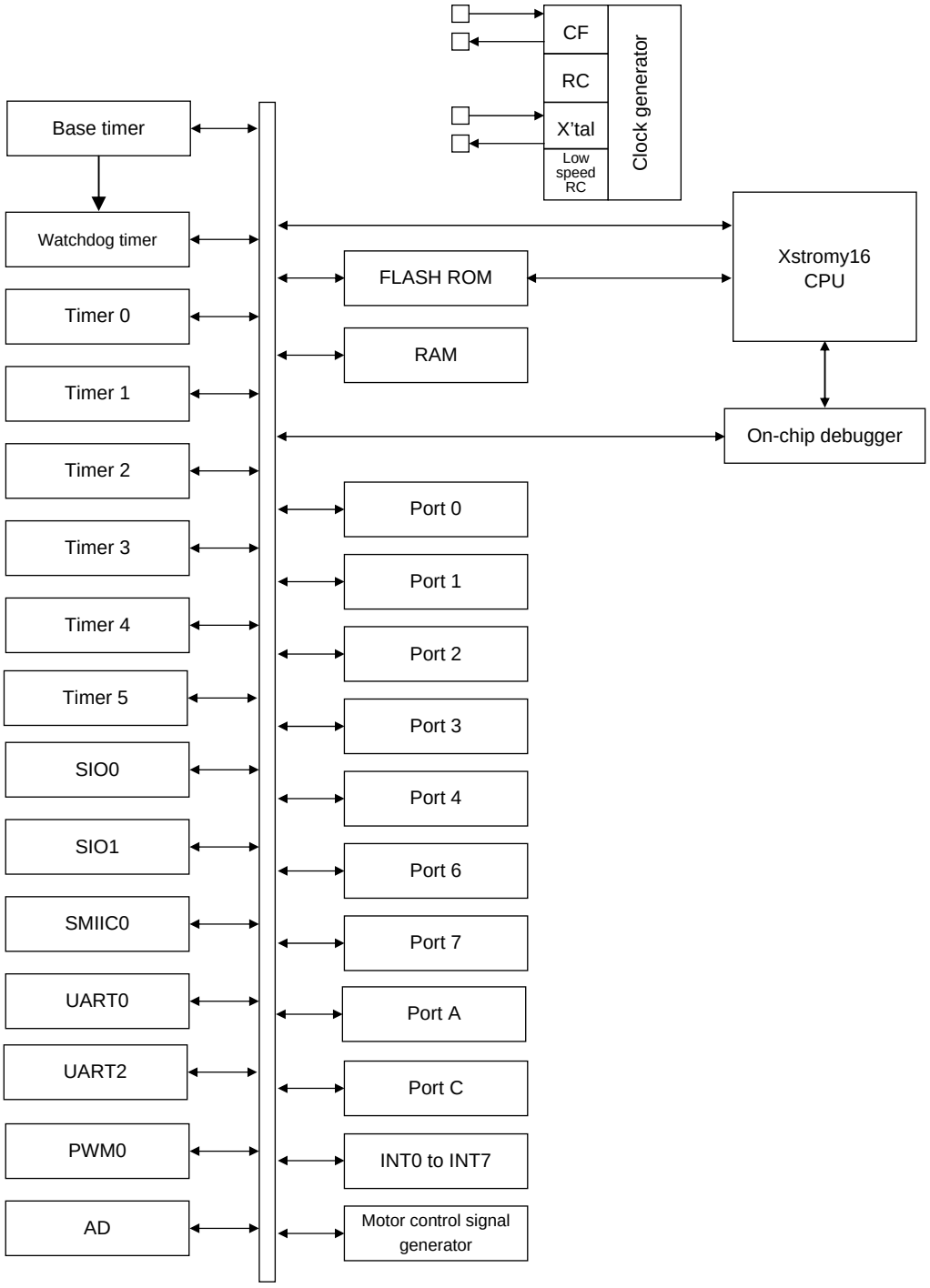


Pin Assignment



SQFP64 (10×10) (Lead-free and halogen-free type)

System Block Diagram



Pin Description

Pin Name	I/O	Description
$V_{SS}1$, $V_{SS}2$, $V_{SS}3$	-	- Power sources
$V_{DD}1$, $V_{DD}2$, $V_{DD}3$	-	+ Power sources
Port 0 P00 to P07	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • HOLD release input (P00 to P03, P04, P05) • Port 0 interrupt input (P00 to P03, P04, P05) • Pin functions P06: Timer 0L output P07: Timer 0L output/UART0 clock input
Port 1 P10 to P17	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions P10: SIO0 data output P11: SIO0 data input/pulse input/output P12: SIO0 clock input/output P13: UART0 transmit P14: Timer 3L output/UART0 receive P15: Timer 3H output P16: UART2 receive P17: UART2 transmit
Port 2 P20 to P27	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions P20: INT4 input/HOLD release input/timer 3 event input/timer 2L capture input/timer 2H capture input P21: INT5 input/HOLD release input/timer 3 event input/timer 2L capture input/timer 2H capture input P22: SMIIC0 clock input/output P23: SMIIC0 bus input/output/data input P24: SMIIC0 data output (used in 3-wire SIO mode) P25: Timer 4 output P26: Timer 5 output Interrupt acknowledge type INT4, INT5: H level, L level, H edge, L edge, both edges
Port 3 P30 to P33	I/O	• 4-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions P30: INT0 input/HOLD release/timer 2L capture input P31: INT1 input/HOLD release/timer 2H capture input P32: INT2 input/HOLD release/timer 2 event input/timer 2L capture input P33: INT3 input/HOLD release/timer 2 event input/timer 2H capture input Interrupt acknowledge type INT0 to INT3: H level, L level, H edge, L edge, both edges

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Pin Name	I/O	Description
Port 4 P40 to P47	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions P40: INT6 input/HOLD release input P41: INT7 input/HOLD release input P43: SIO1 data output P44: SIO1 data input/bus input/output P45: SIO1 clock input/output P46: PWM00 output P47: PWM01 output Interrupt acknowledge type INT6, INT7: H level, L level, H edge, L edge, both edges
Port 6 P60 to P67	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions AN0 (P60) to AN7 (P67): AD converter input port
Port 7 P70 to P72	I/O	• 3-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions AN8 (P70) to AN10 (P72): AD converter input port
Port A PA0 to PA3	I/O	• 4-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Multiplexed pin functions PA0: USM0 output 0 PA1: USM0 output 1 PA2: USM0 output 2 PA3: USM0 output 3
Port C PC0 to PC2	I/O	• 3-bit I/O port (on output: Nch-open drain (PC0 to PC1), CMOS (PC2)) • I/O specifiable in 1-bit units • Pin functions PC0: 32.768kHz crystal oscillator input PC1: 32.768kHz crystal oscillator output PC2: FILT
TEST	I/O	• TEST pin • Used to communicate with on-chip debugger. • Connects an external 100kΩ pull-down resistor.
RESB	I	Reset pin
CF1	I	Ceramic oscillator input pin
CF2	O	Ceramic oscillator output pin

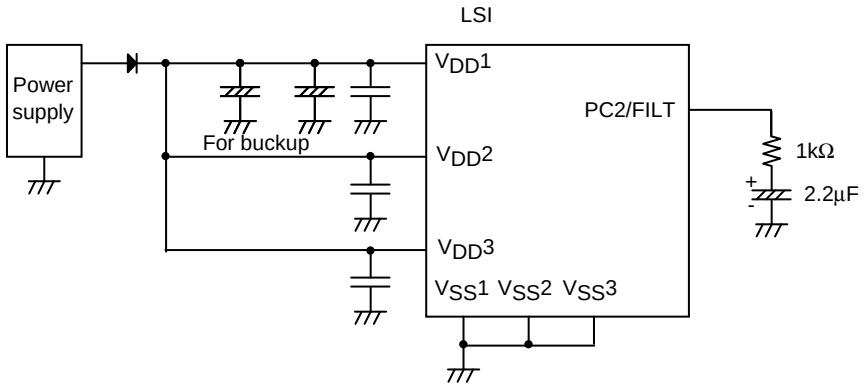
Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

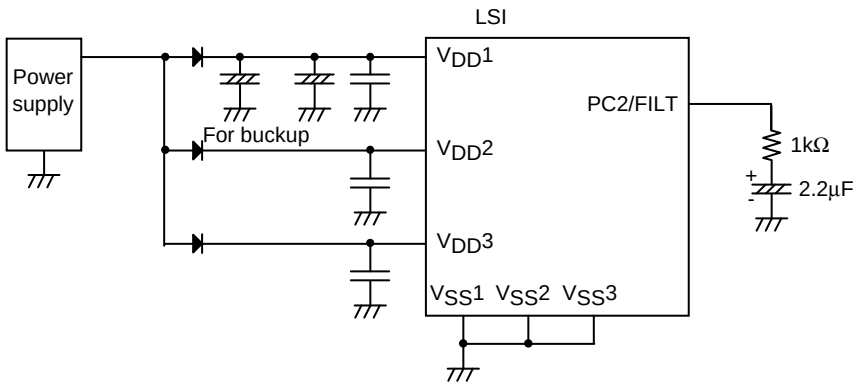
Port Name	Option Selected in Units of	Option Type No.	Output Type	Pull-up Resistor
P00 to P07 P10 to P17 P20 to P27 P30 to P33	1 bit	1	CMOS	Programmable
P40 to P47 P60 to P67 P70 to P72 PA0 to PA3		2	N-channel open drain	
PC2	-	-	CMOS	
PC0	-	-	N-channel open drain (32.768kHz crystal oscillator input)	None
PC1	-	-	N-channel open drain (32.768kHz crystal oscillator output)	None

* Make the following connection to minimize the noise input to the $V_{DD}1$ pin and prolong the backup time.
  Be sure to electrically short the $V_{SS}1$, $V_{SS}2$ and $V_{SS}3$ pins.

Example 1: When data is being backed up in the HOLD mode, the H level signals to the output ports are fed by the backup capacitors.



Example 2: When data is being backed up in the HOLD mode, the H level output at any ports is not sustained and is unpredictable.



Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter		Symbol	Applicable Pin /Remarks	Conditions		Specification			
					V_{DD}[V]	min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$	$V_{DD}1=V_{DD}2=V_{DD}3$		-0.3		+6.5	V
Input voltage		V_I(1)	CF1, RESB			-0.3		V_{DD} +0.3	
Input/output voltage		V_{IO}(1)	Ports 0, 1, 2 Ports 3, 4 Ports 6, 7 Ports A, C			-0.3		V_{DD} +0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2 P70 to P72 P40 to P45 PA0 to PA3	CMOS output selected Per applicable pin		-10			mA
		IOPH(2)	P46, P47	Per applicable pin		-20			
		IOPH(3)	Port 6 P30 to P33 PC2	Per applicable pin		-5			
	Average output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2 P70 to P72 P36 to P37 P40 to P45 PA0 to PA3	CMOS output selected Per applicable pin		-7.5			
		IOMH(2)	P46, P47	Per applicable pin		-10			
		IOMH(3)	Port 6 P30 to P33 PC2	Per applicable pin		-3			
	Total output current	ΣIOAH(1)	P30 to P33, PC2	Total of currents at applicable pins		-15			
		ΣIOAH(2)	Port 6	Total of currents at applicable pins		-15			
		ΣIOAH(3)	Port 6 P30 to P33 PC2	Total of currents at applicable pins		-20			
		ΣIOAH(4)	Ports 0, 1 P25 to P27	Total of currents at applicable pins		-25			
		ΣIOAH(5)	P20 to P24	Total of currents at applicable pins		-25			
		ΣIOAH(6)	Ports 0, 1, 2	Total of currents at applicable pins		-45			
		ΣIOAH(7)	P40 to P45 PA0 to PA3	Total of currents at applicable pins		-25			
		ΣIOAH(8)	P46 to P47 P70 to P72	Total of currents at applicable pins		-25			
		ΣIOAH(9)	Port 4 P70 to P72 PA0 to PA3	Total of currents at applicable pins		-45			

Note 1-1: Average output current refers to the average of output currents measured for a period of 100ms.

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Parameter		Symbol	Applicable Pin /Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	unit
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 4 P70 to P72 PA0 to PA3 P20, P21, P24 to P27	Per applicable pin				20	mA
		IOPL(2)	P22, P23	Per applicable pin				25	
		IOPL(3)	P30 to P33 Port 6 PC0 to PC2	Per applicable pin				10	
	Average output current (Note 1-1)	IOML(1)	Ports 0, 1, 4 P70 to P72 PA0 to PA3 P20, P21, P24 to P27	Per applicable pin				15	
		IOML(2)	P22, P23	Per applicable pin				20	
		IOML(3)	P30 to P33 Port 6 PC0 to PC2	Per applicable pin				7.5	
	Total output current	ΣIOAL(1)	P30 to P34 PC0 to PC2	Total of currents at applicable pins				15	
		ΣIOAL(2)	Port 6	Total of currents at applicable pins				15	
		ΣIOAL(3)	Port 6 P30 to P33 PC0 to PC2	Total of currents at applicable pins				20	
		ΣIOAL(4)	Ports 0, 1 P25 to P27	Total of currents at applicable pins				45	
		ΣIOAL(5)	P20 to P24	Total of currents at applicable pins				45	
		ΣIOAL(6)	Ports 0, 1, 2	Total of currents at applicable pins				80	
		ΣIOAL(7)	P40 to P45 PA0 to PA3	Total of currents at applicable pins				45	
		ΣIOAL(8)	P46 to P47 P70 to P72	Total of currents at applicable pins				45	
		ΣIOAL(9)	Port 4 P70 to P72 PA0 to PA3	Total of currents at applicable pins				80	
Allowable power dissipation		Pd max	SQFP64 (10×10)	Ta=-40 to +85°C				200	mW
Operating ambient temperature		Topr				-40		+85	°C
Storage ambient temperature		Tstg				-55		+125	

Note 1-1: Average output current refers to the average of output currents measured for a period of 100ms.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Electrical Characteristics at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Applicable Pin /Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
High level input current	I_{IH}(1)	Ports 0, 1, 2 Ports 3, 4 Ports 6, 7 Ports A, C RESB	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (Including output Tr. off leakage current)	2.2 to 5.5			1	μA
	I_{IH}(2)	CF1	$V_{IN}=V_{DD}$	2.2 to 5.5			15	
Low level input current	I_{IL}(1)	Ports 0, 1, 2 Ports 3, 4 Ports 6, 7 Ports A, C RESB	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (Including output Tr. off leakage current)	2.2 to 5.5	-1			
	I_{IL}(2)	CF1	$V_{IN}=V_{SS}$	2.2 to 5.5	-15			
High level output voltage	V_{OH}(1)	Ports 0, 1, 2 PA0 to PA3 P40 to P45	I_{OH}=-1.0mA	4.5 to 5.5	V_{DD}-1			V
	V_{OH}(2)		I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	V_{OH}(3)		I_{OH}=-0.2mA	2.2 to 5.5	V_{DD}-0.4			
	V_{OH}(4)	Port 6 P30 to P33 PC2	I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	V_{OH}(5)		I_{OH}=-0.2mA	2.2 to 5.5	V_{DD}-0.4			
	V_{OH}(6)	P46, P47	I_{OH}=-10mA	4.5 to 5.5	V_{DD}-1.5			
	V_{OH}(7)		I_{OH}=-1.6mA	3.0 to 5.5	V_{DD}-0.4			
	V_{OH}(8)		I_{OH}=-1.0mA	2.2 to 5.5	V_{DD}-0.4			
Low level output voltage	V_{OL}(1)	Ports 0, 1 Ports 4, 7 P20 to P21, P24 to P27 PA0 to PA3	I_{OL}=10mA	4.5 to 5.5			1.5	
	V_{OL}(2)		I_{OL}=1.6mA	3.0 to 5.5			0.4	
	V_{OL}(3)		I_{OL}=1.0mA	2.2 to 5.5			0.4	
	V_{OL}(4)	P22, P23	I_{OL}=11mA	4.5 to 5.5			1.5	
	V_{OL}(5)		I_{OL}=3.0mA	3.0 to 5.5			0.4	
	V_{OL}(6)		I_{OL}=1.3mA	2.2 to 5.5			0.4	
	V_{OL}(7)	Ports 6, C P30 to P33	I_{OL}=1.6mA	3.0 to 5.5			0.4	
	V_{OL}(8)		I_{OL}=1.0mA	2.2 to 5.5			0.4	
Pull-up resistor	Rpu(1)	Ports 0, 1, 2, 3 Ports 4, 6, 7 Ports A, PC2	$V_{OH}=0.9V_{DD}$	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			2.2 to 4.5	18	55	150	
Hysteresis voltage	VHYS	RESB When ports 1, 2, 3, 4, A PnFSAn=1		2.2 to 5.5		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	Pins other than that under test $V_{IN}=V_{SS}$ f=1MHz Ta=25°C	2.2 to 5.5		10		pF

SIO0 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-2-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Period	tSCK(3)	SCK0 (P12)	• See Fig. 6.	2.2 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
			tSCKHBSY(3)				2			
Serial input	Data setup time		tsDI(2)	SI0 (P11), SB0 (P11)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.2 to 5.5	0.03			µs
	Data hold time		thDI(2)				0.03			
Serial output	Input clock	Output delay time	tdD0(3)	SO0 (P10), SB0 (P11)	• (Note 4-2-2)	2.2 to 5.5			1tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-2-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig.6.

SIO1 Serial Input/Output Characteristics (Wakeup Function Disabled) (Note 4-3-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Period	tSCK(4)	SCK1(P45)	• See Fig. 6.	2.2 to 5.5	4			tCYC
		Low level pulse width	tSCKL(4)				2			
		High level pulse width	tSCKH(4)				2			
			tSCKHA(4)		• Automatic communication mode • See Fig. 6.		6			
			tSCKHBSY(4a)		• Automatic communication mode • See Fig. 6.		23			
			tSCKHBSY(4b)		• Mode other than automatic communication mode • See Fig. 6.		4			
	Output clock	Period	tSCK(5)	SCK1(P45)	• CMOS output selected • See Fig. 6.	2.2 to 5.5	4			tCYC
		Low level pulse width	tSCKL(5)				1/2			tSCK
		High level pulse width	tSCKH(5)				1/2			
			tSCKHA(5)		• Automatic communication mode • CMOS output selected • See Fig. 6.		6			tCYC
			tSCKHBSY(5a)		• Automatic communication mode • CMOS output selected • See Fig. 6.		4		23	
			tSCKHBSY(5b)		• Mode other than automatic communication mode • See Fig. 6.		4			
Serial input	Data setup time		tsDI(3)	SI1(P44), SB1(P44)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.2 to 5.5	0.03			µs
	Data hold time		thDI(3)				0.03			
Serial output	Input clock	Output delay time	tdD0(4)	SO1(P43), SB1(P44)	• (Note 4-3-2)	2.2 to 5.5			1tCYC +0.05	µs
	Output clock		tdDO(5)		• (Note 4-3-2)				1tCYC +0.05	

Note 4-3-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-3-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

SMIIC0 I²C Mode Input/Output Characteristics

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Clock	Input clock	Period	tSCL	SM0CK(P22)	• See Fig. 8.	2.2 to 5.5	5			Tfilt
		Low level pulse width	tSCLL				2.5			
		High level pulse width	tSCLH				2			
	Output clock	Period	tSCLx	SM0CK(P22)	• Specified as interval up to time when output state starts changing.	2.2 to 5.5	10			
		Low level pulse width	tSCLLx				1/2			tSCL
		High level pulse width	tSCLHx				1/2			
SM0CK and SM0DA pins input spike suppression time			tsp	SM0CK(P22) SM0DA(P23)	• See Fig. 8.				1	Tfilt
Bus release time between start and stop	Input		tBUF	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.2 to 5.5	2.5			Tfilt
	Output		tBUFx	SM0CK(P22) SM0DA(P23)	• Standard clock mode • Specified as interval up to time when output state starts changing.		5.5			µs
					• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.6			
Start/restart condition hold time	Input		tHD;STA	SM0CK(P22) SM0DA(P23)	• When SMIIC register control bit, I^2CSHDS=0 • See Fig. 8.	2.2 to 5.5	2.0			Tfilt
					• When SMIIC register control bit, I^2CSHDS=1 • See Fig. 8.		2.5			
	Output		tHD;STAx	SM0CK(P22) SM0DA(P23)	• Standard clock mode • Specified as interval up to time when output state starts changing.		4.1			µs
					• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.0			
Restart condition setup time	Input		tSU;STA	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.2 to 5.5	1.0			Tfilt
	Output		tSU;STAx	SM0CK(P22) SM0DA(P23)	• Standard clock mode • Specified as interval up to time when output state starts changing.		5.5			µs
					• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.6			

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Parameter		Symbol	Applicable Pin/Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	unit
Stop condition setup time	Input	tSU;STO	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.2 to 5.5	1.0			Tfilt
	Output	tSU;STOx	SM0CK(P22) SM0DA(P23)	• Standard clock mode • Specified as interval up to time when output state starts changing.		4.9			µs
				• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.1			
Data hold time	Input	tHD;DAT	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.2 to 5.5	0			Tfilt
	Output	tHD;DATx	SM0CK(P22) SM0DA(P23)	• Specified as interval up to time when output state starts changing.		1		1.5	
Data setup time	Input	tSU;DAT	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.2 to 5.5	1			Tfilt
	Output	tSU;DATx	SM0CK(P22) SM0DA(P23)	• Specified as interval up to time when output state starts changing.		1tSCL -1.5Tfilt			
SM0CK and SM0DA pins fall time	Input	tF	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.2 to 5.5			300	ns
	Output	tF	SM0CK (P22) SM0DA (P23)	• When SMIIC register control bits, PSLW=1, P5V=1	5	20 +0.1Cb		250	
				• When SMIIC register control bits, PSLW=1, P5V=0	3	20 +0.1Cb		250	
				• SM0CK, SM0DA port output FAST mode • Cb≤400pF	3 to 5.5			100	

Note 4-6-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-6-2: The value of Tfilt is determined by the values of the register SMIC0BRG, bits 7 and 6 (BRP1, BRP0) and the system clock frequency.

BRP1	BRP0	Tfilt
0	0	tCYC×1
0	1	tCYC×2
1	0	tCYC×3
1	1	tCYC×4

Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range:

250ns ≥ Tfilt >140ns

Note 4-6-3: Cb represents the total loads (in pF) connected to the bus pins. Cb ≤ 400pF

Note 4-6-4: The standard clock mode refers to a mode that is entered by configuring SMIC0BRG as follows:

250ns ≥ Tfilt >140ns

BRDQ (bit5) = 1

SCL frequency setting ≤ 100kHz

The high-speed clock mode refers to a mode that is entered by configuring SMIC0BRG as follows:

250ns ≥ Tfilt >140ns

BRDQ (bit5) = 0

SCL frequency setting ≤ 400kHz

Consumption Current Characteristics at Ta=-40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=0V$

typ: 5.0V (V_{DD}=4.5V to 5.5V), 3.3V (V_{DD}=3.0V to 4.5V, 2.2V to 4.5V)

Parameter	Symbol	Applicable Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$	• FmCF=12MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz • Internal RC oscillation stopped • 1/1 frequency division mode	4.5 to 5.5		9.3	15.0	mA
	IDDOP(2)		• FmCF=10MHz ceramic oscillator mode • FmX'tal=32.768kHz crystal oscillator mode • System clock set to 10MHz • Internal RC oscillation stopped • 1/1 frequency division mode	4.5 to 5.5		8.5	14.4	
	IDDOP(3)			3.0 to 4.5		5.0	8.3	
	IDDOP(4)		• FmCF=4MHz ceramic oscillator mode • FmX'tal=32.768kHz crystal oscillator mode • System clock set to 4MHz • Internal RC oscillation stopped • 1/2 frequency division mode	4.5 to 5.5		3.8	5.6	
	IDDOP(5)			2.2 to 4.5		2.5	4.6	
	IDDOP(6)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillator mode • System clock set to internal RC oscillation • 1/1 frequency division mode	4.5 to 5.5		2.5	5.6	
	IDDOP(7)			2.2 to 4.5		1.7	4.6	
	IDDOP(8)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillator mode • System clock set to 32.768kHz • Internal RC oscillation stopped • 1/1 frequency division mode	4.5 to 5.5		63	155	µA
	IDDOP(9)			2.2 to 4.5		39	102	
	IDDOP(10)		• FmCF=12MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz • Internal RC oscillation stopped • PLL oscillation mode • 1/1 frequency division mode	4.5 to 5.5		11.0	17.5	mA
	IDDOP(11)		• FmCF=10MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 10MHz • Internal RC oscillation stopped • PLL oscillation mode • 1/1 frequency division mode	4.5 to 5.5		10.3	17.0	
	IDDOP(12)			3.0 to 4.5		5.9	13.0	

Note 7-1: The consumption current value includes none of the currents that flow into the output transistor and internal pull-up resistors.

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Parameter	Symbol	Applicable Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$	• HALT mode • FmCF=12MHz ceramic mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz • Internal RC oscillation stopped • 1/1 frequency division mode	4.5 to 5.5		2.9	4.4	mA
	IDDHALT(2)		• HALT mode • FmCF=10MHz ceramic oscillator mode • FmX'tal=32.768kHz crystal oscillator mode • System clock set to 10MHz • Internal RC oscillation stopped • 1/1 frequency division mode	4.5 to 5.5		2.5	4.2	
	IDDHALT(3)			3.0 to 4.5		1.3	3.0	
	IDDHALT(4)		• HALT mode • FmCF=4MHz ceramic oscillator mode • FmX'tal=32.768kHz crystal oscillator mode • System clock set to 4MHz • Internal RC oscillation stopped • 1/2 frequency division mode	4.5 to 5.5		0.90	1.6	
	IDDHALT(5)			2.2 to 4.5		0.40	1.1	
	IDDHALT(6)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillator mode • System clock set to internal RC oscillation • 1/1 frequency division mode	4.5 to 5.5		0.42	1.25	
	IDDHALT(7)			2.2 to 4.5		0.20	0.85	
	IDDHALT(8)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillator mode • System clock set to 32.768kHz • Internal RC oscillation stopped • 1/1 frequency division mode	4.5 to 5.5		23	90	µA
	IDDHALT(9)			2.2 to 4.5		10	40	
HOLD mode consumption current	IDDHOLD(1)	$V_{DD}1$	HOLD mode • CF1=V_{DD} or open (external clock mode)	4.5 to 5.5		0.05	20	µA
	IDDHOLD(2)			2.2 to 4.5		0.03	15	
HOLDX mode consumption current	IDDHOLD(3)		HOLDX mode • CF1=V_{DD} or open (external clock mode) • FmX'tal=32.768kHz crystal oscillator mode	4.5 to 5.5		15	58	
	IDDHOLD(4)			2.2 to 4.5		4	35	

Note 7-1: The consumption current value includes none of the currents that flow into the output transistor and internal pull-up resistors.

Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Resonator

Nominal Frequency	Vendor Name	Resonator	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		typ [ms]	max [ms]	
12MHz	MURATA	CSTCE12M0G52-R0	(10)	(10)	OPEN	220	2.4 to 5.5	0.02	0.2	C1, C2 integrated type
10MHz		CSTCE10M0G52-R0	(10)	(10)	OPEN	470	2.4 to 5.5	0.02	0.2	C1, C2 integrated type
		CSTLS10M0G53-B0	(15)	(15)	OPEN	680	2.6 to 5.5	0.02	0.2	C1, C2 integrated type
8MHz		CSTCE8M00G52-R0	(10)	(10)	OPEN	470	2.3 to 5.5	0.02	0.2	C1, C2 integrated type
		CSTLS8M00G53-B0	(15)	(15)	OPEN	1k	2.5 to 5.5	0.02	0.2	C1, C2 integrated type
4MHz		CSTCR4M00G53-R0	(15)	(15)	OPEN	1.5k	2.2 to 5.5	0.02	0.2	C1, C2 integrated type
		CSTLS4M00G53-B0	(15)	(15)	OPEN	1.5k	2.3 to 5.5	0.02	0.2	C1, C2 integrated type

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the lower limit level of the operating voltage range (see Figure 4)

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Resonator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	10	10	OPEN	0	2.2 to 5.5	0.4	2.0	Applicable CL value=7.0pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillator circuit is executed plus the time interval that is required for the oscillation to get stabilized after the HOLD mode is released (see Figure 4).

Note: The traces to and from the components that are involved in oscillation should be kept as short as possible as the oscillation characteristics are affected by their trace pattern.

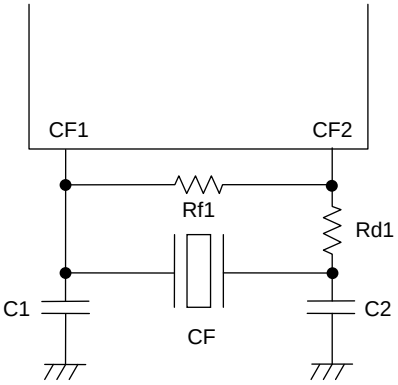


Figure 1 CF Oscillator Circuit

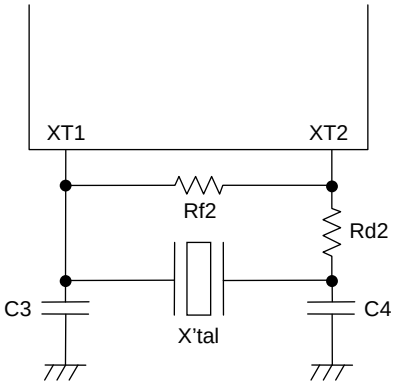


Figure 2 XT Oscillator Circuit

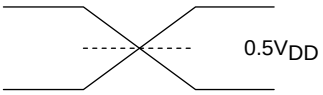
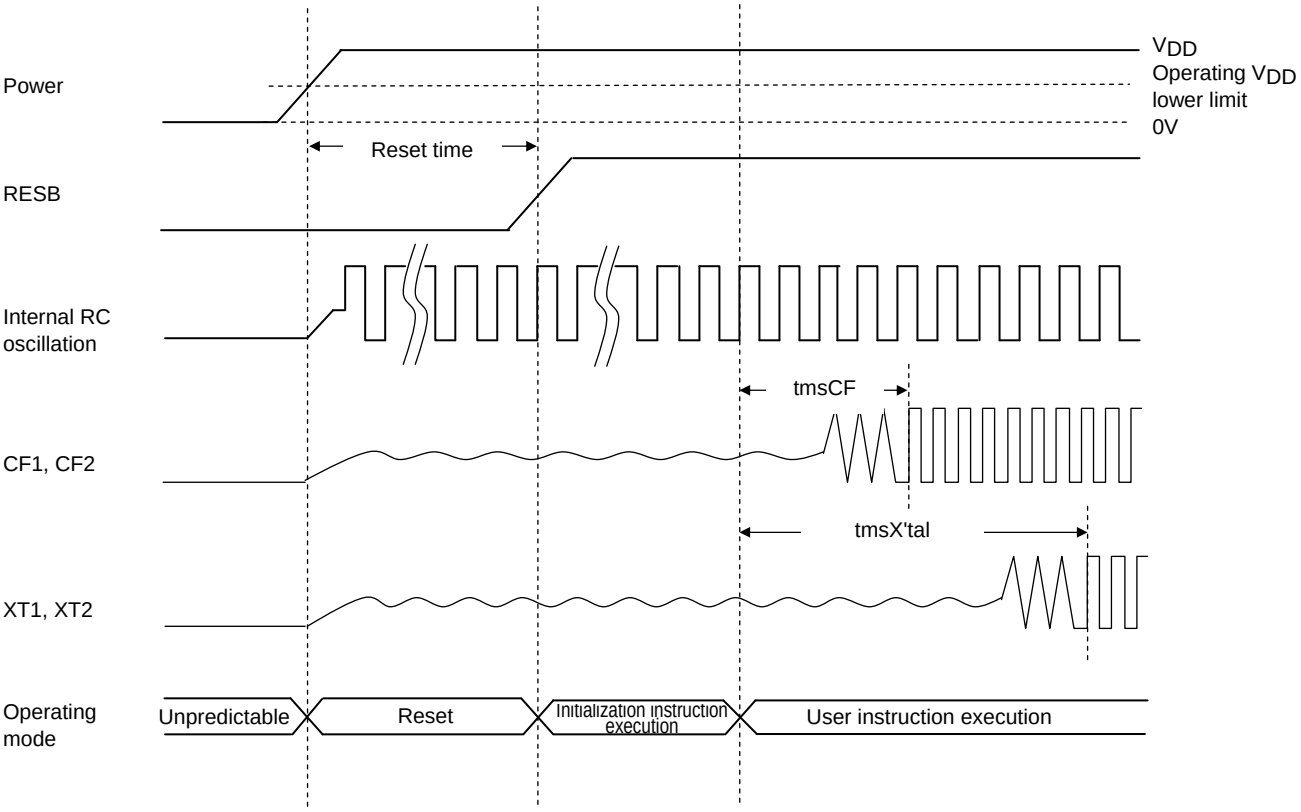
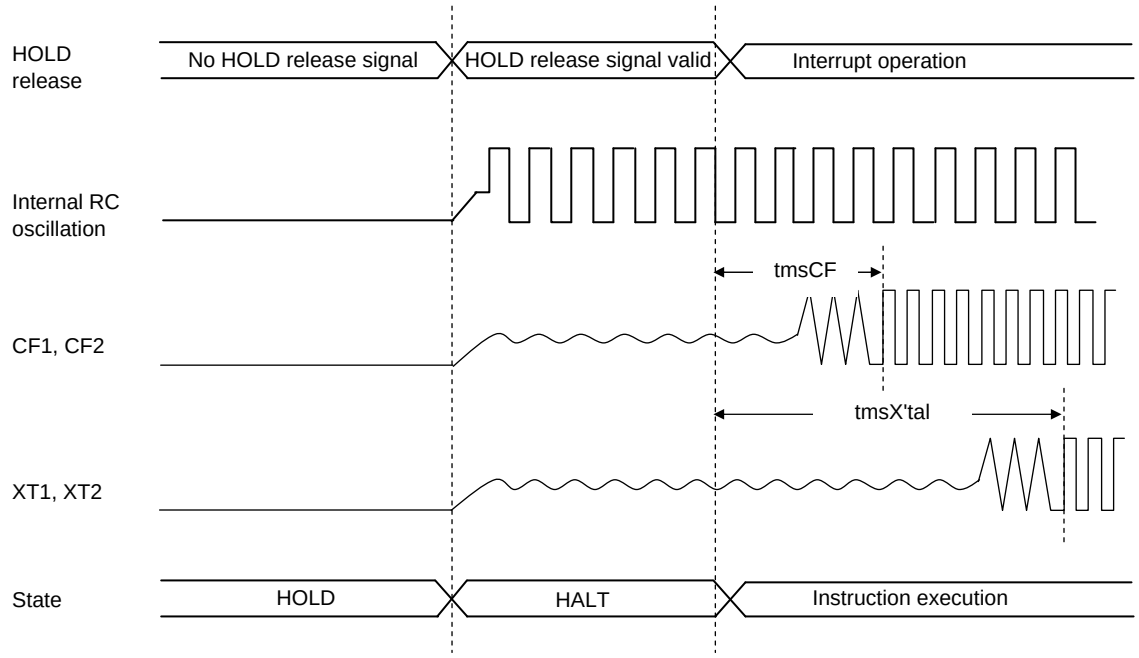


Figure 3 AC Timing Measurement Point

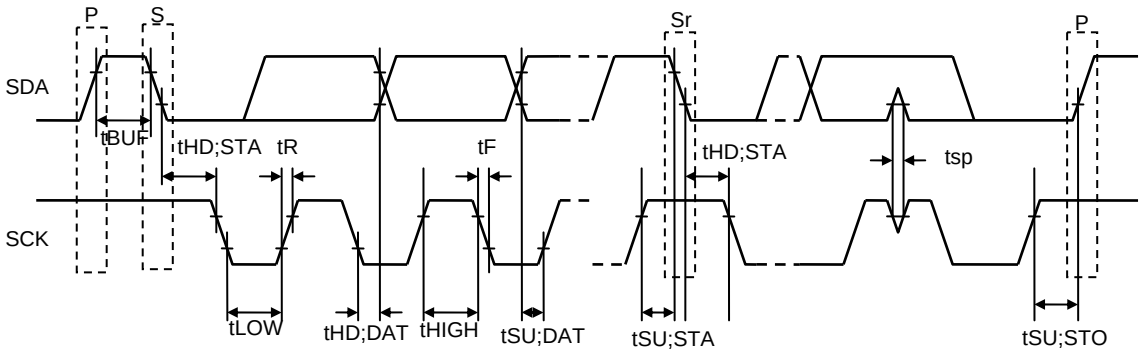


Reset Time and Oscillation Stabilization Time



HOLD Release and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Time Timing Charts



S: Start condition
P: Stop condition
Sr: Restart condition

Figure 8 I^2C Timing

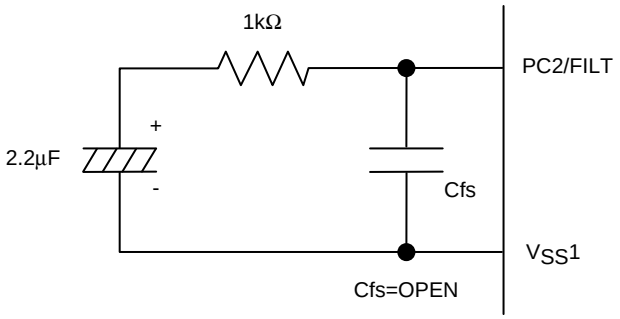


Figure 9 Recommended FILT Circuit
* Take at least 50ms to oscillation to stabilize after PLL is started.