Infineon Technologies - C167CSL16M3VCAFXUMA2 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	11K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	P-MQFP-144-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c167csl16m3vcafxuma2

C167CS-3V

Revision History:	**2001-10**	V1.0
Previous Version:	---	

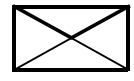
Page	**Subjects (major changes)**

Controller Area Network (CAN): License of Robert Bosch GmbH

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

mcdocu.comments@infineon.com



C167CS-3V

- High Performance 16-bit CPU with 4-Stage Pipeline
  - 125 ns Instruction Cycle Time at 16 MHz CPU Clock
  - 625 ns Multiplication (16 × 16 bit), 1250 ns Division (32/16 bit)
  - Enhanced Boolean Bit Manipulation Facilities
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Single-Cycle Context Switching Support
  - 16 MBytes Total Linear Address Space for Code and Data
  - 1024 Bytes On-Chip Special Function Register Area
- 16-Priority-Level Interrupt System with 56 Sources, Sample-Rate down to 62 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- Clock Generation via on-chip PLL (factors 1:1.5/2/2.5/3/4/5), via prescaler or via direct clock input
- On-Chip Memory Modules
  - 3 KBytes On-Chip Internal RAM (IRAM)
  - 8 KBytes On-Chip Extension RAM (XRAM)
- On-Chip Peripheral Modules
  - 24-Channel 10-bit A/D Converter with Programmable Conversion Time down to 7.8 µs
  - Two 16-Channel Capture/Compare Units
  - 4-Channel PWM Unit
  - Two Multi-Functional General Purpose Timer Units with 5 Timers
  - Two Serial Channels (Synchronous/Asynchronous and High-Speed-Synchronous)
  - Two On-Chip CAN Interfaces (Rev. 2.0B active) with 2 × 15 Message Objects (Full CAN/Basic CAN), can work on one bus with 30 objects
  - On-Chip Real Time Clock
- Up to 16 MBytes External Address Space for Code and Data
  - Programmable External Bus Characteristics for Different Address Ranges
  - Multiplexed or Demultiplexed External Address/Data Buses with 8-Bit or 16-Bit Data Bus Width
  - Five Programmable Chip-Select Signals
  - Hold- and Hold-Acknowledge Bus Arbitration Support
- Idle, Sleep, and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog
- Up to 111 General Purpose I/O Lines, partly with Selectable Input Thresholds and Hysteresis

- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader
- 144-Pin MQFP Package

This document describes several derivatives of the C167 group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

Table 1 C167CS-3V Derivative Synopsis

Derivative[1)]	Program Memory	Operating Frequency
SAB-C167CS-L16M3V	---	16 MHz
SAF-C167CS-L16M3V	---	16 MHz

1) This Data Sheet is valid for devices starting with and including design step BA.

For simplicity all versions are referred to by the term **C167CS-3V** throughout this document.

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the C167CS-3V please refer to the **“Product Catalog Microcontrollers”**, which summarizes all available microcontroller variants.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

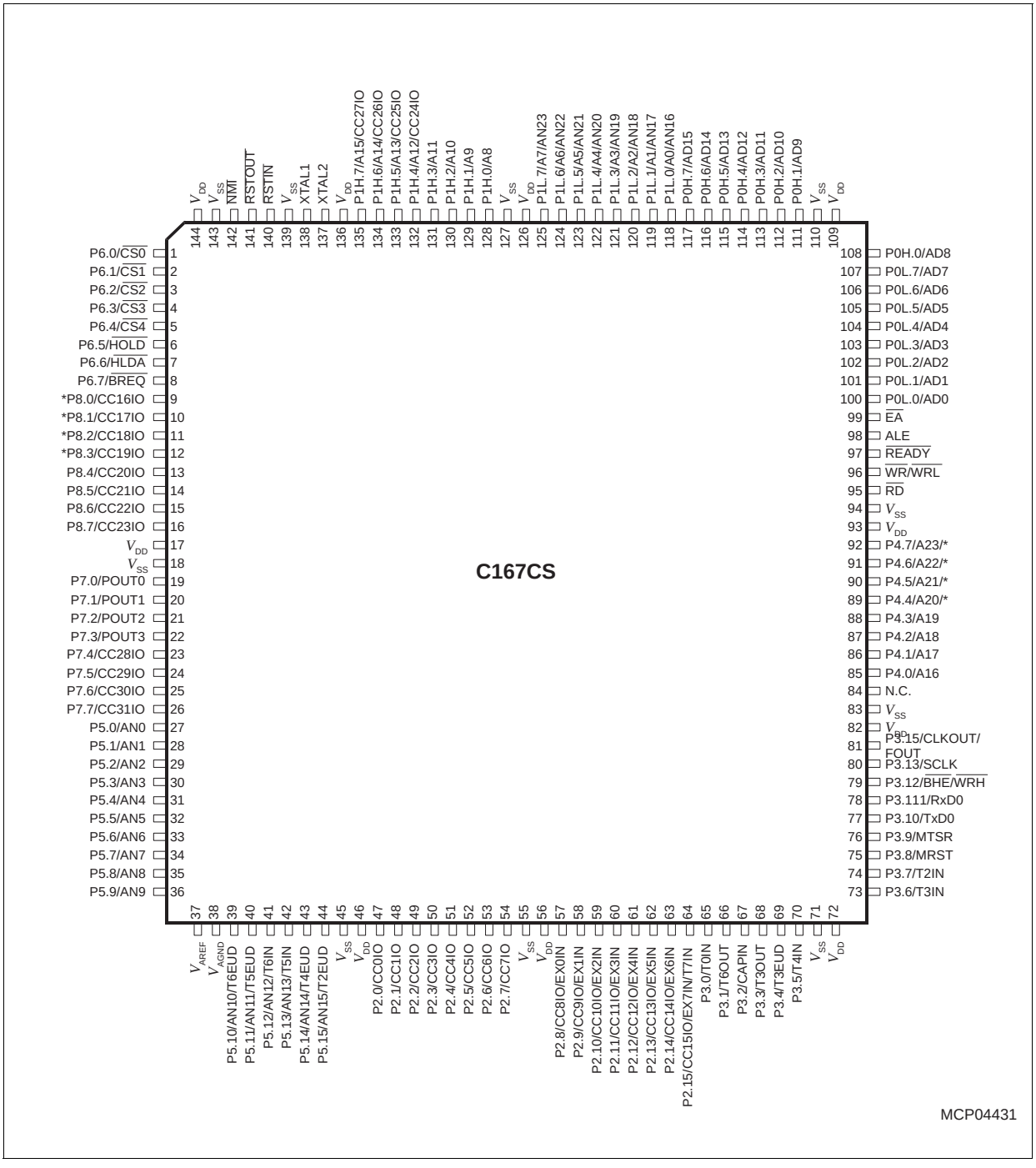


Figure 2

***)** The marked pins of Port 4 and Port 8 can have CAN interface lines assigned to them. **Table 2** on the pages below lists the possible assignments.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function	
P3		IO	Port 3 is a 15-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins also serve for alternate functions:	
P3.0	65	I	T0IN	CAPCOM1 Timer T0 Count Input
P3.1	66	O	T6OUT	GPT2 Timer T6 Toggle Latch Output
P3.2	67	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	68	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	69	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input
P3.5	70	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp
P3.6	73	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	74	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp
P3.8	75	I/O	MRST	SSC Master-Receive/Slave-Transmit Inp./Outp.
P3.9	76	I/O	MTSR	SSC Master-Transmit/Slave-Receive Outp./Inp.
P3.10	77	O	T×D0	ASC0 Clock/Data Output (Async./Sync.)
P3.11	78	I/O	R×D0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.)
P3.12	79	O	$\overline{BHE}$	External Memory High Byte Enable Signal,
		O	$\overline{WRH}$	External Memory High Byte Write Strobe
P3.13	80	I/O	SCLK	SSC Master Clock Output / Slave Clock Input.
P3.15	81	O	CLKOUT	System Clock Output (= CPU Clock)
		O	FOUT	Programmable Frequency Output
NC	84	–	This pin is not connected in the C167CS-3V. No connection to the PCB is required.	

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
PORT1		IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode. The following PORT1 pins also serve for alternate functions:
P1L.0-7	118-125		
P1H.0-7	128-135		
P1L.0	118	I	AN16 Analog Input Channel 16
P1L.1	119	I	AN17 Analog Input Channel 17
P1L.2	120	I	AN18 Analog Input Channel 18
P1L.3	121	I	AN19 Analog Input Channel 19
P1L.4	122	I	AN20 Analog Input Channel 20
P1L.5	123	I	AN21 Analog Input Channel 21
P1L.6	124	I	AN22 Analog Input Channel 22
P1L.7	125	I	AN23 Analog Input Channel 23
P1H.4	132	I/O	CC24IO CAPCOM2: CC24 Capture Inp./Compare Outp.
P1H.5	133	I/O	CC25IO CAPCOM2: CC25 Capture Inp./Compare Outp.
P1H.6	134	I/O	CC26IO CAPCOM2: CC26 Capture Inp./Compare Outp.
P1H.7	135	I/O	CC27IO CAPCOM2: CC27 Capture Inp./Compare Outp.
XTAL2	137	O	XTAL2: Output of the oscillator amplifier circuit.
XTAL1	138	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
V_{DD}	17, 46, 56, 72, 82, 93, 109, 126, 136, 144	–	Digital Supply Voltage: +3.3 V during normal operation and idle mode. ≥2.5 V during power down mode.
V_{SS}	18, 45, 55, 71, 83, 94, 110, 127, 139, 143	–	Digital Ground.

1) The CAN interface lines are assigned to ports P4 and P8 under software control. Within the CAN module several assignments can be selected.

Note: The following behaviour differences must be observed when the bidirectional reset is active:

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT and is cleared automatically after a reset.
- The reset indication flags always indicate a long hardware reset.
- The PORT0 configuration is treated like on a hardware reset. Especially the bootstrap loader may be activated when P0L.4 is low.
- Pin $\overline{\text{RSTIN}}$ may only be connected to external reset devices with an open drain output driver.
- A short hardware reset is extended to the duration of the internal reset sequence.

Functional Description

The architecture of the C167CS-3V combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. In addition the on-chip memory blocks allow the design of compact systems with maximum performance.
The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C167CS-3V.

Note: All time specifications refer to a CPU clock of 16 MHz (see definition in the AC Characteristics section).

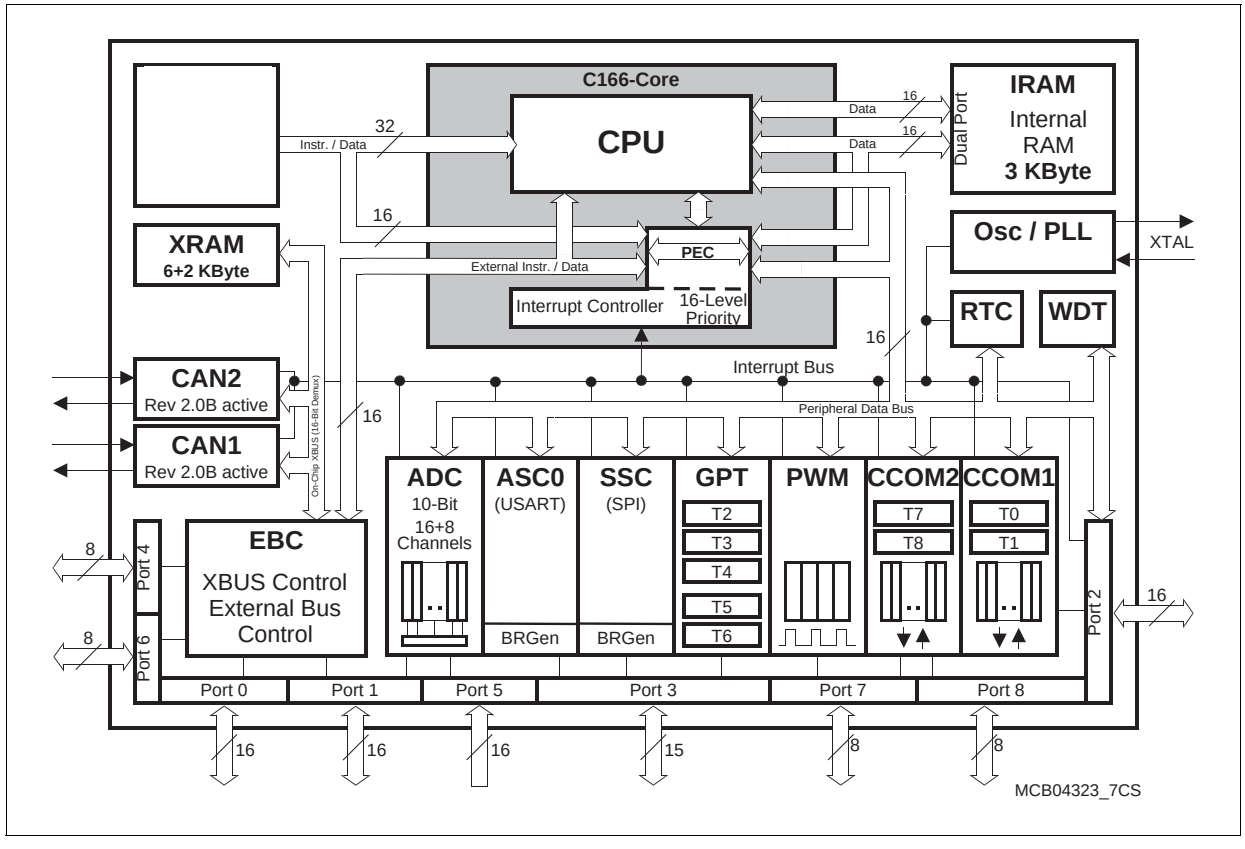


Figure 3 Block Diagram

The program memory, the internal RAM (IRAM) and the set of generic peripherals are connected to the CPU via separate buses. A fourth bus, the XBUS, connects external resources as well as additional on-chip resoures, the X-Peripherals (see **Figure 3**).

The XBUS resources (XRAM, CAN) of the C167CS-3V can be individually enabled or disabled during initialization. Register XPERCON selects the required modules which are then enabled by setting the general X-Peripheral enable bit XPEN (SYSCON.2). Modules that are disabled consume neither address space nor port pins.

Note: The default value of register XPERCON after reset selects 2 KByte XRAM and module CAN1, so the default XBUS resources are compatible with the C167CR.

Table 7 C167CS-3V Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
CC17	$FE62_H$	31_H	CAPCOM Register 17	0000_H
CC17IC **b**	$F162_H$ **E**	$B1_H$	CAPCOM Reg.17 Interrupt Ctrl. Reg.	0000_H
CC18	$FE64_H$	32_H	CAPCOM Register 18	0000_H
CC18IC **b**	$F164_H$ **E**	$B2_H$	CAPCOM Reg. 18 Interrupt Ctrl. Reg.	0000_H
CC19	$FE66_H$	33_H	CAPCOM Register 19	0000_H
CC19IC **b**	$F166_H$ **E**	$B3_H$	CAPCOM Reg. 19 Interrupt Ctrl. Reg.	0000_H
CC1IC **b**	$FF7A_H$	BD_H	CAPCOM Reg.1 Interrupt Ctrl. Reg.	0000_H
CC2	$FE84_H$	42_H	CAPCOM Register 2	0000_H
CC20	$FE68_H$	34_H	CAPCOM Register 20	0000_H
CC20IC **b**	$F168_H$ **E**	$B4_H$	CAPCOM Reg. 20 Interrupt Ctrl. Reg.	0000_H
CC21	$FE6A_H$	35_H	CAPCOM Register 21	0000_H
CC21IC **b**	$F16A_H$ **E**	$B5_H$	CAPCOM Reg. 21 Interrupt Ctrl. Reg.	0000_H
CC22	$FE6C_H$	36_H	CAPCOM Register 22	0000_H
CC22IC **b**	$F16C_H$ **E**	$B6_H$	CAPCOM Reg. 22 Interrupt Ctrl. Reg.	0000_H
CC23	$FE6E_H$	37_H	CAPCOM Register 23	0000_H
CC23IC **b**	$F16E_H$ **E**	$B7_H$	CAPCOM Reg. 23 Interrupt Ctrl. Reg.	0000_H
CC24	$FE70_H$	38_H	CAPCOM Register 24	0000_H
CC24IC **b**	$F170_H$ **E**	$B8_H$	CAPCOM Reg. 24 Interrupt Ctrl. Reg.	0000_H
CC25	$FE72_H$	39_H	CAPCOM Register 25	0000_H
CC25IC **b**	$F172_H$ **E**	$B9_H$	CAPCOM Reg. 25 Interrupt Ctrl. Reg.	0000_H
CC26	$FE74_H$	$3A_H$	CAPCOM Register 26	0000_H
CC26IC **b**	$F174_H$ **E**	BA_H	CAPCOM Reg. 26 Interrupt Ctrl. Reg.	0000_H
CC27	$FE76_H$	$3B_H$	CAPCOM Register 27	0000_H
CC27IC **b**	$F176_H$ **E**	BB_H	CAPCOM Reg. 27 Interrupt Ctrl. Reg.	0000_H
CC28	$FE78_H$	$3C_H$	CAPCOM Register 28	0000_H
CC28IC **b**	$F178_H$ **E**	BC_H	CAPCOM Reg. 28 Interrupt Ctrl. Reg.	0000_H
CC29	$FE7A_H$	$3D_H$	CAPCOM Register 29	0000_H
CC29IC **b**	$F184_H$ **E**	$C2_H$	CAPCOM Reg. 29 Interrupt Ctrl. Reg.	0000_H
CC2IC **b**	$FF7C_H$	BE_H	CAPCOM Reg. 2 Interrupt Ctrl. Reg.	0000_H
CC3	$FE86_H$	43_H	CAPCOM Register 3	0000_H

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C167CS-3V. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 9 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Digital supply voltage	V_{DD}	3.15	3.6	V	Active mode, f_{CPUmax} = 16 MHz
		2.5[1)]	3.6	V	PowerDown mode
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	–	±5	mA	Per pin[2)3)]
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	–	50	mA	[3)]
External Load Capacitance	C_L	–	50	pF	Pin drivers in **fast edge** mode[4)]
Ambient temperature	T_A	0	70	°C	SAB-C167CS-3V …
		-40	85	°C	SAF-C167CS-3V …
		-40	125	°C	SAK-C167CS-3V …

1) Output voltages and output currents will be reduced when V_{DD} leaves the range defined for active mode.

2) Overload conditions occur if the standard operatings conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD}$+0.5 V or $V_{OV} < V_{SS}$-0.5 V). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltage must remain within the specified limits. Proper operation is not guaranteed if overload conditions occur on functional pins line XTAL1, $\overline{RD}$, $\overline{WR}$, etc.

3) Not 100% tested, guaranteed by design and characterization.

4) The timing is valid for pin drivers in high current or dynamic current mode. The reduced static output current in dynamic current mode must be respected when designing the system.

Table 10 Current Limits for Port Output Drivers

Port Output Driver	Maximum Output Current (I_{OLmax}, $-I_{OHmax}$)[1]	Nominal Output Current (I_{OLnom}, $-I_{OHnom}$)
(PORT0, PORT1, Port 2, Port 4, ALE, RD, WR, BHE, CLKOUT, RSTOUT, RSTIN[2])	-----	1.6 mA
All other outputs	-----	0.5 mA

1) An output current above $|I_{OXnom}|$ is not specified for the C167CS-3V.

2) Valid for V_{OL} in bidirectional reset mode only.

Power Consumption C167CS-3V

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Power supply current (active) with all peripherals active	I_{DD3}	–	$10 + 2.0 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IL}$, f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals active	I_{IDX3}[2]	–	$5 + 1.1 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IH1}$, f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals deactivated, PLL off, SDD factor = 32	I_{IDO}[3)2)]	–	$500 + 50 \times f_{OSC}$	µA	$\overline{RSTIN} = V_{IH1}$, f_{OSC} in [MHz][1]
Sleep and Power-down mode supply current with RTC running	I_{PDR}[3)2)]	–	$500 + 30 \times f_{OSC}$	µA	$V_{DD} = V_{DDmax}$, f_{OSC} in [MHz][4]
Sleep and Power-down mode supply current with RTC disabled	I_{PDO}	–	30	µA	$V_{DD} = V_{DDmax}$[4]

1) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 10**. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

2) These values are not 100% tested but verified by means of system characterization.

3) This parameter is determined mainly by the current consumed by the oscillator (see **Figure 9**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The values given refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry (see also application notes AP2420: Crystal Oscillator, AP2424: Ceramic Resonator Oscillator).

4) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} - 0.1 V to V_{DD}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

P0.15-13 (P0H.7-5). Register RP0H can be loaded from the upper half of register RSTCON under software control.

Table 11 associates the combinations of these three bits with the respective clock generation mode.

Table 11 C167CS-3V Clock Generation Modes

CLKCFG (RP0H.7-5)	CPU Frequency $f_{CPU} = f_{OSC} \times F$	External Clock Input Range[1)]	Notes
1 1 1	$f_{OSC} \times 4$	2.5 to 4 MHz	Default configuration
1 1 0	$f_{OSC} \times 3$	3.33 to 5.33 MHz	–
1 0 1	$f_{OSC} \times 2$	5 to 8 MHz	–
1 0 0	$f_{OSC} \times 5$	2 to 3.2 MHz	–
0 1 1	$f_{OSC} \times 1$	1 to 16 MHz	Direct drive[2)]
0 1 0	$f_{OSC} \times 1.5$	6.66 to 10.66 MHz	–
0 0 1	$f_{OSC} / 2$	2 to 32 MHz	CPU clock via prescaler
0 0 0	$f_{OSC} \times 2.5$	4 to 6.4 MHz	–

1) The external clock input range refers to a CPU clock range of 10 … 16 MHz.

2) The maximum frequency depends on the duty cycle of the external clock signal.

Prescaler Operation

When prescaler operation is configured (CLKCFG=001_B) the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.
The frequency of f_{CPU} is half the frequency of f_{OSC} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{OSC}.

The timings listed in the AC Characteristics that refer to TCLs therefore can be calculated using the period of f_{OSC} for any TCL.

Phase Locked Loop

When PLL operation is configured (via CLKCFG) the on-chip phase locked loop is enabled and provides the CPU clock (see table above). The PLL multiplies the input frequency by the factor **F** which is selected via the combination of pins P0.15-13 (i.e. $f_{CPU} = f_{OSC} \times$ **F**). With every **F**'th transition of f_{OSC} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, i.e. the CPU clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{OSC}. The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

Direct Drive

When direct drive is configured (CLKCFG = 011_B) the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.

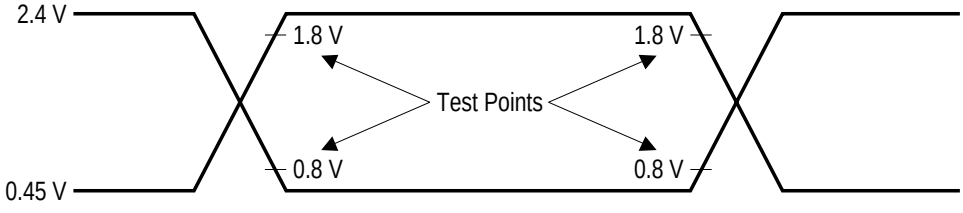
The frequency of f_{CPU} directly follows the frequency of f_{OSC} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{OSC}.

The timings listed below that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances. This minimum value can be calculated via the following formula:

$$TCL_{min} = 1/f_{OSC} \times DC_{min} \qquad \text{(DC = duty cycle)}$$

For two consecutive TCLs the deviation caused by the duty cycle of f_{OSC} is compensated so the duration of 2TCL is always $1/f_{OSC}$. The minimum value TCL_{min} therefore has to be used only once for timings that require an odd number of TCLs (1, 3, …). Timings that require an even number of TCLs (2, 4, …) may use the formula $2TCL = 1/f_{OSC}$.

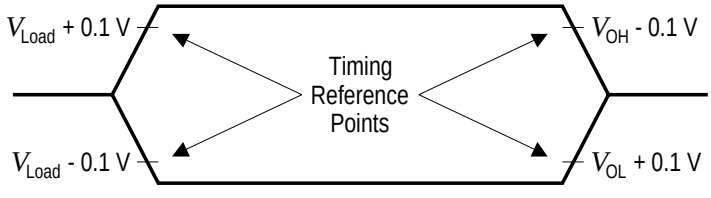
Testing Waveforms



AC inputs during testing are driven at 2.4 V for a logic '1' and 0.45 V for a logic '0'.
Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

MCA04414

Figure 14 Input Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH} / V_{OL} level occurs (I_{OH} / I_{OL} = 20 mA).

MCA00763

Figure 15 Float Waveforms

interdependencies between certain parameters. Some of these interdependencies are described as relative timing (see below) or in additional notes (see standard timing).

Table 18 External Bus Relative Timing (Operating Conditions apply) [1)]

Parameter	Symbol		Limits		Unit
			min.	max.	
Output hold time after $\overline{WR}$ rising edge [2)] Valid for: address, write data out	t_{50}	CC	0	–	ns
Input hold time after $\overline{RD}$ rising edge Valid for: read data in	t_{51}	SR	–	0	ns

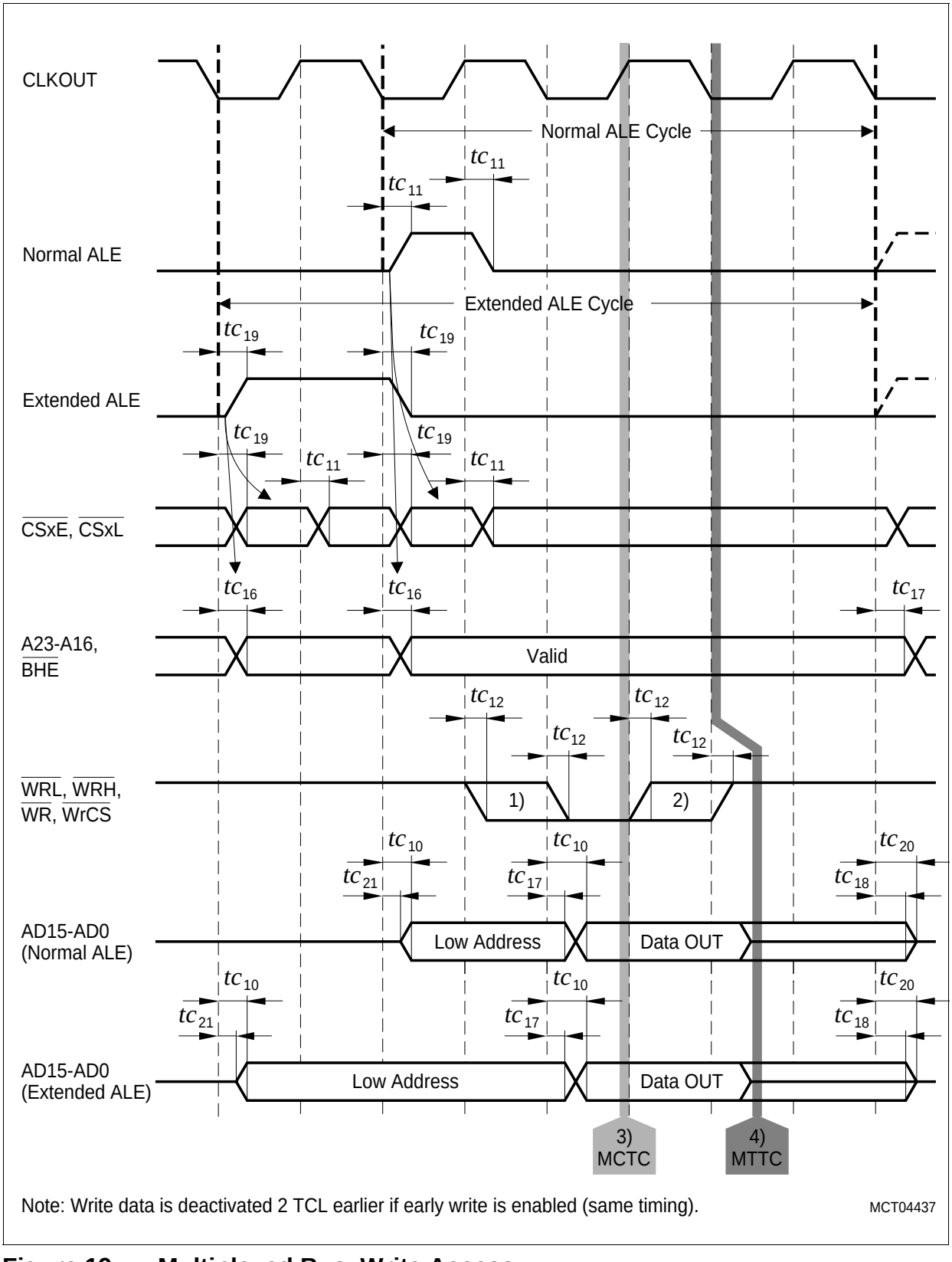
1) Not 100% tested, guaranteed by design and characterization.

2) See also note 2) in **Table 17**.

General Notes For The Following Bus Timing Figures

These standard notes apply to all subsequent timing figures. Additional individual notes are placed at the respective figure.

1) The falling edge of signals $\overline{RD}$ and $\overline{WR}$/$\overline{WRH}$/$\overline{WRL}$/$\overline{WrCS}$ is controlled by the Read/Write delay feature (bit BUSCON.RWDCx).
2) The rising edge of signal $\overline{WR}$/$\overline{WRH}$/$\overline{WRL}$/$\overline{WrCS}$ is controlled by the early write feature (bit BUSCON.EWENx).
3) A bus cycle is extended here, if MCTC waitstates are selected or if the $\overline{READY}$ input is sampled inactive.
4) A bus cycle is extended here, if an MTTC waitstate is selected.



Note: Write data is deactivated 2 TCL earlier if early write is enabled (same timing).

MCT04437

Figure 19 Multiplexed Bus, Write Access

External Bus Arbitration

Table 20 Bus Arbitration Timing (Operating Conditions apply)

Parameter	Symbol		Limits		Unit
			min.	max.	
$\overline{\text{HOLD}}$ input setup time to CLKOUT falling edge	tc_{28}	SR	18	–	ns
CLKOUT to $\overline{\text{BREQ}}$ delay	tc_{29}	CC	-2	9	ns
CLKOUT to $\overline{\text{HLDA}}$ delay	tc_{30}	CC	-2	7	ns
$\overline{\text{CSx}}$ release[1)]	tc_{31}	CC	0	10	ns
$\overline{\text{CSx}}$ drive	tc_{32}	CC	-4	4	ns
Other signals release[1)]	tc_{33}	CC	0	10	ns
Other signals drive[1)]	tc_{34}	CC	0	6	ns

1) Not 100% tested, guaranteed by design and characterization.

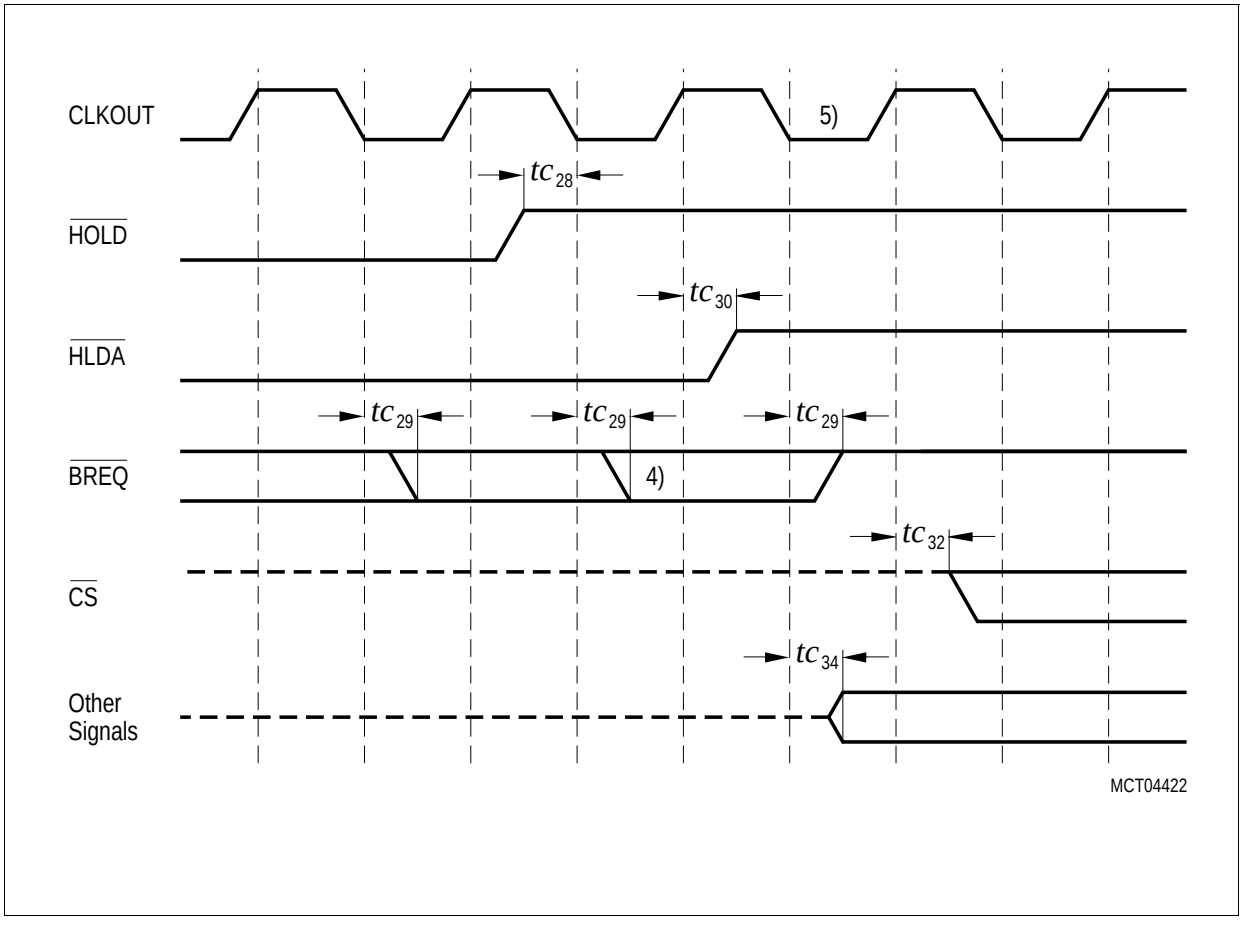


Figure 23 External Bus Arbitration, (Regaining the Bus)

Notes

4) This is the last chance for $\overline{\text{BREQ}}$ to trigger the indicated regain-sequence.
Even if $\overline{\text{BREQ}}$ is activated earlier, the regain-sequence is initiated by $\overline{\text{HOLD}}$ going high.
Please note that $\overline{\text{HOLD}}$ may also be deactivated without the C167CS-3V requesting the bus.

5) The next C167CS-3V driven bus cycle may start here.

External XRAM Access

If XPER-Share mode is enabled the on-chip XRAM of the C167CS-3V can be accessed (during hold states) by an external master like an asynchronous SRAM.

Table 21 XRAM Access Timing (Operating Conditions apply)

Parameter		Symbol		Limits		Unit
				min	max	
Address setup time before $\overline{RD}$/$\overline{WR}$ falling edge		t_{40}	SR	5	–	ns
Address hold time after $\overline{RD}$/$\overline{WR}$ rising edge		t_{41}	SR	0	–	ns
Data turn on delay after $\overline{RD}$ falling edge	Read	t_{42}	CC	2	–	ns
Data output valid delay after address latched	Read	t_{43}	CC	–	57	ns
Data turn off delay after $\overline{RD}$ rising edge	Read	t_{44}	CC	0	10	ns
Write data setup time before $\overline{WR}$ rising edge	Write	t_{45}	SR	10	–	ns
Write data hold time after $\overline{WR}$ rising edge	Write	t_{46}	SR	4	–	ns
$\overline{WR}$ pulse width	Write	t_{47}	SR	20	–	ns
$\overline{WR}$ signal recovery time	Write	t_{48}	SR	t_{40}	–	ns

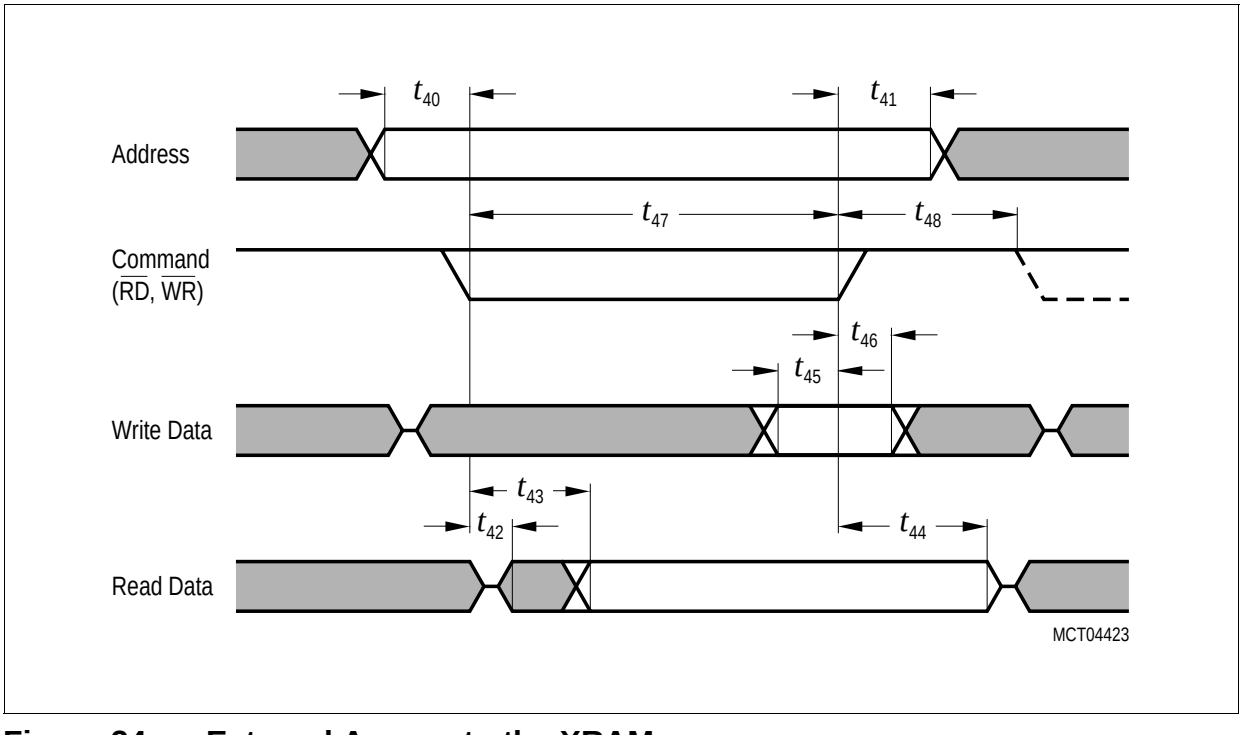
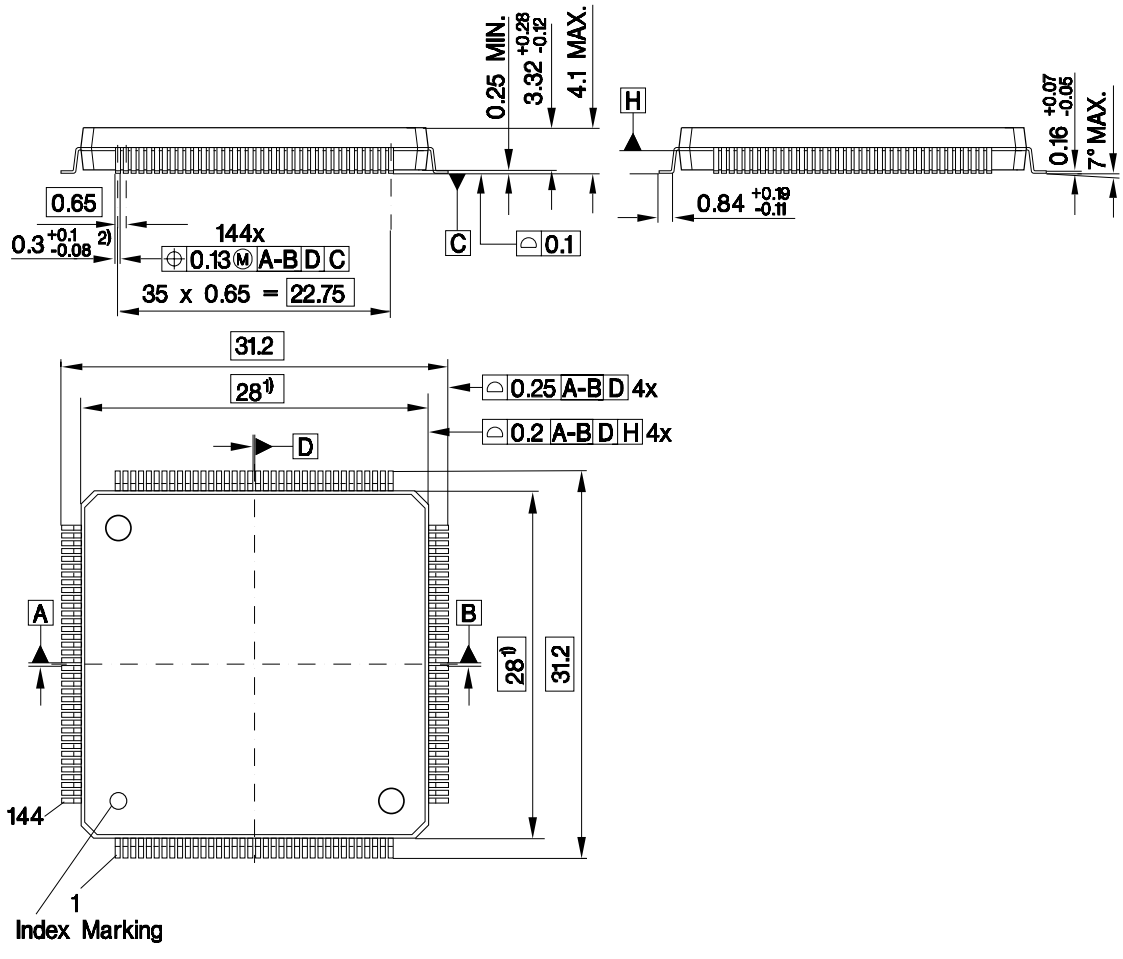


Figure 24 External Access to the XRAM

Package Outlines

P-MQFP-144-6
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm