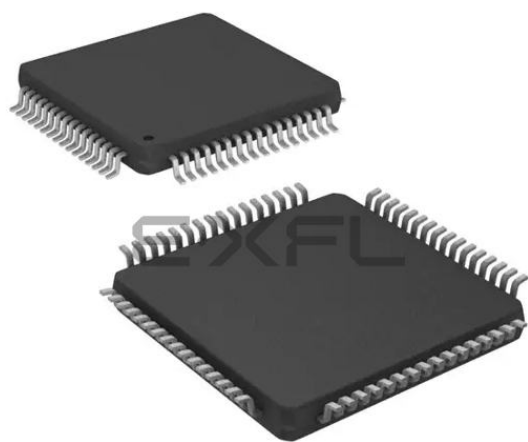




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Details

Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 8x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg842f8-qfp64t

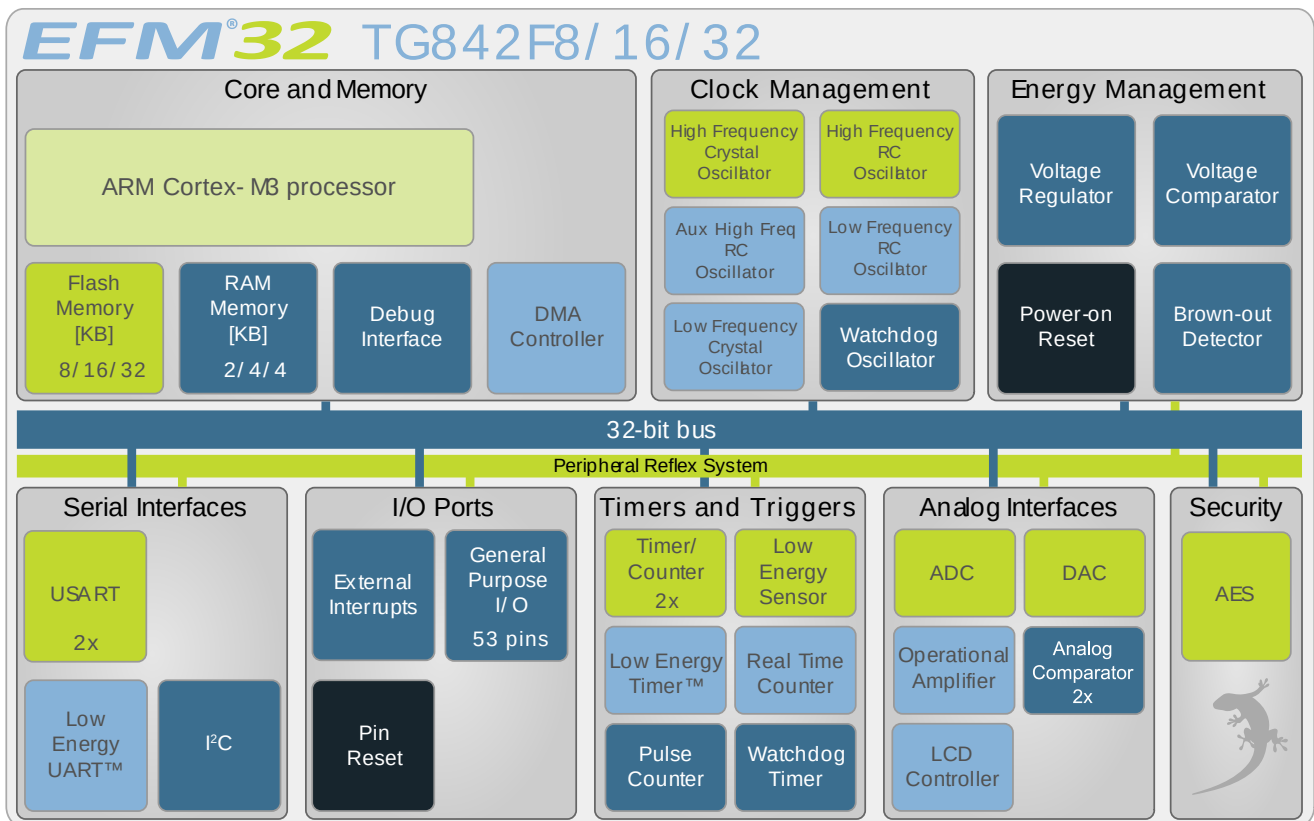
2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32TG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32TG842 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32TG Reference Manual*.

A block diagram of the EFM32TG842 is shown in Figure 2.1 (p. 3) .

Figure 2.1. Block Diagram



2.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EFM32 implementation of the Cortex-M3 is described in detail in *EFM32 Cortex-M3 Reference Manual*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface . In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32TG microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is

divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 μ DMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32TG.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32TG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32TG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

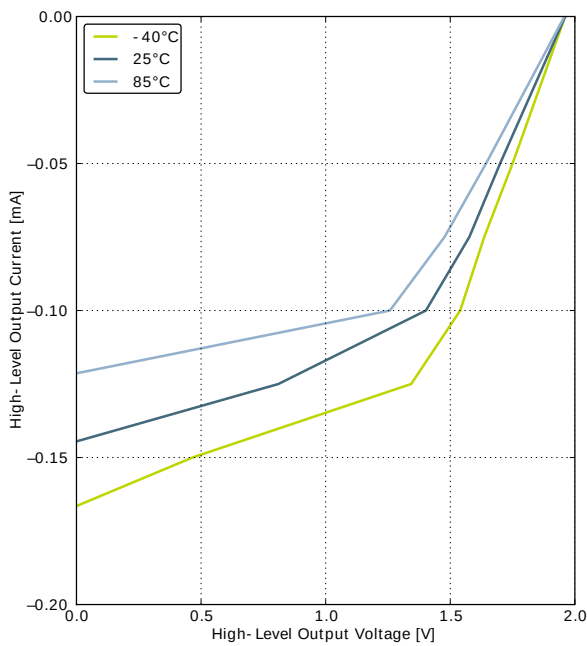
The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

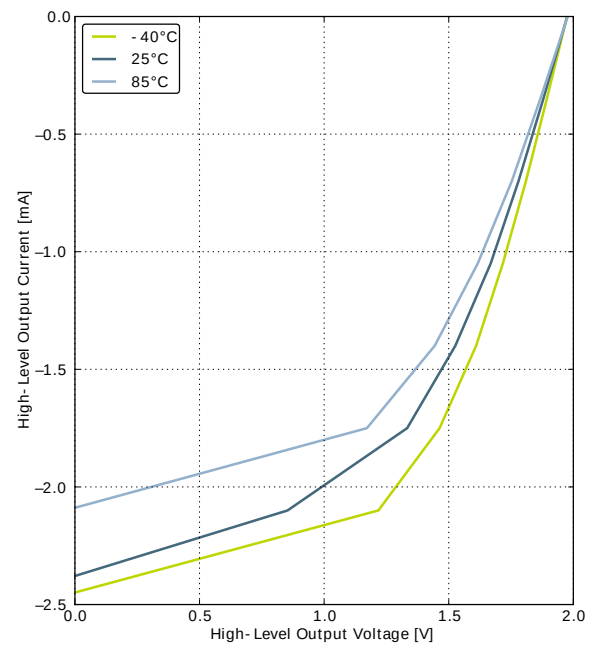
The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 Inter-Integrated Circuit Interface (I2C)

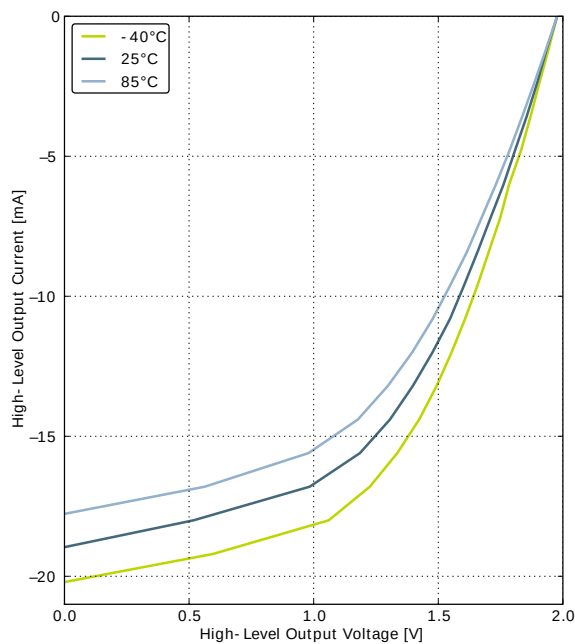
The I²C module provides an interface between the MCU and a serial I²C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I²C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

Figure 3.5. Typical High-Level Output Current, 2V Supply Voltage

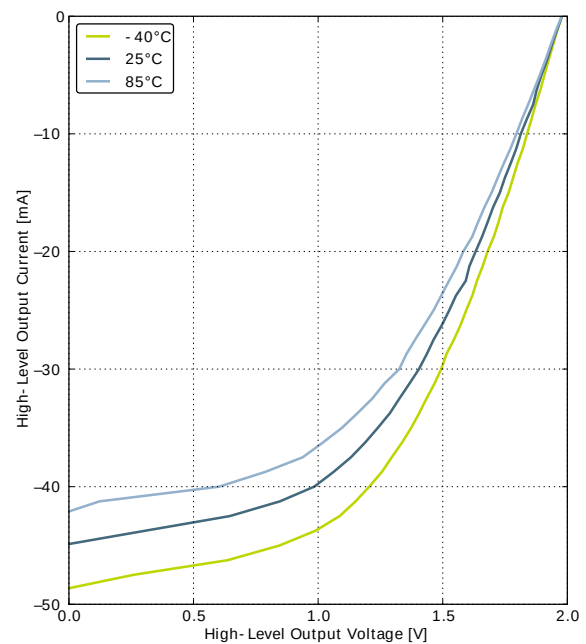
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

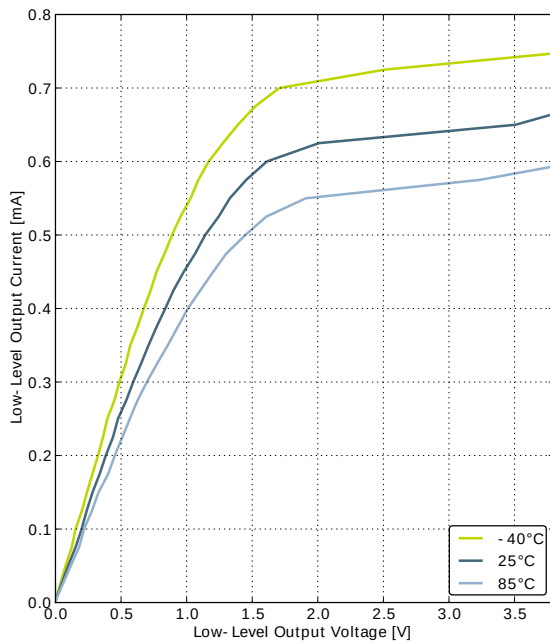


GPIO_Px_CTRL DRIVEMODE = STANDARD

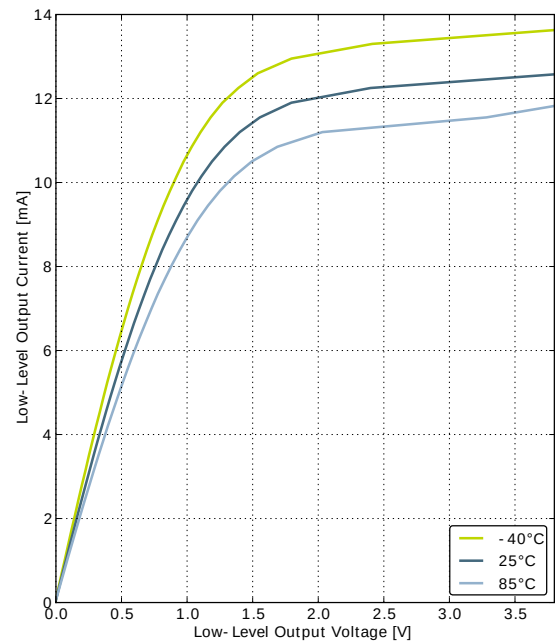


GPIO_Px_CTRL DRIVEMODE = HIGH

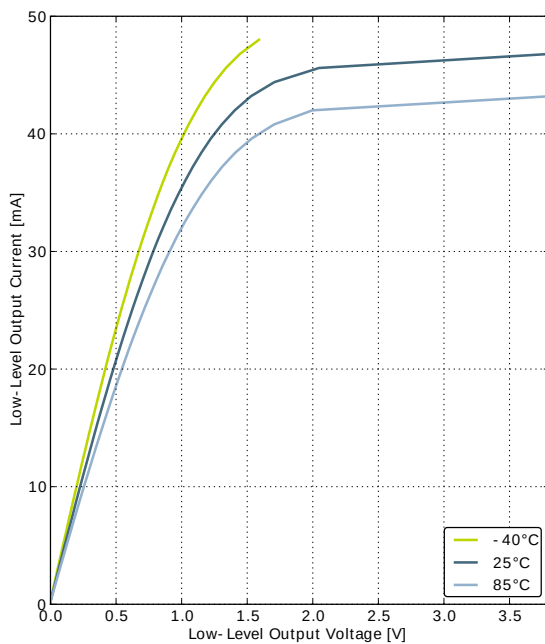
Figure 3.8. Typical Low-Level Output Current, 3.8V Supply Voltage



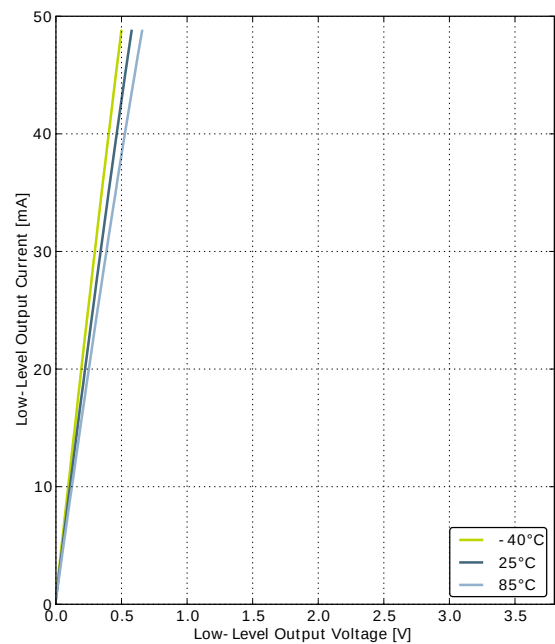
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

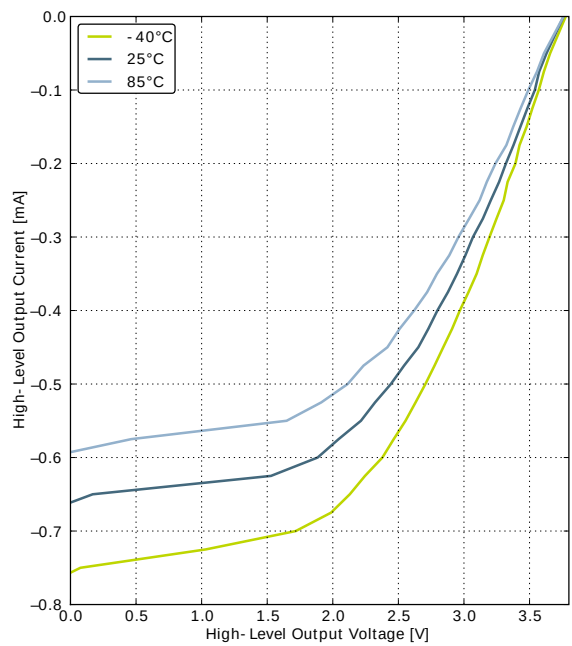


GPIO_Px_CTRL DRIVEMODE = STANDARD

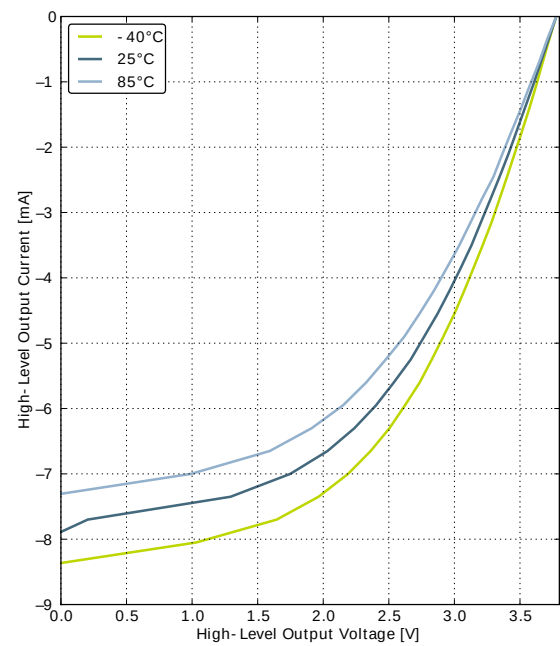


GPIO_Px_CTRL DRIVEMODE = HIGH

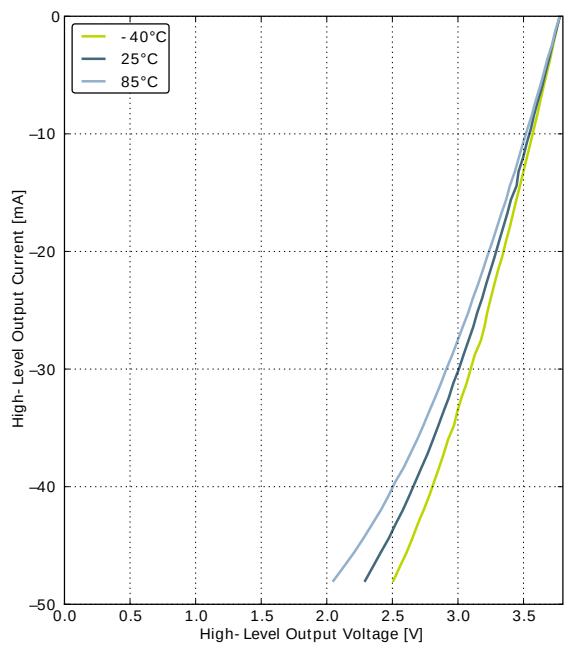
Figure 3.9. Typical High-Level Output Current, 3.8V Supply Voltage



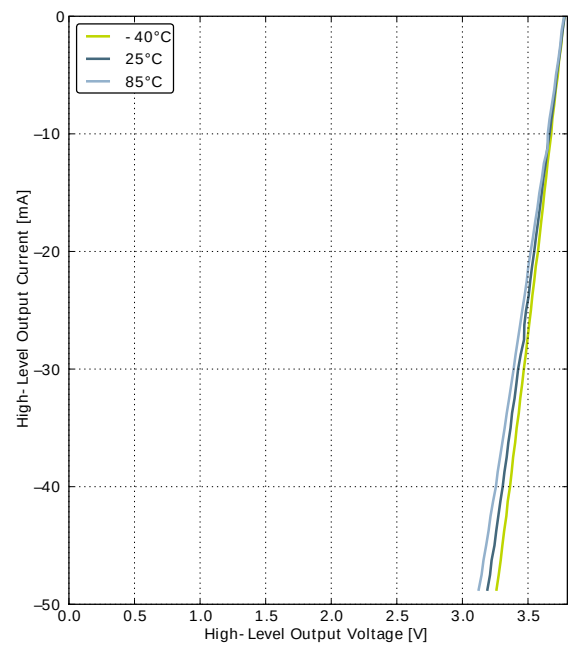
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.8. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR_{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C_{LFXOL}	Supported crystal external load range		$\times^1$		25	pF
I_{LFXO}	Current consumption for core and buffer after startup.	ESR=30 kOhm, C_L =10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t_{LFXO}	Start- up time.	ESR=30 kOhm, C_L =10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

¹See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in energyAware Designer in Simplicity Studio

For safe startup of a given crystal, the energyAware Designer in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

3.9.2 HFXO

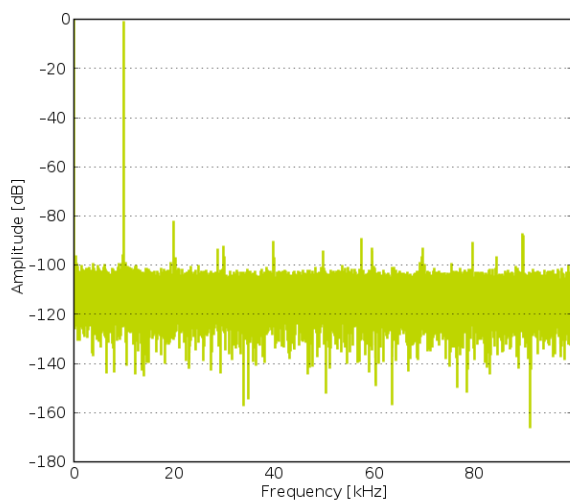
Table 3.9. HFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFXO}	Supported nominal crystal Frequency		4		32	MHz
ESR_{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 32 MHz		30	60	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g_{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C_{HFXOL}	Supported crystal external load range		5		25	pF
I_{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C_L =20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		μ A
		32 MHz: ESR=30 Ohm, C_L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		μ A
t_{HFXO}	Startup time	32 MHz: ESR=30 Ohm, C_L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		400		μ s

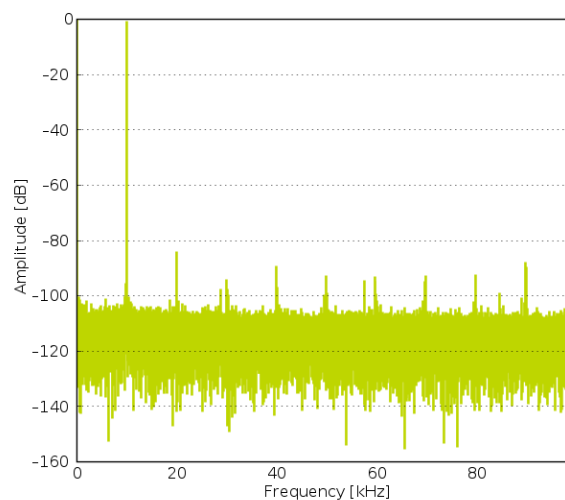
Symbol	Parameter	Condition	Min	Typ	Max	Unit
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference		69		dB
		200 kSamples/s, 12 bit, differential, $2 \times V_{DD}$ reference		70		dB
SINAD _{ADC}	Signal-to-Noise And Distortion-ratio (SINAD)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		64		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differential, $2 \times V_{DD}$ reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	68		dB
		200 kSamples/s, 12 bit, differential, $2 \times V_{DD}$ reference		69		dB
SFDR _{ADC}	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc

3.10.1 Typical performance

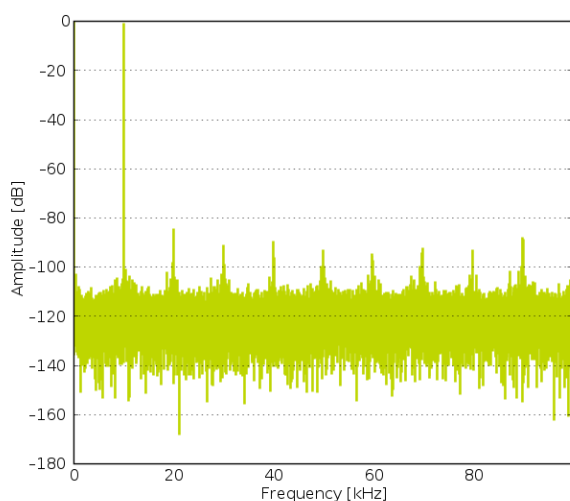
Figure 3.19. ADC Frequency Spectrum, $V_{dd} = 3V$, Temp = 25°C



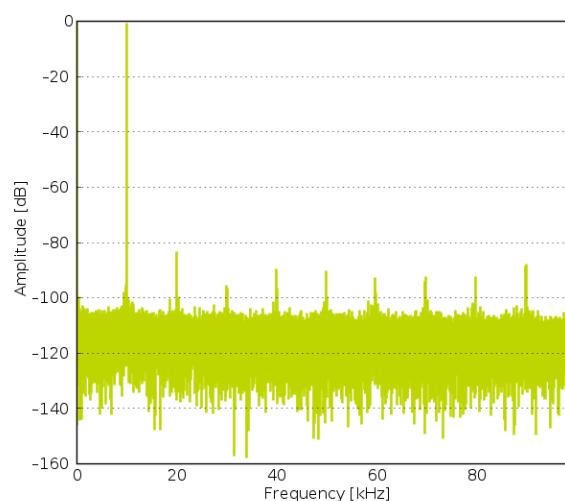
1.25V Reference



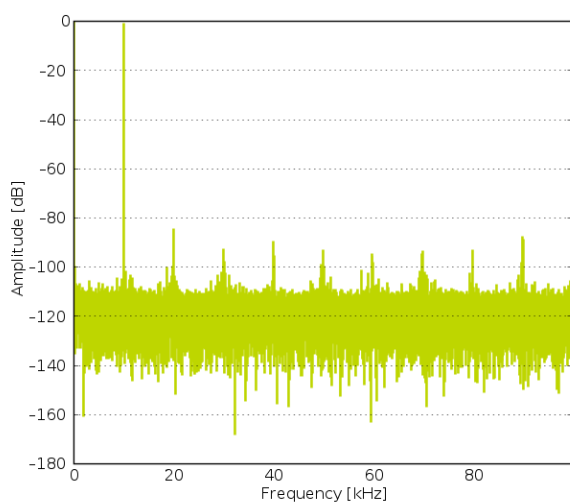
2.5V Reference



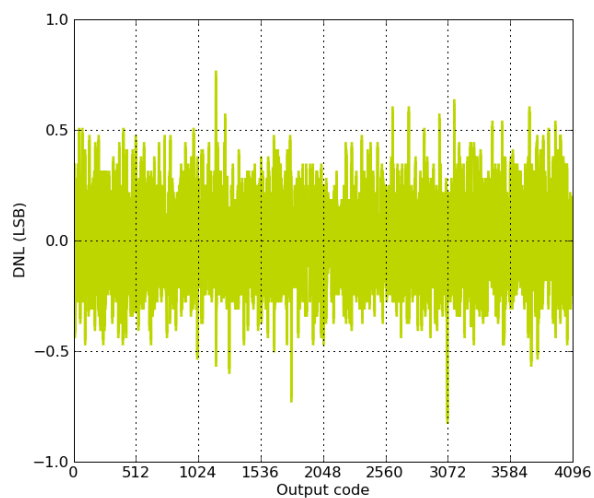
2XVDDVSS Reference



5VDIFF Reference



VDD Reference

Figure 3.21. ADC Differential Linearity Error vs Code, V_{dd} = 3V, Temp = 25°C**1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{DAC}	DAC clock frequency	Continuous Mode			1000	kHz
		Sample/Hold Mode			250	kHz
		Sample/Off Mode			250	kHz
$CYC_{DACCONV}$	Clock cycles per conversion			2		
$t_{DACCONV}$	Conversion time		2			μs
$t_{DACSETTLE}$	Settling time			5		μs
SNR_{DAC}	Signal to Noise Ratio (SNR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		59		dB
$SNDR_{DAC}$	Signal to Noise-pulse Distortion Ratio (SNDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		57		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		54		dB
$SFDR_{DAC}$	Spurious-Free Dynamic Range(SFDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dBc
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		56		dBc
$V_{DACOFFSET}$	Offset voltage	After calibration, single ended		2		mV
DNL_{DAC}	Differential non-linearity	$V_{DD} = 3.0 V$, V_{DD} reference		± 1		LSB
INL_{DAC}	Integral non-linearity	$V_{DD} = 3.0 V$, V_{DD} reference		± 5		LSB
MC_{DAC}	No missing codes			12		bits

3.12 Operational Amplifier (OPAMP)

The electrical characteristics for the Operational Amplifiers are based on simulations.

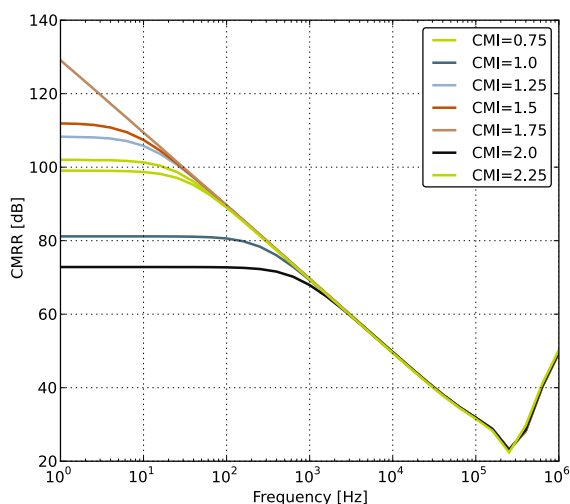
Table 3.16. OPAMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{OPAMP}	Active Current	OPA2 BIASPROG=0xF, HALFBIAS=0x0, Unity Gain		350	405	μA
		OPA2 BIASPROG=0x7, HALFBIAS=0x1, Unity Gain		95	115	μA
		OPA2 BIASPROG=0x0, HALFBIAS=0x1, Unity Gain		13	17	μA
G_{OL}	Open Loop Gain	OPA2 BIASPROG=0xF, HALFBIAS=0x0		101		dB
		OPA2 BIASPROG=0x7, HALFBIAS=0x1		98		dB
		OPA2 BIASPROG=0x0, HALFBIAS=0x1		91		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
GBW _{OPAMP}	Gain Bandwidth Product	OPA0/OPA1 BIASPROG=0xF, HALFBIAS=0x0		16.36		MHz
		OPA0/OPA1 BIASPROG=0x7, HALFBIAS=0x1		0.81		MHz
		OPA0/OPA1 BIASPROG=0x0, HALFBIAS=0x1		0.11		MHz
		OPA2 BIASPROG=0xF, HALFBIAS=0x0		2.11		MHz
		OPA2 BIASPROG=0x7, HALFBIAS=0x1		0.72		MHz
		OPA2 BIASPROG=0x0, HALFBIAS=0x1		0.09		MHz
PM _{OPAMP}	Phase Margin	BIASPROG=0xF, HALFBIAS=0x0, C _L =75 pF		64		°
		BIASPROG=0x7, HALFBIAS=0x1, C _L =75 pF		58		°
		BIASPROG=0x0, HALFBIAS=0x1, C _L =75 pF		58		°
R _{INPUT}	Input Resistance			100		Mohm
R _{LOAD}	Load Resistance	OPA0/OPA1	200			Ohm
		OPA2	2000			Ohm
I _{LOAD_DC}	Load Current	OPA0/OPA1			11	mA
		OPA2			1.5	mA
V _{INPUT}	Input Voltage	OPAxHCMDIS=0	V _{SS}		V _{DD}	V
		OPAxHCMDIS=1	V _{SS}		V _{DD} -1.2	V
V _{OUTPUT}	Output Voltage		V _{SS}		V _{DD}	V
V _{OFFSET}	Input Offset Voltage	Unity Gain, V _{SS} <V _{in} <V _{DD} , OPAxHCMDIS=0		6		mV
		Unity Gain, V _{SS} <V _{in} <V _{DD} -1.2, OPAxHCMDIS=1		1		mV
V _{OFFSET_DRIFT}	Input Offset Voltage Drift				0.02	mV/°C
SR _{OPAMP}	Slew Rate	OPA0/OPA1 BIASPROG=0xF, HALFBIAS=0x0		46.11		V/μs
		OPA0/OPA1 BIASPROG=0x7, HALFBIAS=0x1		1.21		V/μs
		OPA0/OPA1 BIASPROG=0x0, HALFBIAS=0x1		0.16		V/μs
		OPA2 BIASPROG=0xF, HALFBIAS=0x0		4.43		V/μs
		OPA2 BIASPROG=0x7, HALFBIAS=0x1		1.30		V/μs
		OPA2 BIASPROG=0x0, HALFBIAS=0x1		0.16		V/μs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PU _{OPAMP}	Power-up Time	OPA0/OPA1 BIASPROG=0xF, HALFBIAS=0x0		0.09		μs
		OPA0/OPA1 BIASPROG=0x7, HALFBIAS=0x1		1.52		μs
		OPA0/OPA1 BIASPROG=0x0, HALFBIAS=0x1		12.74		μs
		OPA2 BIASPROG=0xF, HALFBIAS=0x0		0.09		μs
		OPA2 BIASPROG=0x7, HALFBIAS=0x1		0.13		μs
		OPA2 BIASPROG=0x0, HALFBIAS=0x1		0.17		μs
N _{OPAMP}	Voltage Noise	V _{out} =1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAX- HCMDIS=0		101		μV _{RMS}
		V _{out} =1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAX- HCMDIS=1		141		μV _{RMS}
		V _{out} =1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAXHCMDIS=0		196		μV _{RMS}
		V _{out} =1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAXHCMDIS=1		229		μV _{RMS}
		RESSEL=7, 0.1 Hz<f<10 kHz, OPAXHCMDIS=0		1230		μV _{RMS}
		RESSEL=7, 0.1 Hz<f<10 kHz, OPAXHCMDIS=1		2130		μV _{RMS}
		RESSEL=7, 0.1 Hz<f<1 MHz, OPAXHCMDIS=0		1630		μV _{RMS}
		RESSEL=7, 0.1 Hz<f<1 MHz, OPAXHCMDIS=1		2590		μV _{RMS}

Figure 3.24. OPAMP Common Mode Rejection Ratio



3.13 Analog Comparator (ACMP)

Table 3.17. ACMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ACMPIN}	Input voltage range		0		V_{DD}	V
V_{ACMPCM}	ACMP Common Mode voltage range		0		V_{DD}	V
I_{ACMP}	Active current	BIASPROG=0b0000, FULL-BIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1	0.6	μA
		BIASPROG=0b1111, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87	12	μA
		BIASPROG=0b1111, FULL-BIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195	520	μA
$I_{ACMPREF}$	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0.0	0.5	μA
		Internal voltage reference		2.15	3.00	μA
$V_{ACMPOFFSET}$	Offset voltage	BIASPROG= 0b1010, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	-12	0	12	mV
$V_{ACMPHYST}$	ACMP hysteresis	Programmable		17		mV
R_{CSRES}	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		39		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		71		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		104		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		136		kOhm
$t_{ACMPSTART}$	Startup time				10	μs

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 40) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

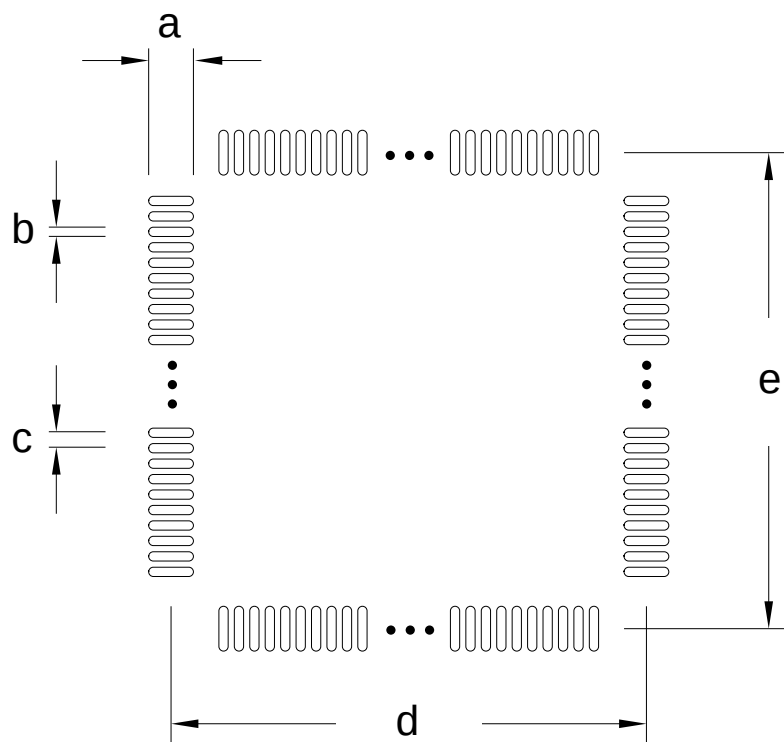
Total ACMP Active Current

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

QFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
32	PD4	ADC0_CH4 OPAMP_P2		LEU0_TX #0	
33	PD5	ADC0_CH5 OPAMP_OUT2 #0		LEU0_RX #0	
34	PD6	ADC0_CH6 DAC0_P1 / OPAMP_P1	TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2
35	PD7	ADC0_CH7 DAC0_N1 / OPAMP_N1	TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2
36	PD8				CMU_CLK1 #1
37	PC6	ACMP0_CH6		I2C0_SDA #2	LES_CH6 #0
38	PC7	ACMP0_CH7		I2C0_SCL #2	LES_CH7 #0
39	VDD_DREG	Power supply for on-chip voltage regulator.			
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.			
41	PE4	LCD_COM0		US0_CS #1	
42	PE5	LCD_COM1		US0_CLK #1	
43	PE6	LCD_COM2		US0_RX #1	
44	PE7	LCD_COM3		US0_TX #1	
45	PC12	ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT			CMU_CLK0 #1 LES_CH12 #0
46	PC13	ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT	TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0		LES_CH13 #0
47	PC14	ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT	TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3	LES_CH14 #0
48	PC15	ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT	TIM1_CC2 #0	US0_CLK #3	LES_CH15 #0 DBG_SWO #1
49	PF0		TIM0_CC0 #5 LETIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1
50	PF1		TIM0_CC1 #5 LETIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1 GPIO_EM4WU3
51	PF2	LCD_SEG0	TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
52	PF3	LCD_SEG1			PRS_CH0 #1
53	PF4	LCD_SEG2			PRS_CH1 #1
54	PF5	LCD_SEG3			PRS_CH2 #1
55	IOVDD_5	Digital IO power supply 5.			
56	VSS	Ground.			
57	PE8	LCD_SEG4			PRS_CH3 #1
58	PE9	LCD_SEG5			
59	PE10	LCD_SEG6	TIM1_CC0 #1	US0_TX #0	BOOT_TX
60	PE11	LCD_SEG7	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG1	PF3							LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4							LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5							LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG4	PE8							LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG5	PE9							LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG6	PE10							LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG7	PE11							LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG8	PE12							LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG9	PE13							LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG10	PE14							LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG11	PE15							LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG13	PA0							LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG14	PA1							LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG15	PA2							LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG16	PA3							LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG17	PA4							LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG18	PA5							LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG20/ LCD_COM4	PB3							LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4
LCD_SEG21/ LCD_COM5	PB4							LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5
LCD_SEG22/ LCD_COM6	PB5							LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6
LCD_SEG23/ LCD_COM7	PB6							LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7
LES_ALTEX0	PD6							LESENSE alternate exite output 0.
LES_ALTEX1	PD7							LESENSE alternate exite output 1.
LES_ALTEX2	PA3							LESENSE alternate exite output 2.
LES_ALTEX3	PA4							LESENSE alternate exite output 3.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LES_ALTEX4	PA5							LESENSE alternate exit output 4.
LES_ALTEX5	PE11							LESENSE alternate exit output 5.
LES_ALTEX6	PE12							LESENSE alternate exit output 6.
LES_ALTEX7	PE13							LESENSE alternate exit output 7.
LES_CH4	PC4							LESENSE channel 4.
LES_CH5	PC5							LESENSE channel 5.
LES_CH6	PC6							LESENSE channel 6.
LES_CH7	PC7							LESENSE channel 7.
LES_CH12	PC12							LESENSE channel 12.
LES_CH13	PC13							LESENSE channel 13.
LES_CH14	PC14							LESENSE channel 14.
LES_CH15	PC15							LESENSE channel 15.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7		PF1	PC5				Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15	PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14	PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13			PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14			PD7				Pulse Counter PCNT0 input number 1.
PRS_CH0	PA0	PF3						Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4						Peripheral Reflex System PRS, channel 1.
PRS_CH2		PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3		PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0		PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1		PD2		PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2		PD3		PF2		Timer 0 Capture Compare input / output channel 2.
TIM1_CC0	PC13	PE10		PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11		PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11	PC13			Timer 1 Capture Compare input / output channel 2.
US0_CLK	PE12	PE5		PC15	PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4		PC14	PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6		PE12	PB8			USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7		PE13	PB7			USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX		PD1	PD6					USART1 Asynchronous Receive.

Figure 5.2. TQFP64 PCB Solder Mask**Table 5.2. QFP64 PCB Solder Mask Dimensions (Dimensions in mm)**

Symbol	Dim. (mm)
a	1.72
b	0.42
c	0.50
d	11.50
e	11.50

7 Revision History

7.1 Revision 1.40

March 6th, 2015

Updated Block Diagram.

Updated Energy Modes current consumption.

Updated Power Management section.

Updated LFRCO and HFRCO sections.

Added AUXHFRCO to block diagram and Electrical Characteristics.

Corrected unit to kHz on LFRCO plots y-axis.

Updated ADC section and added clarification on conditions for INL_{ADC} and DNL_{ADC} parameters.

Updated DAC section and added clarification on conditions for INL_{DAC} and DNL_{DAC} parameters.

Updated OPAMP section.

Updated ACMP section and the response time graph.

Updated VCMP section.

Updated Digital Peripherals section.

7.2 Revision 1.30

July 2nd, 2014

Corrected single power supply voltage minimum value from 1.85V to 1.98V.

Updated current consumption.

Updated transition between energy modes.

Updated power management data.

Updated GPIO data.

Updated LFXO, HFXO, HFRCO and ULFRCO data.

Updated LFRCO and HFRCO plots.

Updated ACMP data.

7.3 Revision 1.21

November 21st, 2013

Updated figures.

Updated errata-link.

Updated chip marking.

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