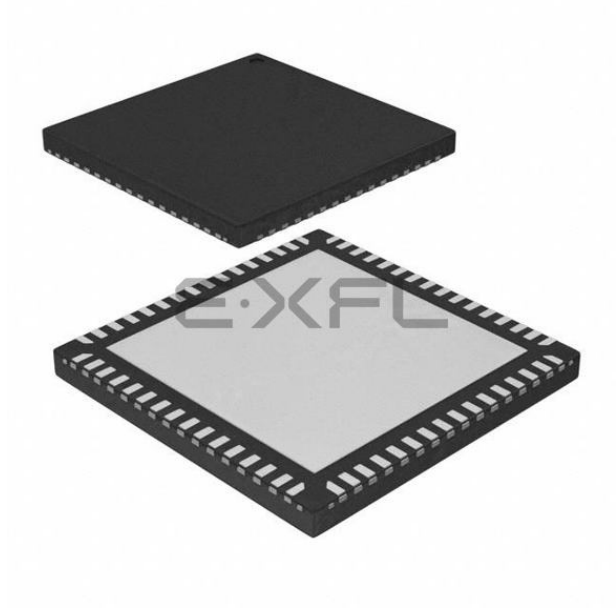
Silicon Labs - EFM32TG230F16-QFN64 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	56
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg230f16-qfn64

divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32TG.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32TG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32TG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 Inter-Integrated Circuit Interface (I2C)

The I^2C module provides an interface between the MCU and a serial I^2C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I^2C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

2.1.12 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Auto-baud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

2.1.13 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.14 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output.

2.1.15 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

2.1.16 Low Energy Timer (LETIMER)

The unique LETIMER™, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

2.1.17 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

2.1.18 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.2 Configuration Summary

The features of the EFM32TG230 is a subset of the feature set described in the EFM32TG Reference Manual. Table 2.1 (p. 7) describes device specific implementation of the features.

Table 2.1. Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration	TIM0_CC[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	56 pins	Available pins are shown in Table 4.3 (p. 51)

2.3 Memory Map

The *EFM32TG230* memory map is shown in Figure 2.2 (p. 8), with RAM and Flash sizes for the largest memory configuration.

3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on T_{AMB}=25°C and V_{DD}=3.0 V, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 9) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 9) .

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage temperature range		-40		150[1]	°C
T_S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	°C
V_{DDMAX}	External main supply voltage		0		3.8	V
V_{IOPIN}	Voltage on any I/O pin		-0.3		V_{DD}+0.3	V

[1]Based on programmed devices tested for 10000 hours at 150°C. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Ambient temperature range	-40		85	°C
V_{DDOP}	Operating supply voltage	1.98		3.8	V
f_{APB}	Internal APB clock frequency			32	MHz
f_{AHB}	Internal AHB clock frequency			32	MHz

3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 3.4. Energy Modes Transitions

Symbol	Parameter	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0		0		HF-CORE-CLK cycles
t_{EM20}	Transition time from EM2 to EM0		2		µs
t_{EM30}	Transition time from EM3 to EM0		2		µs
t_{EM40}	Transition time from EM4 to EM0		163		µs

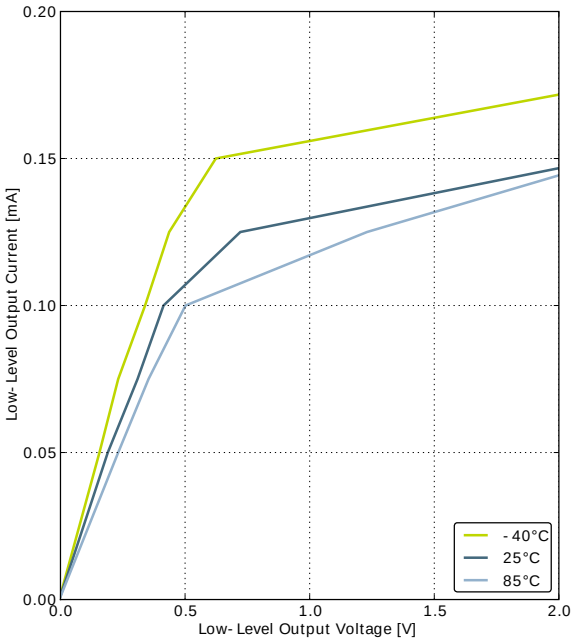
3.6 Power Management

The EFM32TG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

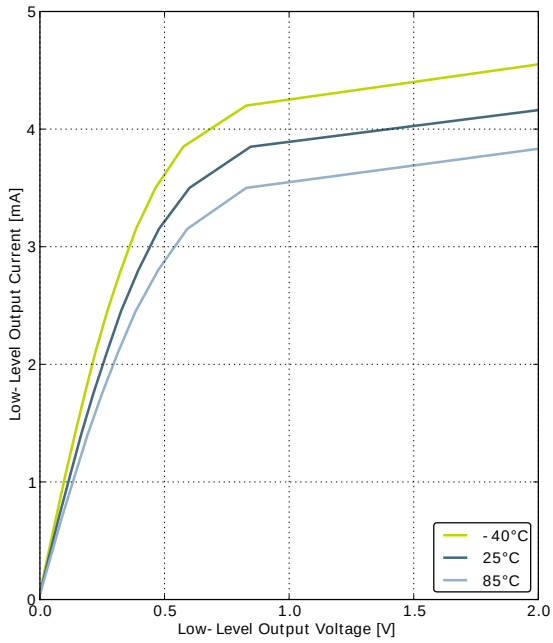
Table 3.5. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BODextthr-}$	BOD threshold on falling external supply voltage		1.74		1.96	V
$V_{BODextthr+}$	BOD threshold on rising external supply voltage			1.85	1.98	V
$V_{PORthr+}$	Power-on Reset (POR) threshold on rising external supply voltage				1.98	V
t_{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		µs
$C_{DECOUPLE}$	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		µF

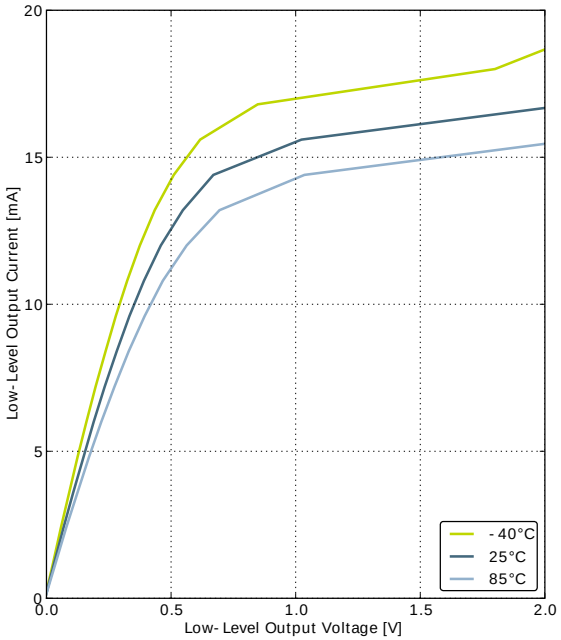
Figure 3.4. Typical Low-Level Output Current, 2V Supply Voltage



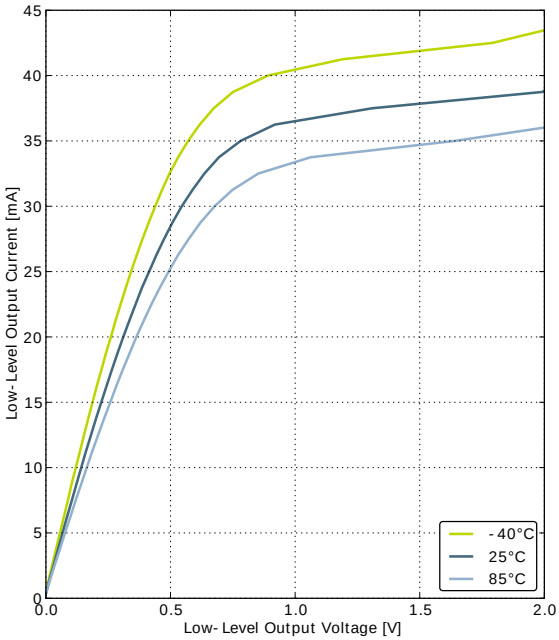
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

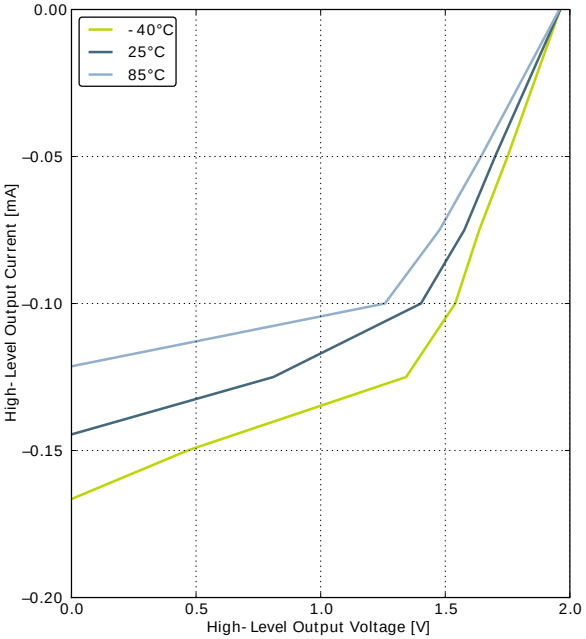


GPIO_Px_CTRL DRIVEMODE = STANDARD

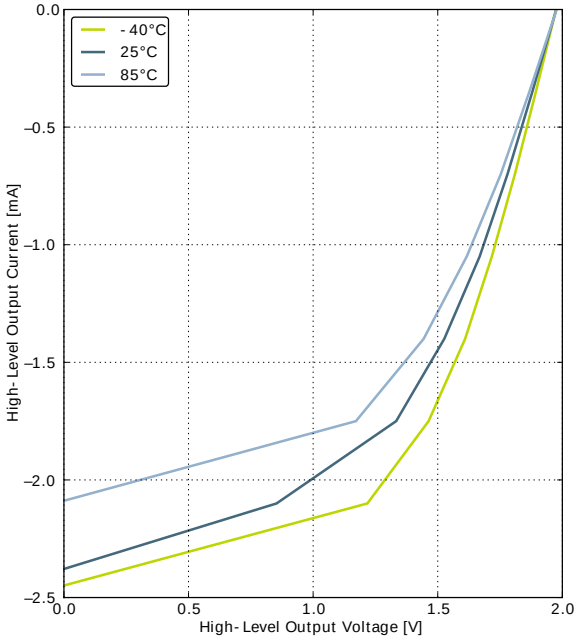


GPIO_Px_CTRL DRIVEMODE = HIGH

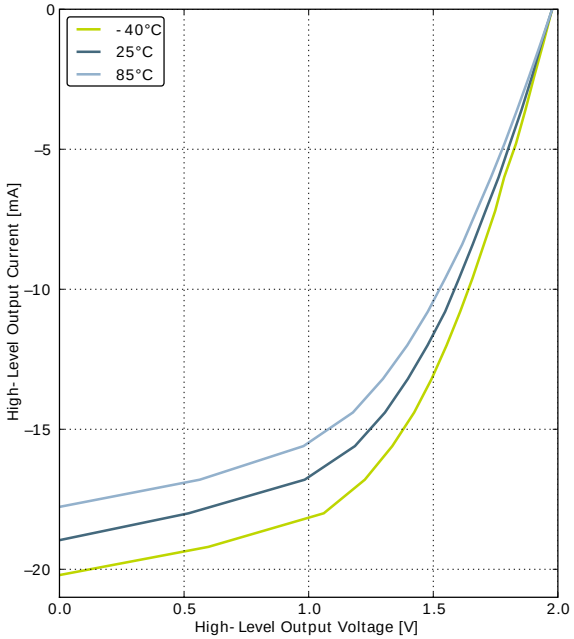
Figure 3.5. Typical High-Level Output Current, 2V Supply Voltage



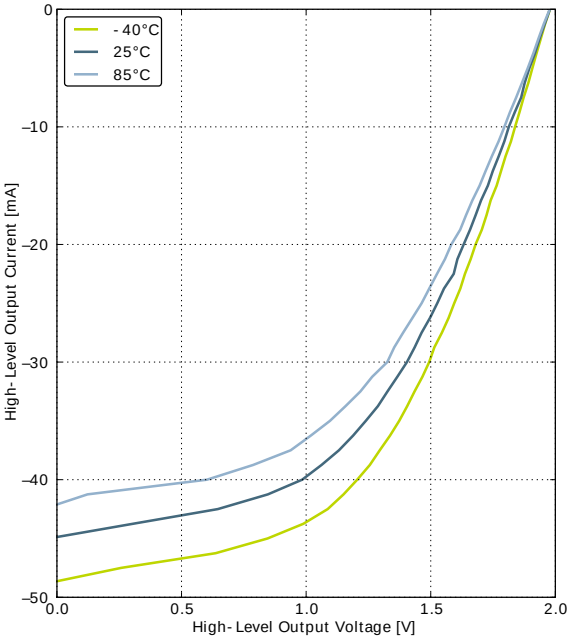
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		f_{HFRCO} = 14 MHz		104	120	µA
		f_{HFRCO} = 11 MHz		94	110	µA
		f_{HFRCO} = 6.6 MHz		63	90	µA
		f_{HFRCO} = 1.2 MHz		22	32	µA
$TUNESTEP_{H-FRCO}$	Frequency step for LSB change in TUNING value			0.3[3]		%

[1]For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

[2]For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

[3]The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

Figure 3.11. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature

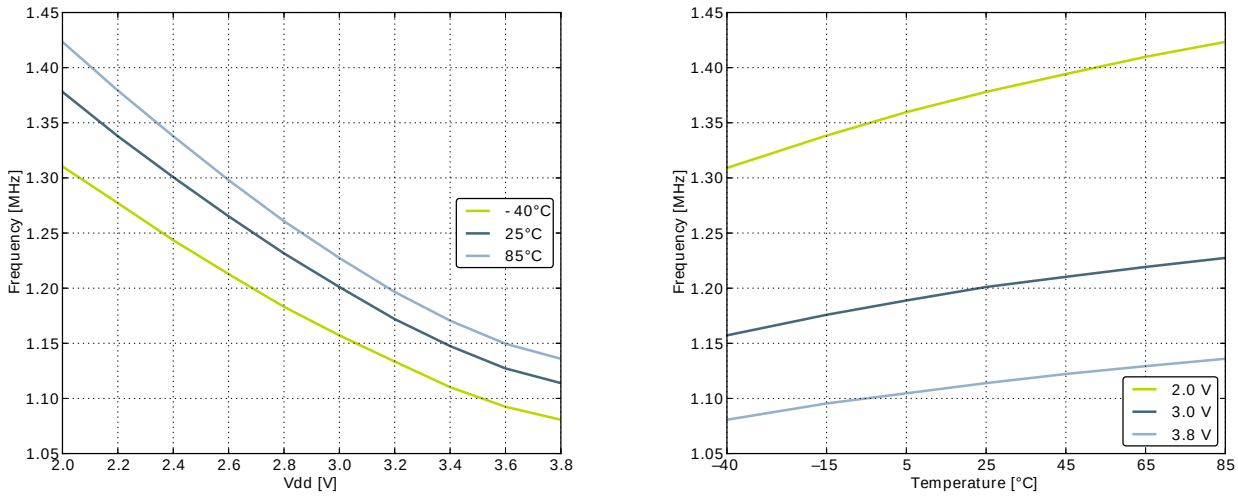
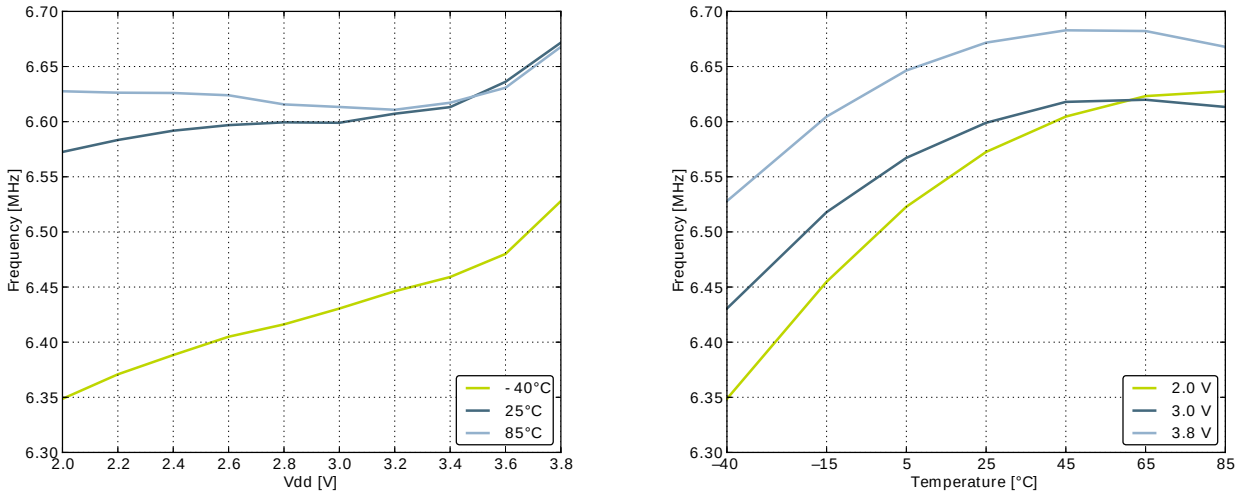


Figure 3.12. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature



3.10 Analog Digital Converter (ADC)

Table 3.14. ADC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ADCIN}	Input voltage range	Single ended	0		V_{REF}	V
		Differential	$-V_{REF}/2$		$V_{REF}/2$	V
$V_{ADCREFIN}$	Input range of external reference voltage, single ended and differential		1.25		V_{DD}	V
$V_{ADCREFIN\_CH7}$	Input range of external negative reference voltage on channel 7	See $V_{ADCREFIN}$	0		V_{DD} - 1.1	V
$V_{ADCREFIN\_CH6}$	Input range of external positive reference voltage on channel 6	See $V_{ADCREFIN}$	0.625		V_{DD}	V
$V_{ADCCMIN}$	Common mode input range		0		V_{DD}	V
I_{ADCIN}	Input current	2pF sampling capacitors		<100		nA
$CMRR_{ADC}$	Analog input common mode rejection ratio			65		dB
I_{ADC}	Average active current	1 MSamples/s, 12 bit, external reference		377		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00		67		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01		68		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10		71		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b11		244		µA
I_{ADCREF}	Current consumption of internal voltage reference	Internal voltage reference		65		µA
C_{ADCIN}	Input capacitance			2		pF
R_{ADCIN}	Input ON resistance		1			MOhm
$R_{ADCFILT}$	Input RC filter resistance			10		kOhm
$C_{ADCFILT}$	Input RC filter/decoupling capacitance			250		fF

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference		69		dB
		200 kSamples/s, 12 bit, differential, 2xV_{DD} reference		70		dB
$SINAD_{ADC}$	SIgnal-to-Noise And Distortion-ratio (SINAD)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		64		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differential, 2xV_{DD} reference		68		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference		66		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V_{DD} reference	62	68		dB
		200 kSamples/s, 12 bit, differential, 2xV_{DD} reference		69		dB
$SFDR_{ADC}$	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differential, 2xV_{DD} reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, V_{DD} reference	68	76		dBc
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		79		dBc
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		79		dBc
		200 kSamples/s, 12 bit, differential, 5V reference		78		dBc
		200 kSamples/s, 12 bit, differential, V_{DD} reference		79		dBc
		200 kSamples/s, 12 bit, differential, 2xV_{DD} reference		79		dBc
$V_{ADCOFFSET}$	Offset voltage	After calibration, single ended	-4	0.3	4	mV
		After calibration, differential		0.3		mV
$TGRAD_{ADCTH}$	Thermometer output gradient			-1.92		mV/°C
				-6.3		ADC Codes/°C
DNL_{ADC}	Differential non-linearity (DNL)	V_{DD}= 3.0 V, external 2.5V reference	-1	±0.7	4	LSB
INL_{ADC}	Integral non-linearity (INL), End point method	V_{DD}= 3.0 V, external 2.5V reference		±1.2	±3	LSB
MC_{ADC}	No missing codes		11.999[1]	12		bits
$GAIN_{ED}$	Gain error drift	1.25V reference		0.01[2]	0.033[3]	%/°C
		2.5V reference		0.01[2]	0.03[3]	%/°C
$OFFSET_{ED}$	Offset error drift	1.25V reference		0.2[2]	0.7[3]	LSB/°C
		2.5V reference		0.2[2]	0.62[3]	LSB/°C

[1]On the average every ADC will have one missing code, most likely to appear around 2048 ± n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic

at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

[2]Typical numbers given by abs(Mean) / (85 - 25).

[3]Max number given by (abs(Mean) + 3x stddev) / (85 - 25).

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.17 (p. 30) and Figure 3.18 (p. 30) , respectively.

Figure 3.17. Integral Non-Linearity (INL)

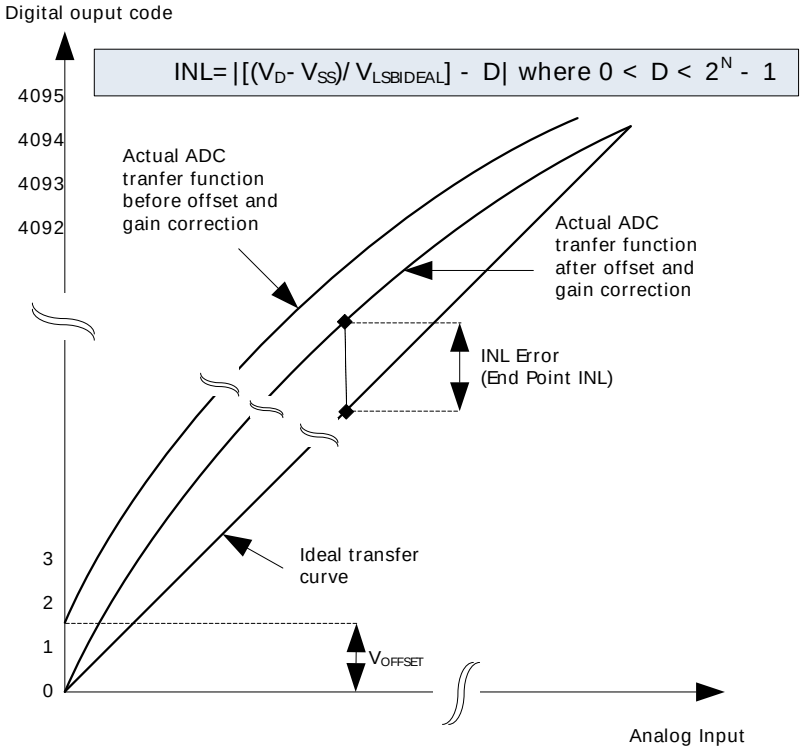


Figure 3.18. Differential Non-Linearity (DNL)

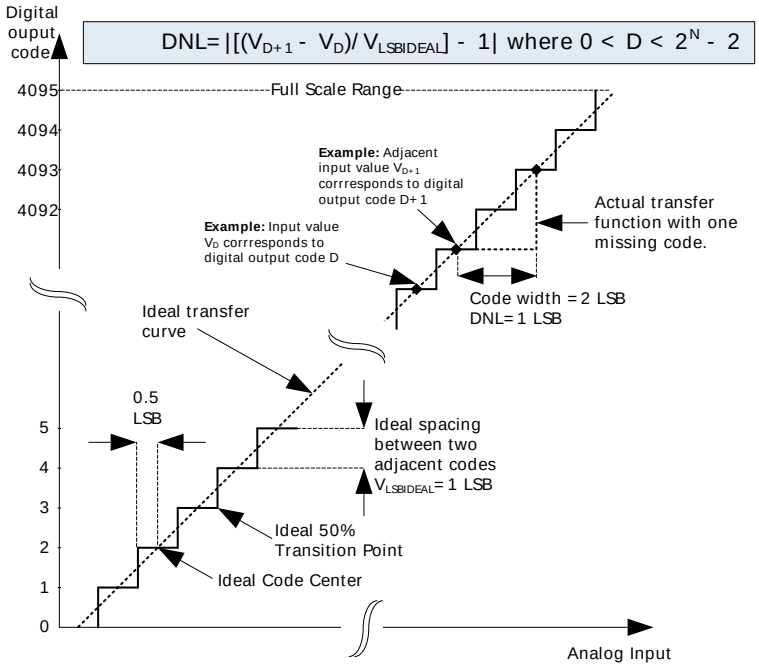


Figure 3.26. OPAMP Negative Power Supply Rejection Ratio

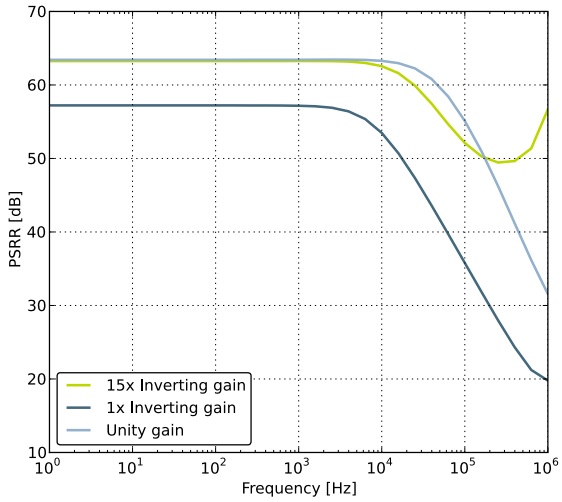


Figure 3.27. OPAMP Voltage Noise Spectral Density (Unity Gain) V_{out}=1V

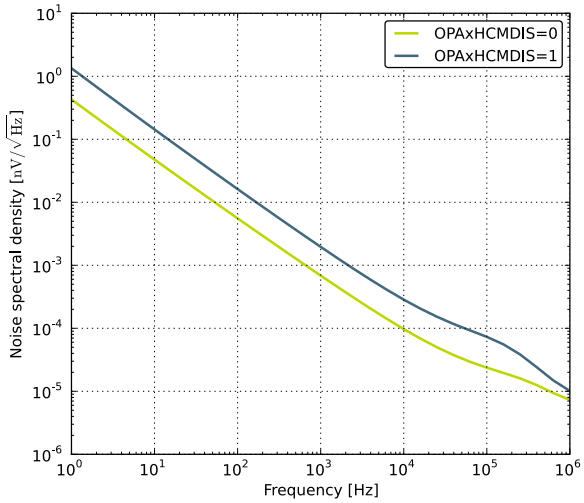
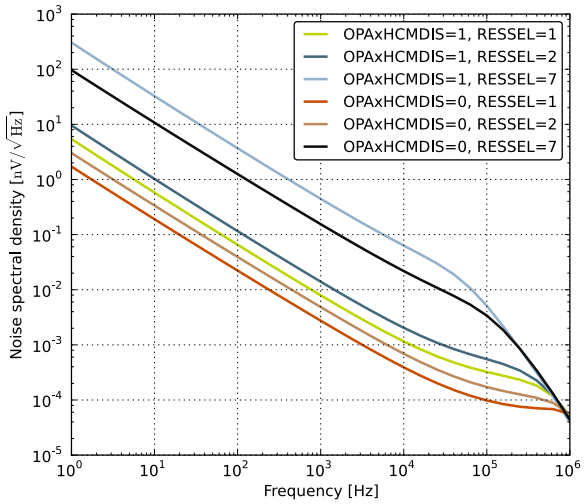


Figure 3.28. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)



Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7		PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6		PC0	PF0	PE12	I2C0 Serial Data input / output.
LES_ALTEX0	PD6							LESENSE alternate exite output 0.
LES_ALTEX1	PD7							LESENSE alternate exite output 1.
LES_ALTEX2	PA3							LESENSE alternate exite output 2.
LES_ALTEX3	PA4							LESENSE alternate exite output 3.
LES_ALTEX4	PA5							LESENSE alternate exite output 4.
LES_ALTEX5	PE11							LESENSE alternate exite output 5.
LES_ALTEX6	PE12							LESENSE alternate exite output 6.
LES_ALTEX7	PE13							LESENSE alternate exite output 7.
LES_CH0	PC0							LESENSE channel 0.
LES_CH1	PC1							LESENSE channel 1.
LES_CH2	PC2							LESENSE channel 2.
LES_CH3	PC3							LESENSE channel 3.
LES_CH4	PC4							LESENSE channel 4.
LES_CH5	PC5							LESENSE channel 5.
LES_CH6	PC6							LESENSE channel 6.
LES_CH7	PC7							LESENSE channel 7.
LES_CH8	PC8							LESENSE channel 8.
LES_CH9	PC9							LESENSE channel 9.
LES_CH10	PC10							LESENSE channel 10.
LES_CH11	PC11							LESENSE channel 11.
LES_CH12	PC12							LESENSE channel 12.
LES_CH13	PC13							LESENSE channel 13.
LES_CH14	PC14							LESENSE channel 14.
LES_CH15	PC15							LESENSE channel 15.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5				Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15	PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14	PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13		PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1	PD7				Pulse Counter PCNT0 input number 1.
PRS_CH0	PA0	PF3						Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4						Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1	PE8						Peripheral Reflex System PRS, channel 3.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
TIM0_CC0	PA0	PA0		PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1		PD2	PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2		PD3	PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM1_CC0	PC13	PE10		PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11		PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11	PC13			Timer 1 Capture Compare input / output channel 2.
US0_CLK	PE12		PC9	PC15	PB13	PB13		USART0 clock input / output.
US0_CS	PE13		PC8	PC14	PB14	PB14		USART0 chip select input / output.
US0_RX	PE11		PC10	PE12	PB8	PC1		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10		PC11	PE13	PB7	PC0		USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX	PC1	PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0	PD7					USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32TG230* is shown in Table 4.3 (p. 51). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

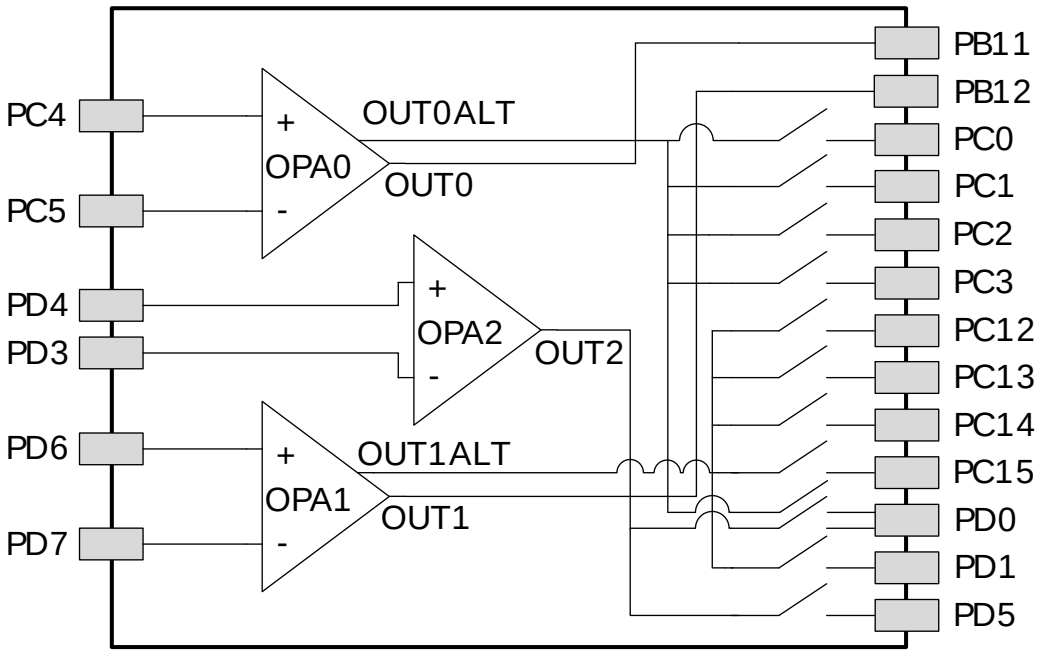
Table 4.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	-	-	-	-	PA10	PA9	PA8	-	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	-	PB14	PB13	PB12	PB11	-	-	PB8	PB7	-	-	-	-	-	-	-
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	-	-	-	-	-	-	-	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	PF5	PF4	PF3	PF2	PF1	PF0

4.4 Opamp Pinout Overview

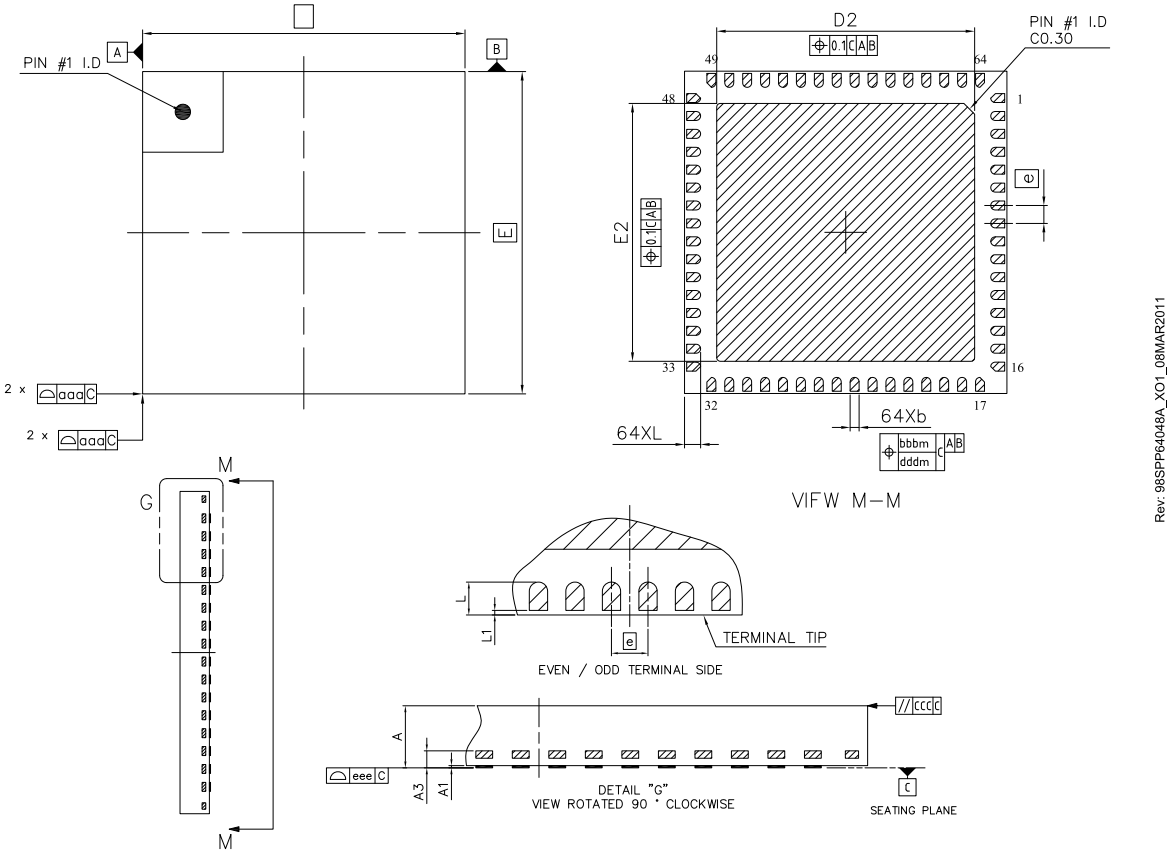
The specific opamp terminals available in *EFM32TG230* is shown in Figure 4.2 (p. 52) .

Figure 4.2. Opamp Pinout



4.5 QFN64 Package

Figure 4.3. QFN64



Note:

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.

3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional

Table 4.4. QFN64 (Dimensions in mm)

Symbol	A	A1	A3	b	D	E	D2	E2	e	L	L1	aaa	bbb	ccc	ddd	eee
Min	0.80	0.00		0.20			7.10	7.10		0.40	0.00					
Nom	0.85	-	0.203 REF	0.25	9.00 BSC	9.00 BSC	7.20	7.20	0.50 BSC	0.45		0.10	0.10	0.10	0.05	0.08
Max	0.90	0.05		0.30			7.30	7.30		0.50	0.10					

The QFN64 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see:
http://www.silabs.com/support/quality/pages/default.aspx

5 PCB Layout and Soldering

5.1 Recommended PCB Layout

Figure 5.1. QFN64 PCB Land Pattern

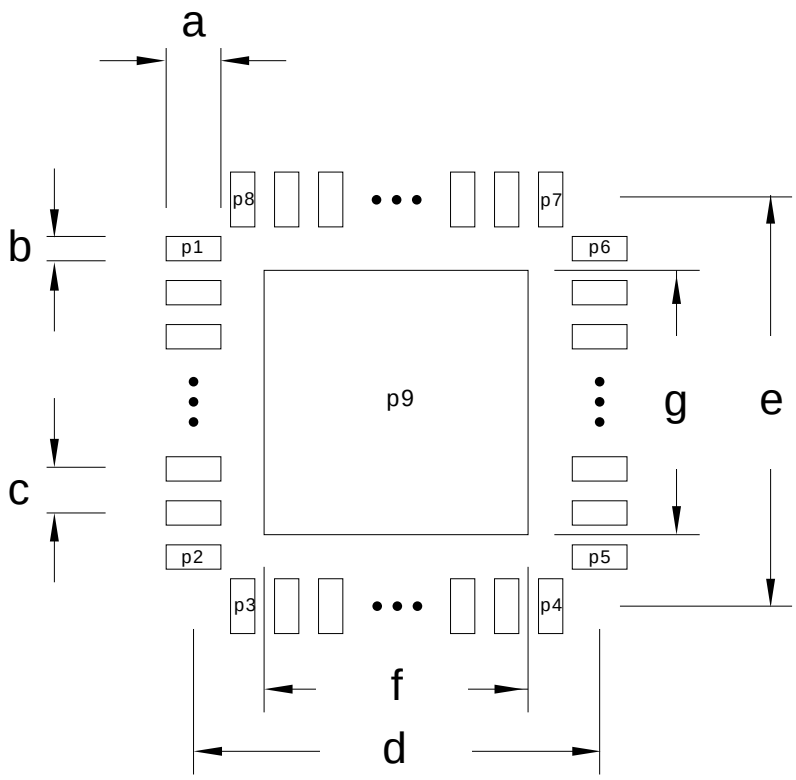


Table 5.1. QFN64 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin number	Symbol	Pin number
a	0.85	P1	1	P8	64
b	0.30	P2	16	P9	65
c	0.50	P3	17	-	-
d	8.90	P4	32	-	-
e	8.90	P5	33	-	-
f	7.20	P6	48	-	-
g	7.20	P7	49	-	-

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