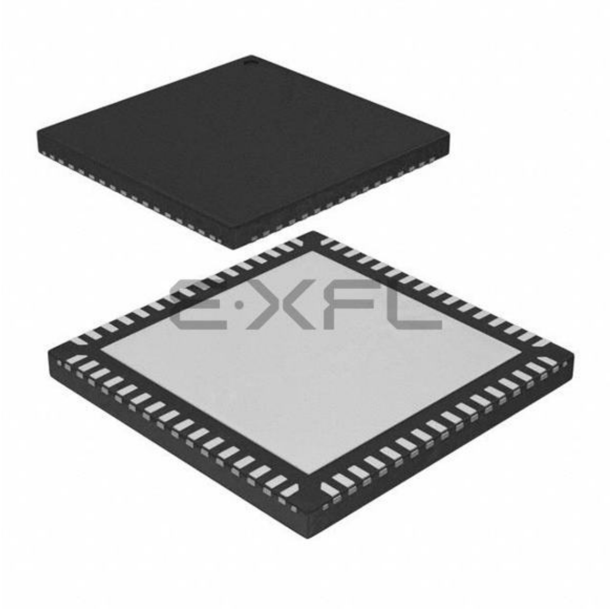
# Silicon Labs - EFM32TG230F8-QFN64 Datasheet



## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 56 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.85V ~ 3.8V |
| Data Converters | A/D 8x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-QFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32tg230f8-qfn64 |

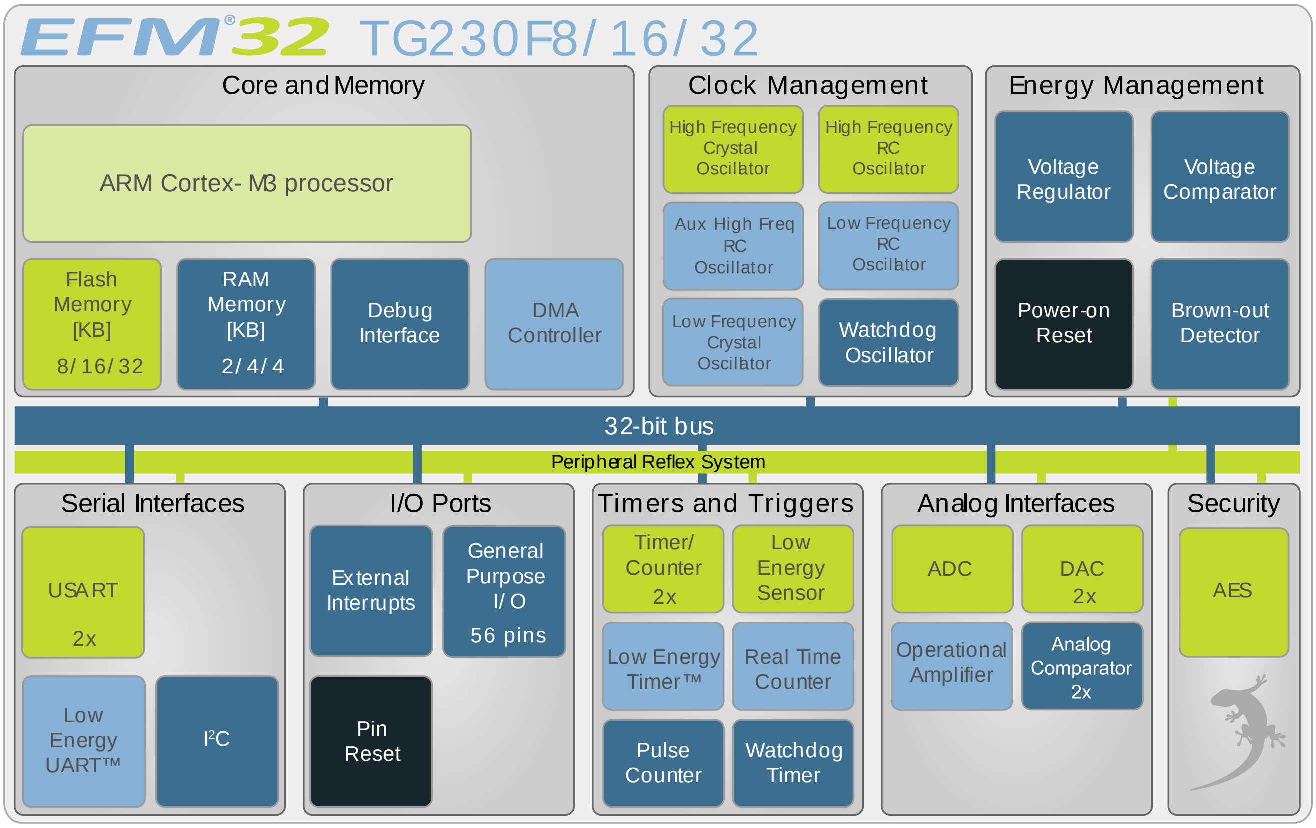
# 2 System Summary

## 2.1 System Introduction

The EFM32 MCUs are the world’s most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32TG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32TG230 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32TG Reference Manual*.

A block diagram of the EFM32TG230 is shown in Figure 2.1 (p. 3) .

***Figure 2.1. Block Diagram***



### 2.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EFM32 implementation of the Cortex-M3 is described in detail in *EFM32 Cortex-M3 Reference Manual*.

### 2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface . In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

### 2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32TG microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is

### 2.1.19 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 2.1.20 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

### 2.1.21 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

### 2.1.22 Operational Amplifier (OPAMP)

The EFM32TG230 features 3 Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors etc.

### 2.1.23 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface (LESENSE$^{TM}$), is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable FSM which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

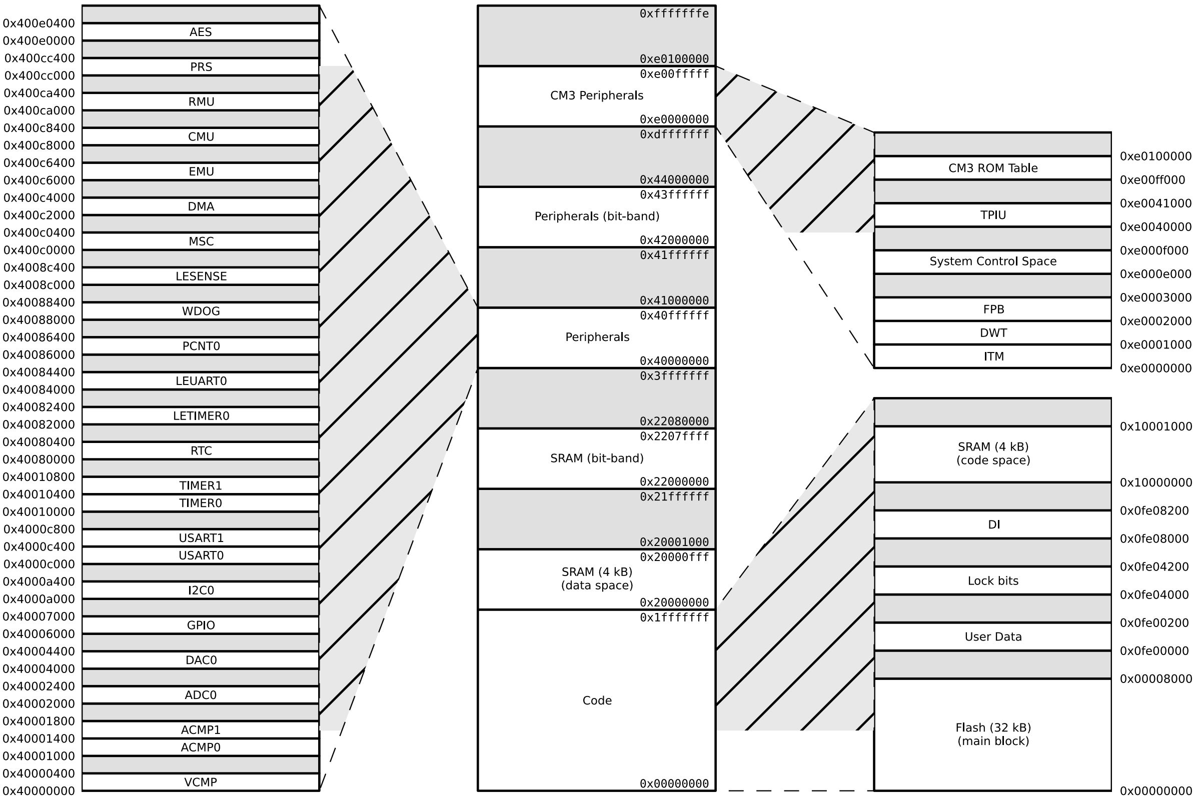
### 2.1.24 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

### 2.1.25 General Purpose Input/Output (GPIO)

In the EFM32TG230, there are 56 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

***Figure 2.2. EFM32TG230 Memory Map with largest RAM and Flash sizes***



# 3 Electrical Characteristics

## 3.1 Test Conditions

### 3.1.1 Typical Values

The typical data are based on $T_{AMB}$=25°C and $V_{DD}$=3.0 V, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

### 3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

## 3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 9) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 9) .

***Table 3.1. Absolute Maximum Ratings***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature range | | -40 | | 150[1] | °C |
| $T_S$ | Maximum soldering temperature | Latest IPC/JEDEC J-STD-020 Standard | | | 260 | °C |
| $V_{DDMAX}$ | External main supply voltage | | 0 | | 3.8 | V |
| $V_{IOPIN}$ | Voltage on any I/O pin | | -0.3 | | $V_{DD}$+0.3 | V |

[1] Based on programmed devices tested for 10000 hours at 150°C. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

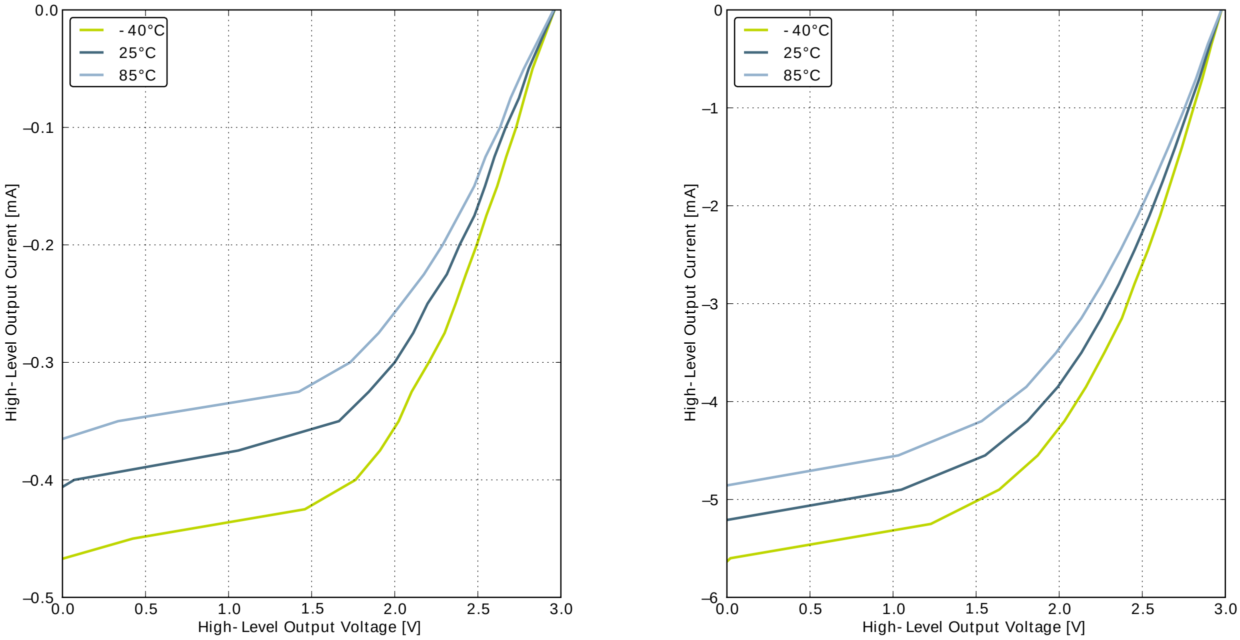
## 3.3 General Operating Conditions

### 3.3.1 General Operating Conditions

***Table 3.2. General Operating Conditions***

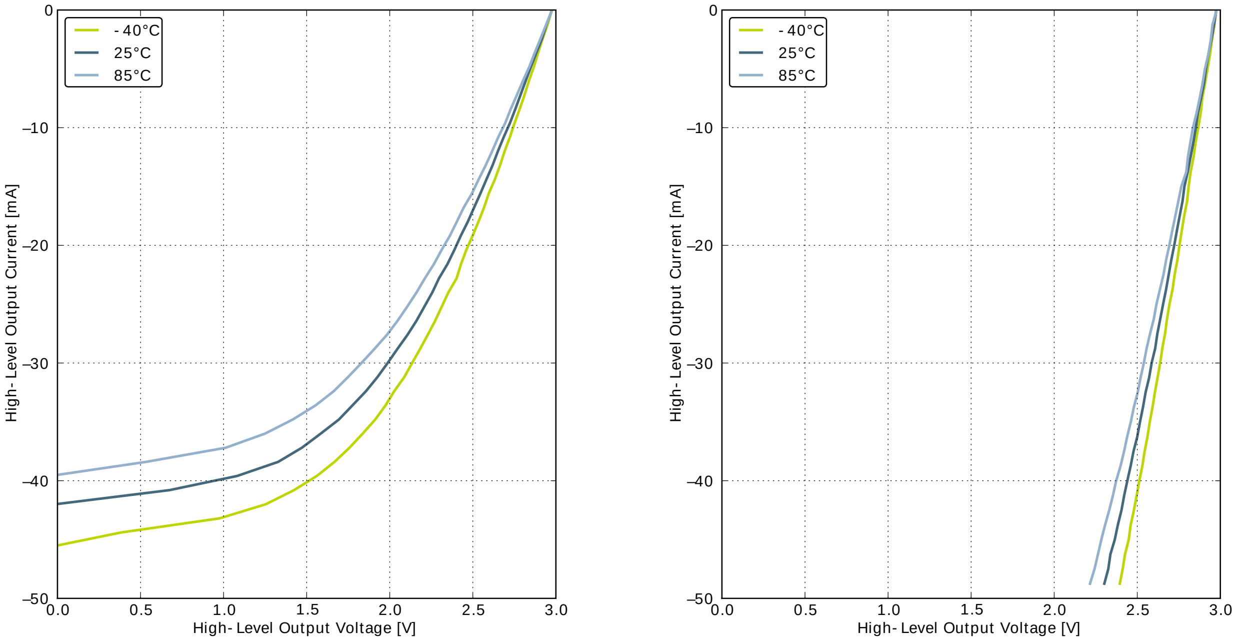
| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{AMB}$ | Ambient temperature range | -40 | | 85 | °C |
| $V_{DDOP}$ | Operating supply voltage | 1.98 | | 3.8 | V |
| $f_{APB}$ | Internal APB clock frequency | | | 32 | MHz |
| $f_{AHB}$ | Internal AHB clock frequency | | | 32 | MHz |

## *Figure 3.7. Typical High-Level Output Current, 3V Supply Voltage*



GPIO_Px_CTRL DRIVEMODE = LOWEST

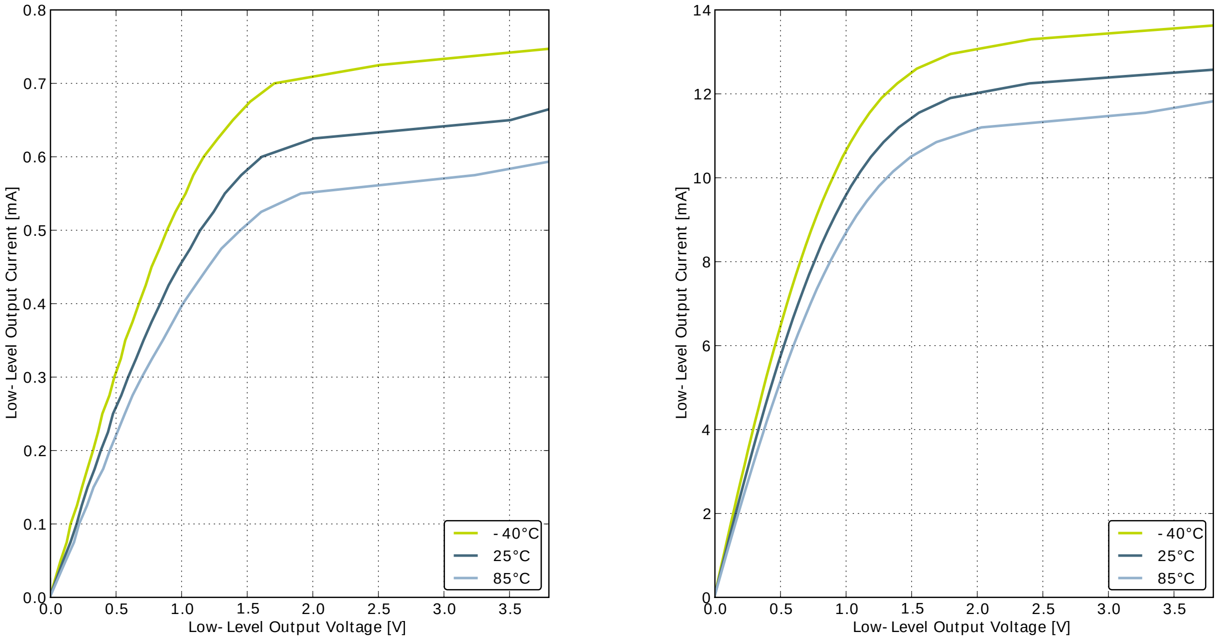
GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

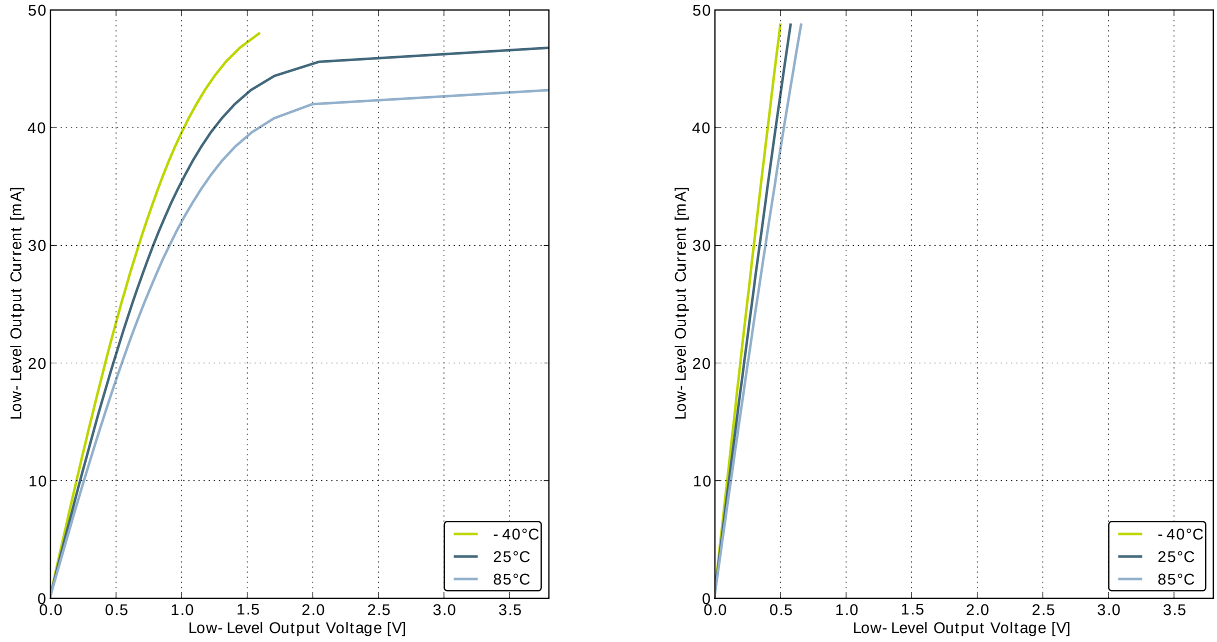
GPIO_Px_CTRL DRIVEMODE = HIGH

**Figure 3.8. Typical Low-Level Output Current, 3.8V Supply Voltage**



GPIO_Px_CTRL DRIVEMODE = LOWEST

GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

GPIO_Px_CTRL DRIVEMODE = HIGH

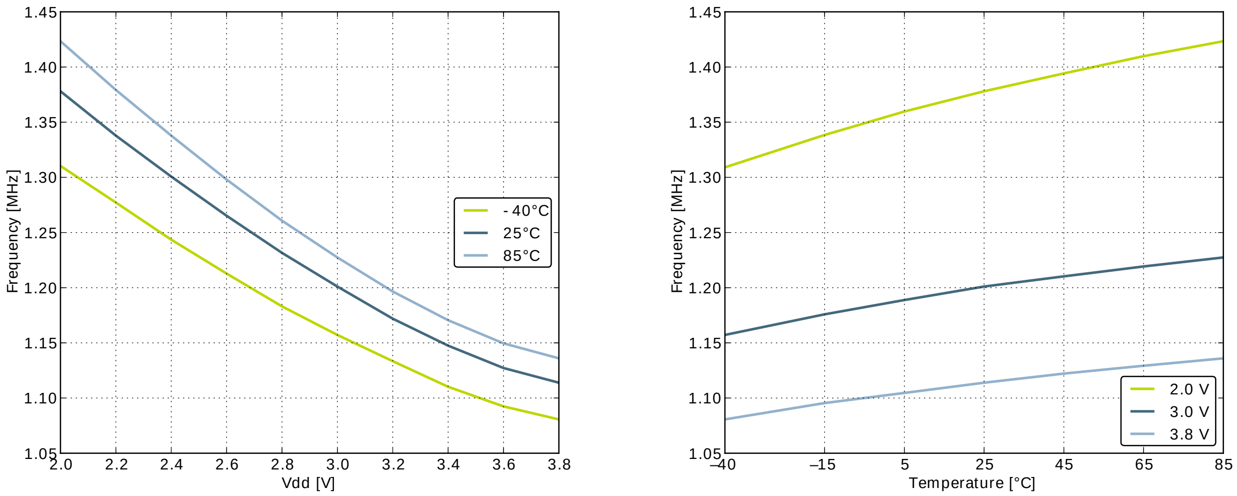
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | $f_{HFRCO}$ = 14 MHz | | 104 | 120 | µA |
| | | $f_{HFRCO}$ = 11 MHz | | 94 | 110 | µA |
| | | $f_{HFRCO}$ = 6.6 MHz | | 63 | 90 | µA |
| | | $f_{HFRCO}$ = 1.2 MHz | | 22 | 32 | µA |
| TUNESTEP$_{HFRCO}$ | Frequency step for LSB change in TUNING value | | | 0.3[3] | | % |

[1] For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

[2] For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

[3] The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

### Figure 3.11. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature



### Figure 3.12. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature

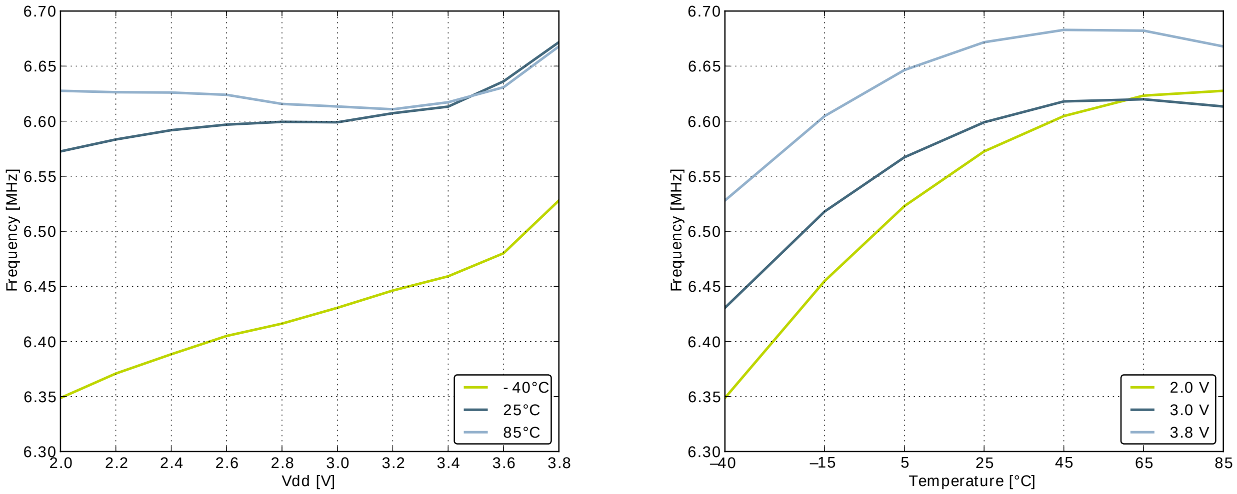
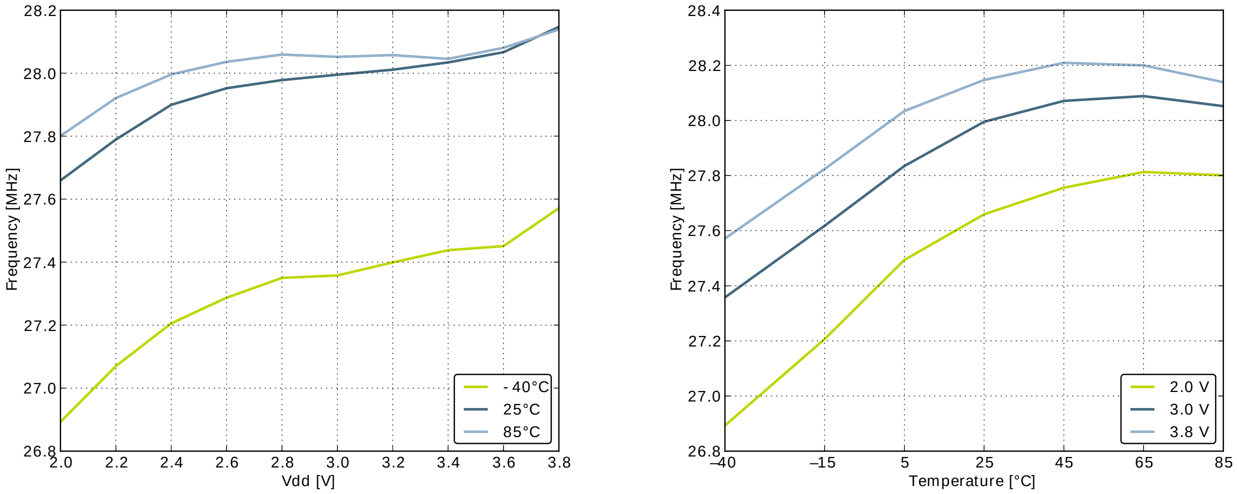


*Figure 3.16. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature*



## 3.9.5 AUXHFRCO

*Table 3.12. AUXHFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{AUXHFRCO}$ | Oscillation frequency, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | 28 MHz frequency band | 27.16 | 28.0 | 28.84 | MHz |
| | | 21 MHz frequency band | 20.37 | 21.0 | 21.63 | MHz |
| | | 14 MHz frequency band | 13.58 | 14.0 | 14.42 | MHz |
| | | 11 MHz frequency band | 10.67 | 11.0 | 11.33 | MHz |
| | | 7 MHz frequency band | 6.40[1] | 6.60[1] | 6.80[1] | MHz |
| | | 1 MHz frequency band | 1.16[2] | 1.20[2] | 1.24[2] | MHz |
| $t_{AUXHFRCO\_settling}$ | Settling time after start-up | $f_{AUXHFRCO}$ = 14 MHz | | 0.6 | | Cycles |
| $TUNESTEP_{AUXHFRCO}$ | Frequency step for LSB change in TUNING value | | | 0.3[3] | | % |

[1] For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

[2] For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

[3] The TUNING field in the CMU_AUXHFRCOCTRL register may be used to adjust the AUXHFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

## 3.9.6 ULFRCO

*Table 3.13. ULFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{ULFRCO}$ | Oscillation frequency | 25°C, 3V | 0.70 | | 1.75 | kHz |
| $TC_{ULFRCO}$ | Temperature coefficient | | | 0.05 | | %/°C |
| $VC_{ULFRCO}$ | Supply voltage coefficient | | | -18.2 | | %/V |

## 3.10 Analog Digital Converter (ADC)

*Table 3.14. ADC*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ADCIN}$ | Input voltage range | Single ended | 0 | | $V_{REF}$ | V |
| | | Differential | $-V_{REF}/2$ | | $V_{REF}/2$ | V |
| $V_{ADCREFIN}$ | Input range of external reference voltage, single ended and differential | | 1.25 | | $V_{DD}$ | V |
| $V_{ADCREFIN\_CH7}$ | Input range of external negative reference voltage on channel 7 | See $V_{ADCREFIN}$ | 0 | | $V_{DD}$ - 1.1 | V |
| $V_{ADCREFIN\_CH6}$ | Input range of external positive reference voltage on channel 6 | See $V_{ADCREFIN}$ | 0.625 | | $V_{DD}$ | V |
| $V_{ADCCMIN}$ | Common mode input range | | 0 | | $V_{DD}$ | V |
| $I_{ADCIN}$ | Input current | 2pF sampling capacitors | | <100 | | nA |
| $CMRR_{ADC}$ | Analog input common mode rejection ratio | | | 65 | | dB |
| $I_{ADC}$ | Average active current | 1 MSamples/s, 12 bit, external reference | | 377 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b00 | | 67 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b01 | | 68 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b10 | | 71 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b11 | | 244 | | µA |
| $I_{ADCREF}$ | Current consumption of internal voltage reference | Internal voltage reference | | 65 | | µA |
| $C_{ADCIN}$ | Input capacitance | | | 2 | | pF |
| $R_{ADCIN}$ | Input ON resistance | | 1 | | | MOhm |
| $R_{ADCFILT}$ | Input RC filter resistance | | | 10 | | kOhm |
| $C_{ADCFILT}$ | Input RC filter/decoupling capacitance | | | 250 | | fF |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | | 63 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference | | 69 | | dB |
| | | 200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference | | 70 | | dB |
| $SINAD_{ADC}$ | SIgnal-to-Noise And Distortion-ratio (SINAD) | 1 MSamples/s, 12 bit, single ended, internal 1.25V reference | | 58 | | dB |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5V reference | | 62 | | dB |
| | | 1 MSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 64 | | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25V reference | | 60 | | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5V reference | | 64 | | dB |
| | | 1 MSamples/s, 12 bit, differential, 5V reference | | 54 | | dB |
| | | 1 MSamples/s, 12 bit, differential, $V_{DD}$ reference | | 66 | | dB |
| | | 1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference | | 68 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 61 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 65 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | | 63 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference | 62 | 68 | | dB |
| | | 200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference | | 69 | | dB |
| $SFDR_{ADC}$ | Spurious-Free Dynamic Range (SFDR) | 1 MSamples/s, 12 bit, single ended, internal 1.25V reference | | 64 | | dBc |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5V reference | | 76 | | dBc |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $SR_{DAC}$ | Sample rate | | | | 500 | ksamples/s |
| $f_{DAC}$ | DAC clock frequency | Continuous Mode | | | 1000 | kHz |
| | | Sample/Hold Mode | | | 250 | kHz |
| | | Sample/Off Mode | | | 250 | kHz |
| $CYC_{DACCONV}$ | Clock cyckles per conversion | | | 2 | | |
| $t_{DACCONV}$ | Conversion time | | 2 | | | µs |
| $t_{DACSETTLE}$ | Settling time | | | 5 | | µs |
| $SNR_{DAC}$ | Signal to Noise Ratio (SNR) | 500 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 58 | | dB |
| | | 500 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 59 | | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25V reference | | 58 | | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 2.5V reference | | 58 | | dB |
| | | 500 kSamples/s, 12 bit, differential, $V_{DD}$ reference | | 59 | | dB |
| $SNDR_{DAC}$ | Signal to Noise-pulse Distortion Ratio (SNDR) | 500 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 57 | | dB |
| | | 500 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 54 | | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25V reference | | 56 | | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 2.5V reference | | 53 | | dB |
| | | 500 kSamples/s, 12 bit, differential, $V_{DD}$ reference | | 55 | | dB |
| $SFDR_{DAC}$ | Spurious-Free Dynamic Range(SFDR) | 500 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 62 | | dBc |
| | | 500 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 56 | | dBc |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25V reference | | 61 | | dBc |
| | | 500 kSamples/s, 12 bit, differential, internal 2.5V reference | | 55 | | dBc |
| | | 500 kSamples/s, 12 bit, differential, $V_{DD}$ reference | | 60 | | dBc |
| $V_{DACOFFSET}$ | Offset voltage | After calibration, single ended | | 2 | | mV |
| | | After calibration, differential | | 2 | | mV |
| $DNL_{DAC}$ | Differential non-linearity | $V_{DD}$= 3.0 V, $V_{DD}$ reference | | ±1 | | LSB |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | OPAxHCMDIS=1 | $V_{SS}$ | | $V_{DD}$-1.2 | V |
| $V_{OUTPUT}$ | Output Voltage | | $V_{SS}$ | | $V_{DD}$ | V |
| $V_{OFFSET}$ | Input Offset Voltage | Unity Gain, $V_{SS}<V_{in}<V_{DD}$, OPAxHCMDIS=0 | | 6 | | mV |
| | | Unity Gain, $V_{SS}<V_{in}<V_{DD}$-1.2, OPAxHCMDIS=1 | | 1 | | mV |
| $V_{OFFSET\_DRIFT}$ | Input Offset Voltage Drift | | | | 0.02 | mV/°C |
| $SR_{OPAMP}$ | Slew Rate | OPA0/OPA1 BIASPROG=0xF, HALFBIAS=0x0 | | 46.11 | | V/µs |
| | | OPA0/OPA1 BIASPROG=0x7, HALFBIAS=0x1 | | 1.21 | | V/µs |
| | | OPA0/OPA1 BIASPROG=0x0, HALFBIAS=0x1 | | 0.16 | | V/µs |
| | | OPA2 BIASPROG=0xF, HALFBIAS=0x0 | | 4.43 | | V/µs |
| | | OPA2 BIASPROG=0x7, HALFBIAS=0x1 | | 1.30 | | V/µs |
| | | OPA2 BIASPROG=0x0, HALFBIAS=0x1 | | 0.16 | | V/µs |
| $PU_{OPAMP}$ | Power-up Time | OPA0/OPA1 BIASPROG=0xF, HALFBIAS=0x0 | | 0.09 | | µs |
| | | OPA0/OPA1 BIASPROG=0x7, HALFBIAS=0x1 | | 1.52 | | µs |
| | | OPA0/OPA1 BIASPROG=0x0, HALFBIAS=0x1 | | 12.74 | | µs |
| | | OPA2 BIASPROG=0xF, HALFBIAS=0x0 | | 0.09 | | µs |
| | | OPA2 BIASPROG=0x7, HALFBIAS=0x1 | | 0.13 | | µs |
| | | OPA2 BIASPROG=0x0, HALFBIAS=0x1 | | 0.17 | | µs |
| $N_{OPAMP}$ | Voltage Noise | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAxHCMDIS=0 | | 101 | | $\mu V_{RMS}$ |
| | | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAxHCMDIS=1 | | 141 | | $\mu V_{RMS}$ |
| | | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAxHCMDIS=0 | | 196 | | $\mu V_{RMS}$ |
| | | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<1 MHz, OPAxHCMDIS=1 | | 229 | | $\mu V_{RMS}$ |
| | | RESSEL=7, 0.1 Hz<f<10 kHz, OPAxHCMDIS=0 | | 1230 | | $\mu V_{RMS}$ |
| | | RESSEL=7, 0.1 Hz<f<10 kHz, OPAxHCMDIS=1 | | 2130 | | $\mu V_{RMS}$ |
| | | RESSEL=7, 0.1 Hz<f<1 MHz, OPAxHCMDIS=0 | | 1630 | | $\mu V_{RMS}$ |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 |
| 4 | PA3 | | | | LES_ALTEX2 #0 |
| 5 | PA4 | | | | LES_ALTEX3 #0 |
| 6 | PA5 | | | | LES_ALTEX4 #0 |
| 7 | PA6 | | | | GPIO_EM4WU1 |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | |
| 9 | PC0 | ACMP0_CH0<br>DAC0_OUT0ALT #0/<br>OPAMP_OUT0ALT | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5<br>US1_TX #0<br>I2C0_SDA #4 | LES_CH0 #0<br>PRS_CH2 #0 |
| 10 | PC1 | ACMP0_CH1<br>DAC0_OUT0ALT #1/<br>OPAMP_OUT0ALT | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5<br>US1_RX #0<br>I2C0_SCL #4 | LES_CH1 #0<br>PRS_CH3 #0 |
| 11 | PC2 | ACMP0_CH2<br>DAC0_OUT0ALT #2/<br>OPAMP_OUT0ALT | | | LES_CH2 #0 |
| 12 | PC3 | ACMP0_CH3<br>DAC0_OUT0ALT #3/<br>OPAMP_OUT0ALT | | | LES_CH3 #0 |
| 13 | PC4 | ACMP0_CH4<br>DAC0_P0 /<br>OPAMP_P0 | LETIM0_OUT0 #3 | | LES_CH4 #0 |
| 14 | PC5 | ACMP0_CH5<br>DAC0_N0 /<br>OPAMP_N0 | LETIM0_OUT1 #3 | | LES_CH5 #0 |
| 15 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| 16 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| 17 | PA8 | | | | |
| 18 | PA9 | | | | |
| 19 | PA10 | | | | |
| 20 | RESETn | Reset input, active low.<br>To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0 /<br>OPAMP_OUT0 | TIM1_CC2 #3<br>LETIM0_OUT0 #1 | | |
| 22 | PB12 | DAC0_OUT1 /<br>OPAMP_OUT1 | LETIM0_OUT1 #1 | | |
| 23 | AVDD_1 | Analog power supply 1. | | | |
| 24 | PB13 | HFXTAL_P | | US0_CLK #4/5<br>LEU0_TX #1 | |
| 25 | PB14 | HFXTAL_N | | US0_CS #4/5<br>LEU0_RX #1 | |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |
| 28 | PD0 | ADC0_CH0<br>DAC0_OUT0ALT #4/<br>OPAMP_OUT0ALT<br>OPAMP_OUT2 #1 | | US1_TX #1 | |
| 29 | PD1 | ADC0_CH1<br>DAC0_OUT1ALT #4/<br>OPAMP_OUT1ALT | TIM0_CC0 #3 | US1_RX #1 | |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Functionality** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **Description** |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| DAC0_N0 / OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| DAC0_N1 / OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 / OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| DAC0_P0 / OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| DAC0_P1 / OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | | | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | | | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | PC15 | | | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| TIM0_CC0 | PA0 | PA0 | | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM1_CC0 | PC13 | PE10 | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| US0_CLK | PE12 | | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |

## 4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32TG230* is shown in Table 4.3 (p. 51). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

***Table 4.3. GPIO Pinout***

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | - | - | - | - | PA10 | PA9 | PA8 | - | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | - | PB14 | PB13 | PB12 | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

## 4.4 Opamp Pinout Overview

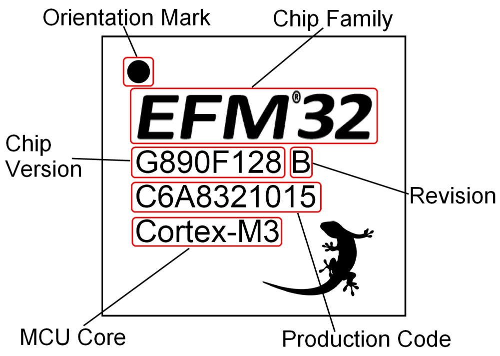
The specific opamp terminals available in *EFM32TG230* is shown in Figure 4.2 (p. 52) .

# 6 Chip Marking, Revision and Errata

## 6.1 Chip Marking

In the illustration below package fields and position are shown.

*Figure 6.1. Example Chip Marking (top view)*



## 6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 57) .

## 6.3 Errata

Please see the errata document for EFM32TG230 for description and resolution of device erratas. This document is available in Simplicity Studio and online at:
http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit

Added link to Environmental and Quality information.

Re-added missing DAC-data.

## 7.4 Revision 1.20

September 30th, 2013

Added I2C characterization data.

Corrected the DAC and OPAMP2 pin sharing information in the Alternate Functionality Pinout section.

Corrected GPIO operating voltage from 1.8 V to 1.85 V.

Corrected the ADC gain and offset measurement reference voltage from 2.25 to 2.5V.

Corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.

Document changed status from "Preliminary".

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

## 7.5 Revision 1.10

June 28th, 2013

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

## 7.6 Revision 1.00

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Added GPIO_EM4WU3, GPIO_EM4WU4 and GPIO_EM4WU5 pins and removed GPIO_EM4WU1 in the Alternate functionality overview table.

Other minor corrections.

## 7.7 Revision 0.96

May 4th, 2012

Corrected PCB footprint figures and tables.

## 7.8 Revision 0.95

February 27th, 2012

# List of Figures

silabs.com

ZERO
ARM Cortex-M0+

TINY
ARM Cortex-M3

GECKO
ARM Cortex-M3

LEOPARD
ARM Cortex-M3

GIANT
ARM Cortex-M3

WONDER
ARM Cortex-M4