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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	5MHz
Connectivity	SCI
Peripherals	LCD, PWM
Number of I/O	24
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f3854hv

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4. Register Indirect with Post-Increment or Pre-Decrement—@Rn+ or @–Rn:

- Register indirect with post-increment—@Rn+

  The @Rn+ mode is used with MOV instructions that load registers from memory.

  The register field of the instruction specifies a 16-bit general register containing the address of the operand. After the operand is accessed, the register is incremented by 1 for MOV.B or 2 for MOV.W. For MOV.W, the original contents of the 16-bit general register must be even.
- Register indirect with pre-decrement—@–Rn

  The @–Rn mode is used with MOV instructions that store register contents to memory.

  The register field of the instruction specifies a 16-bit general register which is decremented by 1 or 2 to obtain the address of the operand in memory. The register retains the decremented value. The size of the decrement is 1 for MOV.B or 2 for MOV.W. For MOV.W, the original contents of the register must be even.

5. Absolute Address—@aa:8 or @aa:16: The instruction specifies the absolute address of the operand in memory.

The absolute address may be 8 bits long (@aa:8) or 16 bits long (@aa:16). The MOV.B and bit manipulation instructions can use 8-bit absolute addresses. The MOV.B, MOV.W, JMP, and JSR instructions can use 16-bit absolute addresses.

For an 8-bit absolute address, the upper 8 bits are assumed to be 1 (H'FF). The address range is H'FF00 to H'FFFF (65280 to 65535).

6. Immediate—#xx:8 or #xx:16: The instruction contains an 8-bit operand (#xx:8) in its second byte, or a 16-bit operand (#xx:16) in its third and fourth bytes. Only MOV.W instructions can contain 16-bit immediate values.

The ADDS and SUBS instructions implicitly contain the value 1 or 2 as immediate data. Some bit manipulation instructions contain 3-bit immediate data in the second or fourth byte of the instruction, specifying a bit number.

7. Program-Counter Relative—@(d:8, PC): This mode is used in the Bcc and BSR instructions. An 8-bit displacement in byte 2 of the instruction code is sign-extended to 16 bits and added to the program counter contents to generate a branch destination address. The possible branching range is –126 to +128 bytes (–63 to +64 words) from the current address. The displacement should be an even number.

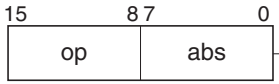
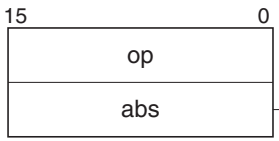
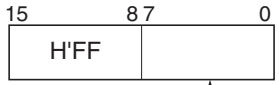
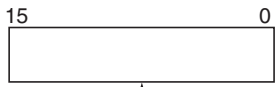
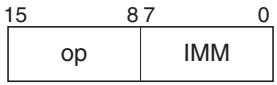
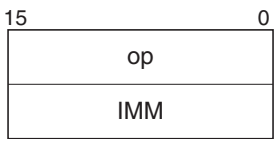
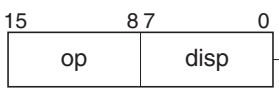
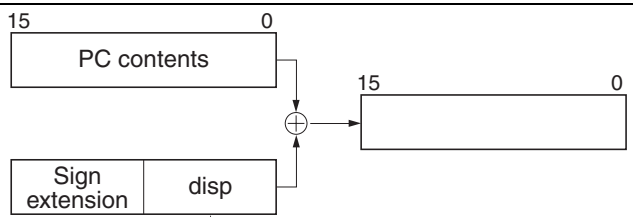
No.	Addressing Mode and Instruction Format	Effective Address Calculation Method	Effective Address (EA)
5	Absolute address @aa:8  @aa:16 	 	
6	Immediate #xx:8  #xx:16 		Operand is 1- or 2-byte immediate data
7	Program-counter relative @(d:8, PC) 		

Table 8.1 (b) H8/3854 Group Port Functions

Port	Description	Pins	Other Functions	Function Switching Register
Port 1	• 5-bit I/O port • Input pull-up MOS option	$P1_7$, $P1_5$/ $\overline{IRQ_3}$, $\overline{IRQ_1}$/ TMIF, TMIB	External interrupts 3, 1 Timer event input TMIF, TMIB	PMR1 TCRF, TMB
		$P1_2$, $P1_1$/ TMOFH, TMOFL	Timer F output compare	PMR1
		$P1_0$/TMOW	Timer A clock output	PMR1
Port 2	• 8-bit I/O port	$P2_7$ to $P2_1$	None	
	• Open drain output option • High-current port	$P2_0$/$\overline{IRQ_4}$/ $\overline{ADTRG}$	External interrupt 4 and A/D converter external trigger	PMR2 AMR
Port 4	• 1-bit input-only port	$P4_3$/$\overline{IRQ_0}$	External interrupt 0	PMR2
	• 3-bit I/O port	$P4_2$/TXD $P4_1$/RXD $P4_0$/SCK_3	SCI3 data output (TXD), data input (RXD), clock input/output (SCK_3)	SCR3 SMR
Port 5	• 8-bit I/O port • Input pull-up MOS option	$P5_7$ to $P5_0$/ $\overline{WKP_7}$ to $\overline{WKP_0}$	Wakeup input ($\overline{WKP_7}$ to $\overline{WKP_0}$)	PMR5
Port 9*	• 8-bit I/O port	$P9_7$ to $P9_0$	None	
Port A*	• 4-bit I/O port	PA_3 to PA_0	None	
Port B	• 4-bit input port	PB_7 to PB_4/ AN_7 to AN_4	A/D converter analog input	AMR

Note: * This I/O port is used to interface to the LCD controller.

Bits 4 and 3—Reserved Bits: Bits 4 and 3 are reserved; they are always read as 1, and cannot be modified.

Bits 2 to 0—Clock Select (TMC2 to TMC0): Bits 2 to 0 select the clock input to TCC. For external clock counting, either the rising or falling edge can be selected.

Bit 2: TMC2	Bit 1: TMC1	Bit 0: TMC0	Description
0	0	0	Internal clock: ϕ/8192 (initial value)
		1	Internal clock: ϕ/2048
	1	0	Internal clock: ϕ/512
		1	Internal clock: ϕ/64
1	0	0	Internal clock: ϕ/16
		1	Internal clock: ϕ/4
	1	0	Internal clock: ϕ_w/4
		1	External event (TMIC): rising or falling edge*

Note: * The edge of the external event signal is selected by bit IEG2 in the IRQ edge select register (IEGR). See section 3.3.2, Interrupt Control Registers for details on the IRQ edge select register. Be sure to set bit IRQ2 in port mode register 1 (PMR1) to 1 before setting bits TMC2 to TMC0 to 111.

Timer Counter C (TCC)

Bit	7	6	5	4	3	2	1	0
	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

TCC is an 8-bit read-only up-/down-counter, which is incremented or decremented by internal or external clock input. The clock source for input to this counter is selected by bits TMC2 to TMC0 in timer mode register C (TMC). TCC values can be read by the CPU at any time.

When TCC overflows (from H'FF to H'00 or to the value set in TLC) or underflows (from H'00 to H'FF or to the value set in TLC), the IRRTC bit in interrupt request register 2 (IRR2) is set to 1.

TCC is allocated to the same address as timer load register C (TLC).

Upon reset, TCC is initialized to H'00.

Auto-Reload Timer Operation: Setting bit TMC7 in TMC to 1 causes timer C to function as an 8-bit auto-reload timer. When a reload value is set in TLC, the same value is loaded into TCC, becoming the value from which TCC starts its count.

After the count value in TCC reaches H'FF (H'00), the next clock signal input causes timer C to overflow (underflow). The TLC value is then loaded TCC, and the count continues from that value. The overflow (underflow) period can be set within a range from 1 to 256 input clocks, depending on the TLC value.

The clock sources, up/down control, and interrupts in auto-reload mode are the same as in interval mode.

In auto-reload mode (TMC7 = 1), when a new value is set in TLC, the TLC value is also set in TCC.

Event Counter Operation: Timer C can operate as an event counter, counting an event signal input at pin TMIC. External event counting is selected by setting TMC bits TMC2 to TMC0 to all 1s (111). TCC counts up or down at the rising or falling edge of the input at pin TMIC.

When timer C is used to count external event inputs, bit IRQ2 in port mode register 1 (PMR1) should be set to 1, and bit IEN2 in interrupt enable register 1 (IENR1) should be cleared to 0 to disable IRQ_2 interrupt requests.

TCC Up/Down Control by Hardware: The counting direction of timer C can be controlled by input at pin UD. When bit TMC6 in TMC is set to 1, high-level input at the UD pin selects down-counting, while low-level input selects up-counting.

When using input at pin UD for this control function, set the UD bit in port mode register 2 (PMR2) to 1.

An overflow period of 1 to 256 times the selected clock can be set.

Block Diagram

Figure 9.8 shows a block diagram of the watchdog timer.

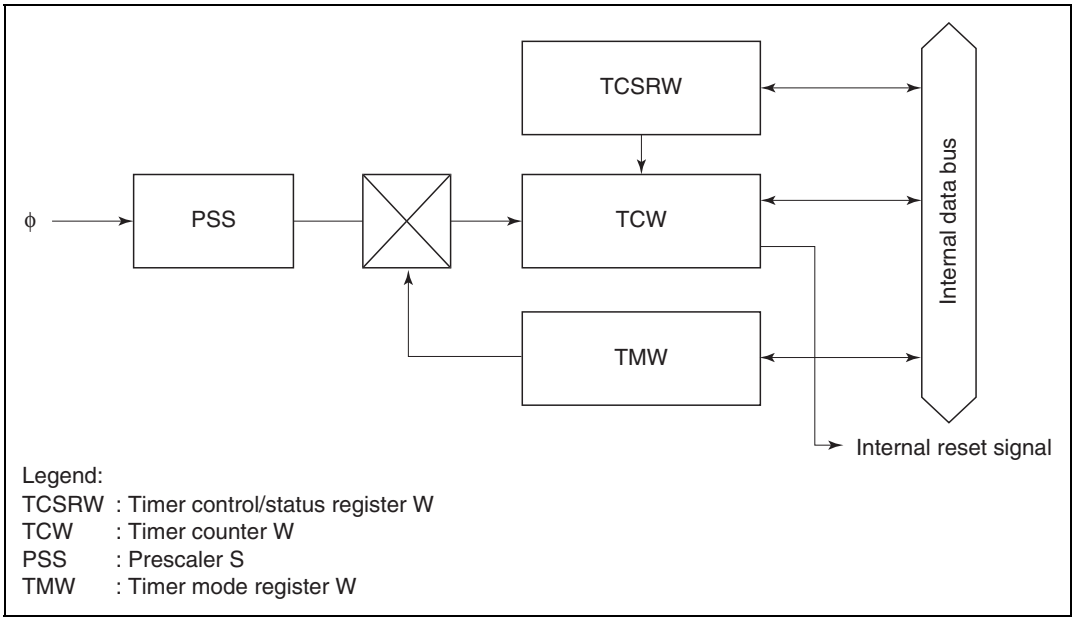


Figure 9.8 Block Diagram of Watchdog Timer

Register Configuration

Table 9.14 shows the watchdog timer register configuration. These registers are valid only in the F-ZTAT version. In the mask ROM version, read accesses to the corresponding addresses will always return 1, and writes are invalid.

Table 9.14 Watchdog Timer Registers

Name	Abbr.	R/W	Initial Value	Address
Timer control/status register W	TCSRW	R/W	H'AA	H'FF90
Timer counter W	TCW	R/W	H'00	H'FF91
Timer mode register W	TMW	R/W	H'FF	H'FF92

Sending a Mark or Break Signal: When TE is cleared to 0 the TXD pin becomes an I/O port, the level and direction (input or output) of which are determined by the PDR and PCR bits. This feature can be used to place the TXD pin in the mark state or send a break signal.

To place the serial communication line in the mark (1) state before TE is set to 1, set the PDR and PCR bits both to 1. Since TE is cleared to 0, TXD becomes a general output port outputting the value 1.

To send a break signal during data transmission, set the PCR bit to 1 and clear the PDR bit to 0, then clear TE to 0. When TE is cleared to 0 the transmitter is initialized, regardless of its current state, so the TXD pin becomes an output port outputting the value 0.

Receive Error Flags and Transmit Operation (Sysnchronous Mode Only): When a receive error flag (OER, PER, or FER) is set to 1, SCI3 will not start transmitting even if TDRE is cleared to 0. Be sure to clear the receive error flags to 0 when starting to transmit. Note that clearing RE to 0 does not clear the receive error flags.

Receive Data Sampling Timing and Receive Margin in Asynchronous Mode: In asynchronous mode SCI3 operates on a base clock with 16 times the bit rate frequency. In receiving, SCI3 synchronizes internally with the falling edge of the start bit, which it samples on the base clock. Receive data is latched at the rising edge of the eighth base clock pulse. See figure 10.25.

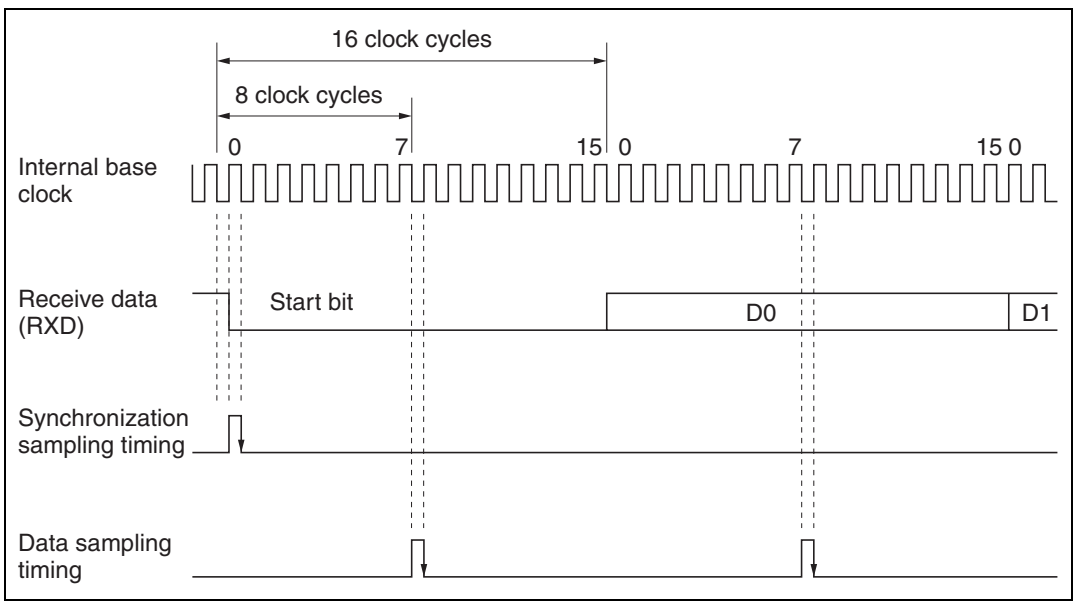


Figure 10.25 Receive Data Sampling Timing in Asynchronous Mode

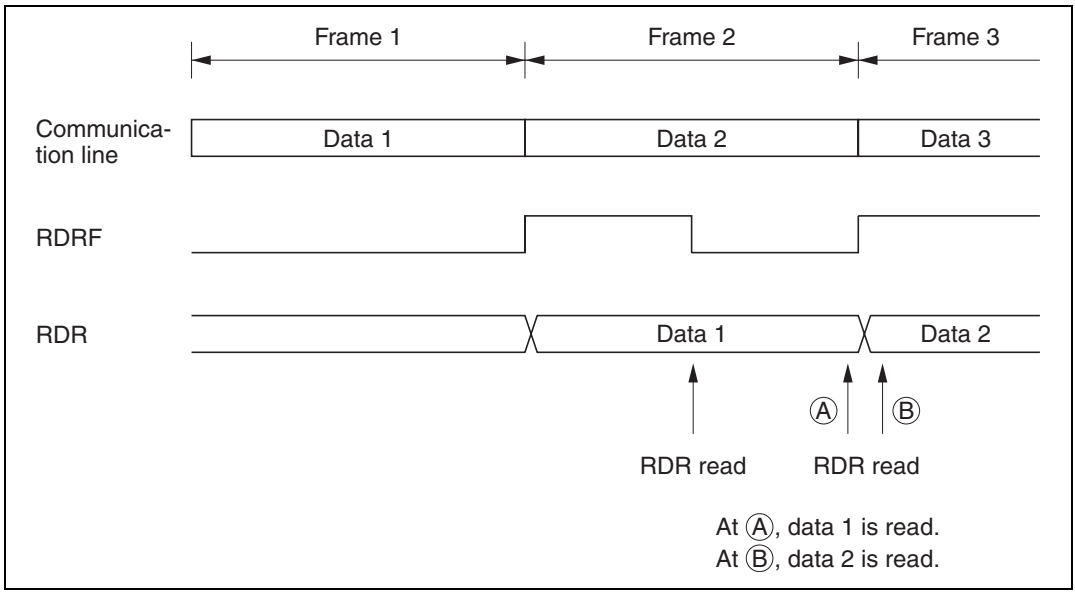


Figure 10.26 Relationship between Data and RDR Read Timing

To avoid the situation described above, after RDRF is confirmed to be 1, RDR should only be read once and should not be read twice or more.

When the same data must be read more than once, the data read the first time should be copied to RAM, for example, and the copied data should be used. An alternative is to read RDR but leave a safe margin of time before reception of the next frame is completed. Specifically, reading of RDR should be completed before bit 7 is transferred in synchronous mode, or before the stop bit is transferred in asynchronous mode.

Caution on Switching of SCK_3 Function: If pin SCK_3 is used as a clock output pin by SCI3 in synchronous mode and is then switched to a general input/output pin (a pin with a different function), the pin outputs a low level signal for half a system clock (ϕ) cycle immediately after it is switched.

This can be prevented by either of the following methods according to the situation.

1. When an SCK_3 function is switched from clock output to non clock-output
   When stopping data transfer, issue one instruction to clear bits TE and RE in SCR3 to 0 and to set bits CKE1 and CKE0 to 1 and 0, respectively. In this case, bit COM in SMR should be left 1. The above prevents SCK_3 from being used as a general input/output pin. To avoid an intermediate level of voltage from being applied to SCK_3, the line connected to SCK_3 should be pulled up to the V_{CC} level via a resistor, or supplied with output from an external device.

13.2.4 Address Register (LR2)

Bit	7	6	5	4	3	2	1	0
	XA2	XA1	XA0	YA4	YA3	YA2	YA1	YA0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

LR2 is an 8-bit write-only register that sets the display memory X- and Y-direction addresses accessed by the CPU.

Upon reset, LR2 is initialized to H'00.

Bits 7 to 5—X Address Setting (XA2 to XA0): Bits 7 to 5 set the display memory X-direction address. A value from H'0 to H'7 can be set, but if the SOB bit in LR0 is set to 1, display data H'7 is invalid with 1/16 duty, and display data from H'5 to H'7 is invalid with 1/32 duty.

When the INC bit in LR1 is set to 1, the address is automatically incremented after the access specified by the RMW bit in LR1, and is cleared after an access with the maximum value for the valid display data area. When INC is 0 and YA4 to YA0 represent the maximum value for the valid display data area, the address is incremented after the access specified by RMW.

Bits 4 to 0—Y Address Setting (YA4 to YA0): Bits 4 to 0 set the display memory Y-direction address. A value from H'00 to H'1F can be set, but display data from H'10 to H'1F is invalid with 1/16 duty, and display data from H'08 to H'1F is invalid with 1/8 duty.

When the INC bit in LR1 is cleared to 0, the address is automatically incremented after the access specified by the RMW bit in LR1, and is cleared after an access with the maximum value for the valid display data area. When INC is 1 and XA2 to XA0 represent the maximum value for the valid display data area, the address is incremented after the access specified by RMW.

Table 14.3 Register Settings, Division Ratios, and Frame Frequencies at Each Display Duty

				Display Duty 1/N			
				1/8		1/16	
				Subclock Frequency f_W (kHz)			
				32.768	38.4	32.768	38.4
FS2	FS1	FS0	Division ratio r	Frame Frequency f_F (Hz)			
0	0	0	2	2048.0	2400.0	1024.0	1200.0
		1	4	1024.0	1200.0	512.0	600.0
	1	0	8	512.0	600.0	256.0	300.0
		1	16	256.0	300.0	128.0	150.0
1	0	0	32	128.0	150.0	64.0	75.0
		1	64	64.0	75.0	32.0	37.5
	1	0	128	32.0	37.5	16.0	18.8
		1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited

14.2.6 Display Data Register (LR4)

Bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0
Initial value	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LR4 is an 8-bit read/write register used to perform read/write access to the display memory specified by XA2 to XA0 and YA3 to YA0 in LR2.

In a write to display memory, the write is performed directly to the display memory via this register. In a read, the data is temporarily latched into this register before being output to the bus.

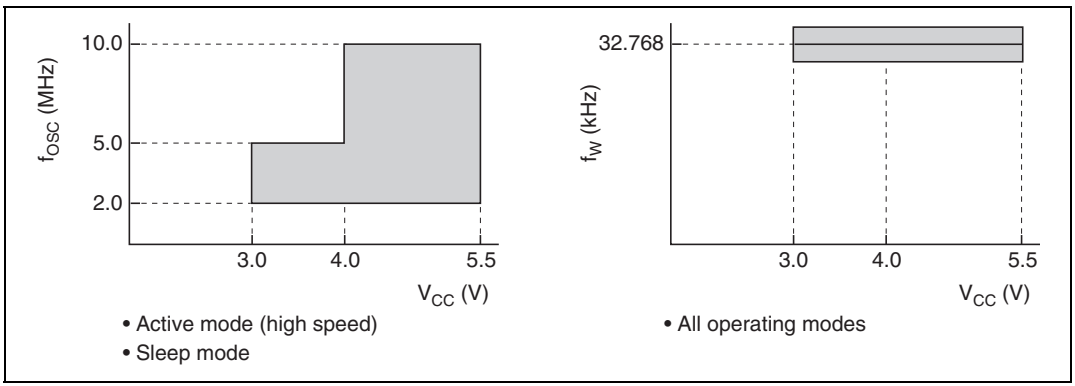
After a reset, the display memory and LR4 contents are undefined.

15.2 H8/3855, H8/3856, and H8/3857 Electrical Characteristics (Standard Specifications)

15.2.1 Power Supply Voltage and Operating Range

The power supply voltage and operating range of the H8/3855, H8/3856, and H8/3857 are indicated by the shaded region in the figures below.

(1) Power Supply Voltage vs. Oscillator Frequency Range



15.2.5 LCD Characteristics

Table 15.8 shows the LCD characteristics, and table 15.9 shows the step-up circuit characteristics, of the H8/3855, H8/3856, and H8/3857.

Table 15.8 LCD Characteristics of H8/3855, H8/3856, and H8/3857

V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C*[4], including subactive mode, unless otherwise specified.

				Values				
Item	**Symbol**	**Applicable Pins**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**	**Notes**
Common driver on-resistance	R_{COM}	COM1 to COM32	±Id = 0.05 mA, V_{LCD} = 4 V	—	6	20	kΩ	*[1]
Segment driver on-resistance	R_{SEG}	SEG1 to SEG64	±Id = 0.05 mA, V_{LCD} = 4 V	—	6	20	kΩ	*[1]
LCD power supply current	I_{EE}	V_{LCD}	V_{LCD} = 5.5 V, f_x = 32.768 kHz	—	20	40	μA	*[2]
LCD power supply voltage	V_{LCD}	V_{LCD}		V_{CC}	—	7.0	V	*[3]

Notes: 1. Applies to the resistance (R_{COM}) between the V1OUT, V2OUT, V5OUT, and V_{SS} pins and the common signal pins (COM1 to COM32), and the resistance (R_{SEG}) between the V1OUT, V3OUT, V4OUT, and V_{SS} pins and the segment signal pins (SEG1 to SEG64), when Id is flowing in the pins.

2. This is the current when the built-in op-amps are operating and display is halted (all driver outputs are at the V_{SS} level).
3. Specifies the voltage range in which the COM/SEG pin output voltages are within the LCD reference voltage values (V1, V2, V3, V4, V5, and V_{SS}) ±0.15 V in the unloaded state. A voltage not lower than V_{CC} must be applied to V_{LCD}.
4. The guaranteed temperature as an electrical characteristic for die type products is 75°C.

Section 16 Electrical Characteristics (H8/3854 Group)

16.1 H8/3852, H8/3853, and H8/3854 Absolute Maximum Ratings (Standard Specifications)

Table 16.1 shows the absolute maximum ratings.

Table 16.1 Absolute Maximum Ratings

Item		Symbol	Value	Unit	Notes
Power supply voltage		V_{CC}	–0.3 to +7.0	V	
Programming voltage (FWE)		V_{in}	–0.3 to V_{CC} +0.3	V	*1
Input voltage	Except LCD power supply	V_{in}	–0.3 to V_{CC} +0.3	V	
	LCD power supply	V_{in}	–0.3 to V_{CC} +0.3	V	*2
Operating temperature		T_{opr}	–20 to +75	°C	*3
Storage temperature		T_{stg}	–55 to +125	°C	

Caution: Permanent damage may occur to the chip if maximum ratings are exceeded. Normal operation should be under the conditions specified in Electrical Characteristics. Exceeding these values can result in incorrect operation and reduced reliability.

Notes: 1. 12 V must not be applied to the FWE pin, as this will permanently damage the device.

2. When the internal power supply and internal bleeder resistances are not used, and the LCD drive voltages are supplied directly from an external source, this applies to V1OUT, V2OUT, V3OUT, V4OUT, and V5OUT.

3. The operating temperature range when programming/erasing flash memory is: T_a = 0°C to +75°C.

16.2.5 LCD Characteristics

Table 16.7 shows the LCD characteristics of the H8/3852, H8/3853, and H8/3854.

Table 16.7 LCD Characteristics of H8/3852, H8/3853, and H8/3854

V_{CC} = 2.7 V to 5.5 V of the mask ROM version of H8/3852, H8/3853, and H8/3854,
V_{CC} = 3.0 V to 5.5 V of H8/3854F, V_{SS} = 0.0 V, T_a = –20°C to +75°C*[2], including subactive mode, unless otherwise specified.

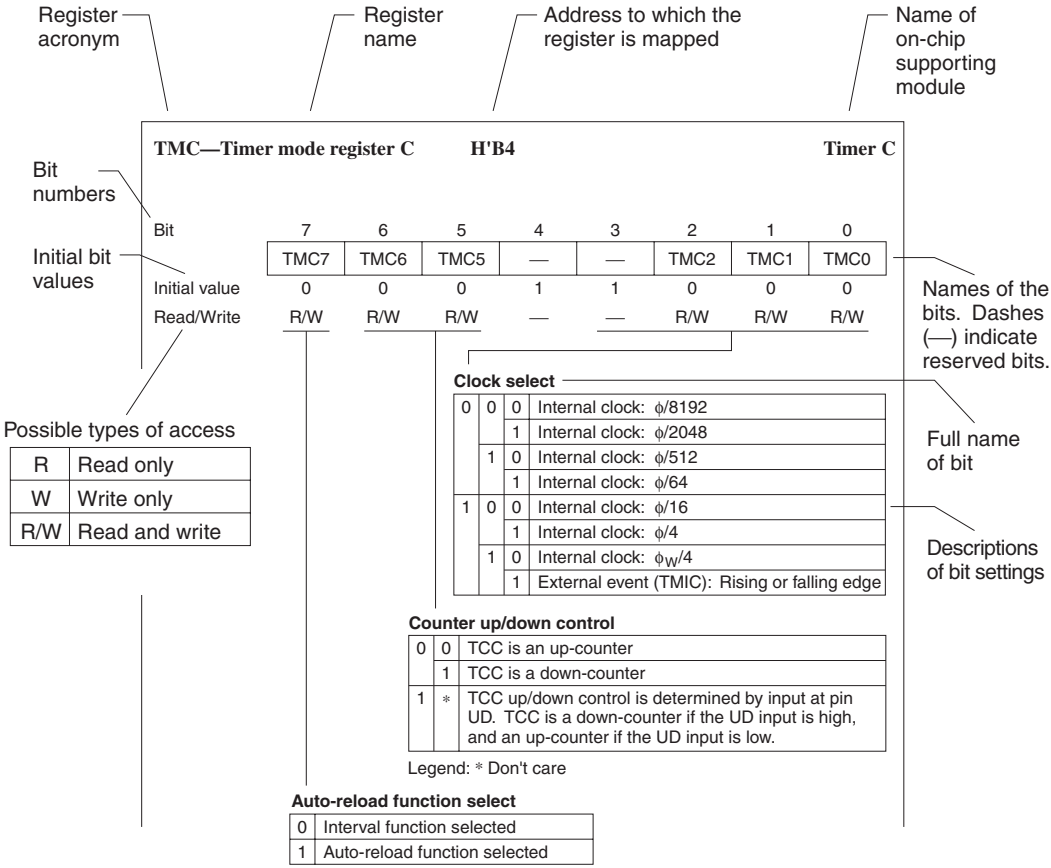
				Values				
Item	**Symbol**	**Applicable Pins**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**	**Notes**
Common driver on-resistance	R_{COM}	COM1 to COM16	±Id = 0.05 mA, V_{CC} = 4 V	—	6	20	kΩ	*[1]
Segment driver on-resistance	R_{SEG}	SEG1 to SEG40	±Id = 0.05 mA, V_{CC} = 4 V	—	6	20	kΩ	*[1]
LCD power supply bleeder resistance	R_{LCD}		V_{CC} = 5.0 V, f_x = 32.768 kHz	200	400	700	kΩ	

Notes: 1. Applies to the resistance (R_{COM}) between the V1OUT, V2OUT, V5OUT, and V_{SS} pins and the common signal pins (COM1 to COM16), and the resistance (R_{SEG}) between the V1OUT, V3OUT, V4OUT, and V_{SS} pins and the segment signal pins (SEG1 to SEG40), when Id is flowing in the pins.

The voltage applied to V1OUT through V5OUT must not exceed V_{CC}.

2. The guaranteed temperature as an electrical characteristic for die type products is 75°C.

B.2 Register Descriptions



EBR—Erase block register **H'83** **Flash memory (On-chip flash memory version only)**

Bit	:	7	6	5	4	3	2	1	0
		—	EB6	EB5	EB4	EB3	EB2	EB1	EB0
Initial value	:	0	0	0	0	0	0	0	0
Read/Write	:	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Flash memory erase blocks

Block (Size)	Addresses
EB0 (1 kbyte)	H'0000 to H'03FF
EB1 (1 kbyte)	H'0400 to H'07FF
EB2 (1 kbyte)	H'0800 to H'0BFF
EB3 (1 kbyte)	H'0C00 to H'0FFF
EB4 (28 kbytes)	H'1000 to H'7FFF
EB5 (16 kbytes)	H'8000 to H'BFFF
EB6 (12 kbytes)	H'C000 to H'EDFF

PMR5—Port mode register 5 **H'CC** **I/O ports**

Bit	7	6	5	4	3	2	1	0
	WKP_7	WKP_6	WKP_5	WKP_4	WKP_3	WKP_2	WKP_1	WKP_0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

$P5_n/\overline{WKP_n}$ pin function switch

0	Functions as $P5_n$ I/O pin
1	Functions as $\overline{WKP}_n$ input pin

PWCR—PWM control register **H'D0** **14-bit PWM (H8/3857 Group only)**

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	PWCR0
Initial value	1	1	1	1	1	1	1	0
Read/Write	—	—	—	—	—	—	—	W

Clock select

0	The input clock is $\phi/2$ ($t\phi^* = 2/\phi$). The conversion period is 16,384/ϕ, with a minimum modulation width of 1/ϕ
1	The input clock is $\phi/4$ ($t\phi^* = 4/\phi$). The conversion period is 32,768/ϕ, with a minimum modulation width of 2/ϕ

Note: *$t\phi$: Period of PWM input clock

PWDRU—PWM data register U **H'D1** **14-bit PWM (H8/3857 Group only)**

Bit	7	6	5	4	3	2	1	0
	—	—	PWDRU5	PWDRU4	PWDRU3	PWDRU2	PWDUR1	PWDRU0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

Upper 6 bits of data for generating PWM waveform

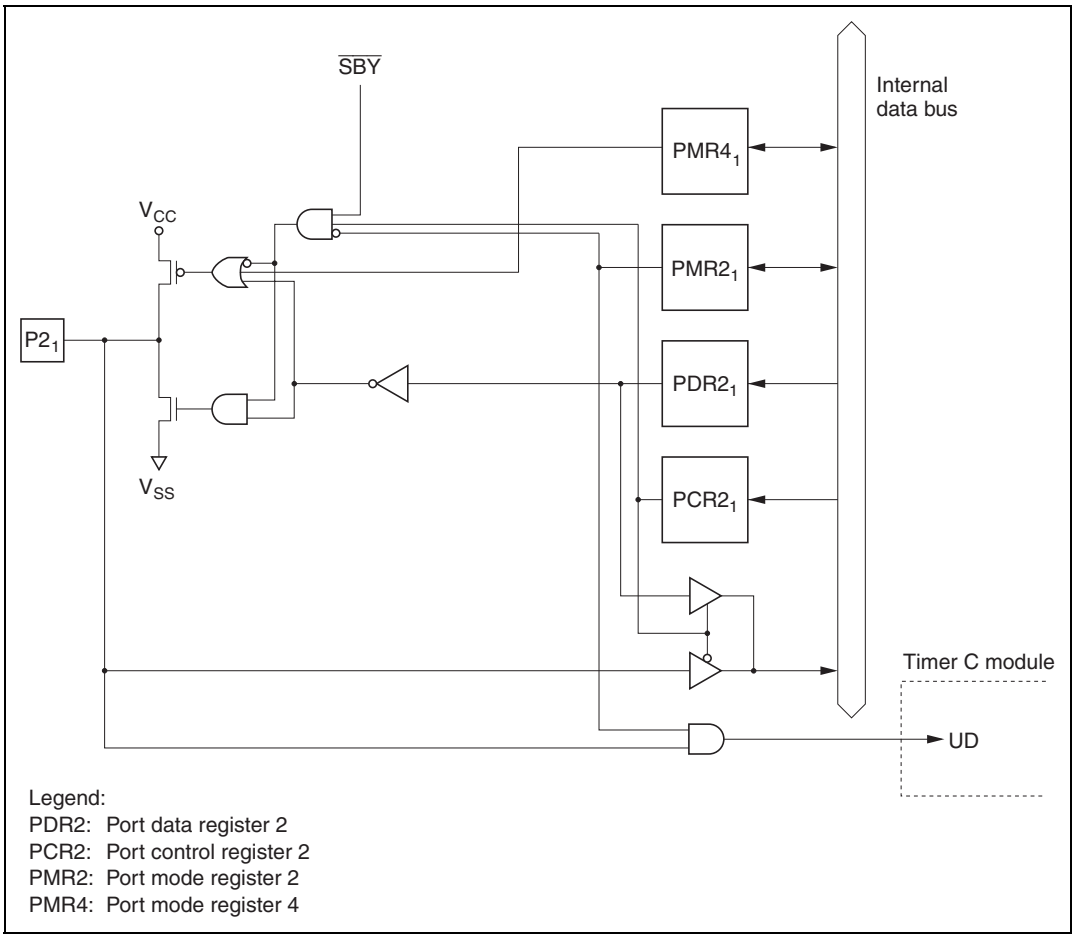


Figure C.2 (b) Port 2 Block Diagram (Pin $P2_1$: H8/3857 Group)

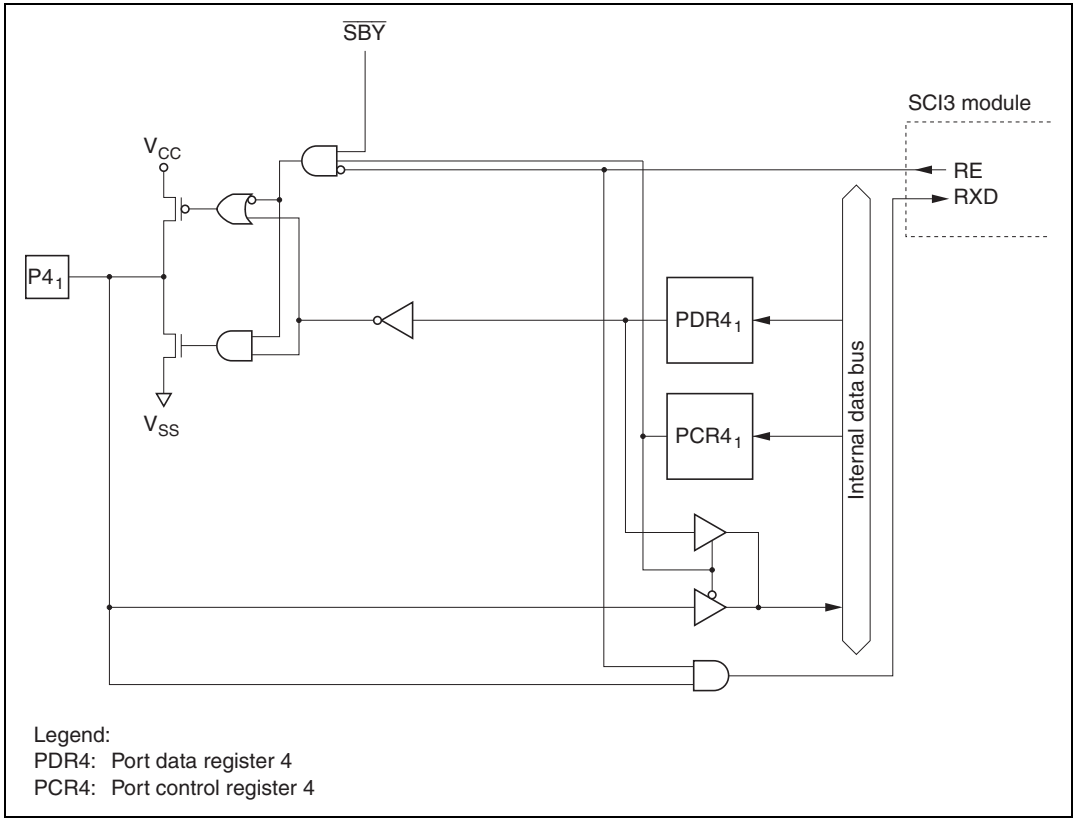


Figure C.4 (c) Port 4 Block Diagram (Pin $P4_1$)