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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300L
Core Size	8-Bit
Speed	5MHz
Connectivity	SCI
Peripherals	LCD, PWM
Number of I/O	35
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f3857fqv

Table 1.1 Features

Item	Description
CPU	High-speed H8/300L CPU • General-register architecture General registers: Sixteen 8-bit registers (can be used as eight 16-bit registers) • Operating speed — Max. operating speed: 5 MHz — Add/subtract: 0.4 μs (operating at 5 MHz) — Multiply/divide: 2.8 μs (operating at 5 MHz) — Can run on 32.768 kHz subclock • Instruction set compatible with H8/300 CPU — Instruction length of 2 bytes or 4 bytes — Basic arithmetic operations between registers — MOV instruction for data transfer between memory and registers Typical instructions • Multiply (8 bits × 8 bits) • Divide (16 bits ÷ 8 bits) • Bit accumulator • Register-indirect designation of bit position
Interrupts	H8/3857 Group: 29 interrupt sources • 13 external interrupt sources: IRQ_4 to IRQ_0, WKP_7 to WKP_0 • 16 internal interrupt sources H8/3854 Group: 26 interrupt sources • 12 external interrupt sources: IRQ_4, IRQ_3, IRQ_1, IRQ_0, WKP_7 to WKP_0 • 14 internal interrupt sources
Clock pulse generators	Two on-chip clock pulse generators • System clock pulse generator: 1 to 10 MHz • Subclock pulse generator: 32.768 kHz
Power-down modes	Six power-down modes • Sleep mode • Standby mode • Watch mode • Subsleep mode • Subactive mode • Active (medium-speed) mode

Table 5.2 Internal State in Each Operation Mode

Function		Active Mode: High Speed	Active Mode: Medium Speed	Sleep Mode	Watch Mode	Subactive Mode	Subsleep Mode	Standby Mode
System clock oscillator		Functions	Functions	Functions	Halted	Halted	Halted	Halted
Subclock oscillator		Functions	Functions	Functions	Functions	Functions	Functions	Functions
CPU operation	Instructions	Functions	Functions	Halted	Halted	Functions	Halted	Halted
	RAM			Retained	Retained		Retained	Retained
	Registers							
	I/O							Retained*1
External interrupts	IRQ_0	Functions	Functions	Functions	Functions	Functions	Functions	Functions
	IRQ_1				Retained*4			
	IRQ_2*6							Retained*4
	IRQ_3							
	IRQ_4							
	WKP_0	Functions	Functions	Functions	Functions	Functions	Functions	Functions
	WKP_1							
	WKP_2							
	WKP_3							
	WKP_4							
	WKP_5							
	WKP_6							
	WKP_7							
Peripheral module functions	Timer A	Functions	Functions	Functions	Functions*3	Functions*3	Functions*3	Retained
	Timer B				Retained	Retained	Retained	
	Timer C*6					Functions/ Retained*2	Functions/ Retained*2	
	Timer F					Retained	Retained	
	SCI1*6	Functions	Functions	Functions	Retained	Retained	Retained	Retained
	SCI3				Reset	Reset	Reset	Reset
	PWM*6	Functions	Functions	Retained	Retained	Retained	Retained	Retained
	A/D	Functions	Functions	Functions	Retained	Retained	Retained	Retained
	LCD*5	Functions	Functions	Functions	Functions	Functions	Functions	Retained

Notes:
1. Register contents held; high-impedance output.
2. Functions only if external clock or $\phi_W/4$ internal clock is selected; otherwise halted and retained.
3. Functions when timekeeping time-base function is selected.
4. External interrupt requests are ignored. The interrupt request register contents are not affected.
5. In module standby mode, only the clock supplied to the LCD controller is stopped. Register values are retained, and all outputs go to the V_{SS} potential.
6. This is a function of the H8/3857 Group only, and is not provided in the H8/3854 Group.

Port Pull-up Control Register 5 (PUCR5)

Bit	7	6	5	4	3	2	1	0
	$PUCR5_7$	$PUCR5_6$	$PUCR5_5$	$PUCR5_4$	$PUCR5_3$	$PUCR5_2$	$PUCR5_1$	$PUCR5_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PUCR5 bits control the on/off state of pin $P5_7$–$P5_0$ MOS pull-ups. When a PCR5 bit is cleared to 0, setting the corresponding PUCR5 bit to 1 turns on the MOS pull-up for the corresponding pin, while clearing the bit to 0 turns off the MOS pull-up.

Upon reset, PUCR5 is initialized to H'00.

Port Mode Register 5 (PMR5)

Bit	7	6	5	4	3	2	1	0
	WKP_7	WKP_6	WKP_5	WKP_4	WKP_3	WKP_2	WKP_1	WKP_0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PMR5 is an 8-bit read/write register, controlling the selection of pin functions for port 5 pins.

Upon reset, PMR5 is initialized to H'00.

Bit n—$P5_n/\overline{WKP_n}$ Pin Function Switch (WKPn): This bit selects whether pin $P5_n/\overline{WKP_n}$ is used as $P5_n$ or as $\overline{WKP_n}$.

Bit n: WKPn	Description	
0	Functions as $P5_n$ I/O pin	(initial value)
1	Functions as $\overline{WKP_n}$ input pin	

Note: n = 7 to 0

Timer Counter B (TCB)

Bit	7	6	5	4	3	2	1	0
	TCB7	TCB6	TCB5	TCB4	TCB3	TCB2	TCB1	TCB0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

TCB is an 8-bit read-only up-counter, which is incremented by internal clock or external event input. The clock source for input to this counter is selected by bits TMB2 to TMB0 in timer mode register B (TMB). TCB values can be read by the CPU at any time.

When TCB overflows from H'FF to H'00 or to the value set in TLB, the IRRTB bit in interrupt request register 2 (IRR2) is set to 1.

TCB is allocated to the same address as timer load register B (TLB).

Upon reset, TCB is initialized to H'00.

Timer Load Register B (TLB)

Bit	7	6	5	4	3	2	1	0
	TLB7	TLB6	TLB5	TLB4	TLB3	TLB2	TLB1	TLB0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

TLB is an 8-bit write-only register for setting the reload value of timer counter B.

When a reload value is set in TLB, the same value is loaded into timer counter B (TCB) as well, and TCB starts counting up from that value. When TCB overflows during operation in auto-reload mode, the TLB value is loaded into TCB. Accordingly, overflow periods can be set within the range of 1 to 256 input clocks.

The same address is allocated to TLB as to TCB.

Upon reset, TLB is initialized to H'00.

The receive shift register (RSR) is for receiving serial data.

Serial data is input in LSB (bit 0) order into RSR from pin RXD, converting it to parallel data. After each byte of data has been received, the byte is automatically transferred to the receive data register (RDR).

RSR cannot be read or written directly by the CPU.

Receive Data Register (RDR)

Bit	7	6	5	4	3	2	1	0
	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

The receive data register (RDR) is an 8-bit register for storing received serial data.

Each time a byte of data is received, the received data is transferred from the receive shift register (RSR) to RDR, completing a receive operation. Thereafter RSR again becomes ready to receive new data. RSR and RDR form a double buffer mechanism that allows data to be received continuously.

RDR is exclusively for receiving data and cannot be written by the CPU.

RDR is initialized to H'00 upon reset or in standby mode, watch mode, subactive mode, or subsleep mode.

Transmit Shift Register (TSR)

Bit	7	6	5	4	3	2	1	0
Read/Write	—	—	—	—	—	—	—	—

The transmit shift register (TSR) is for transmitting serial data.

Transmit data is first transferred from the transmit data register (TDR) to TSR, then is transmitted from pin TXD, starting from the LSB (bit 0).

After one byte of data has been sent, the next byte is automatically transferred from TDR to TSR, and the next transmission begins. If no data has been written to TDR (1 is set in TDRE), there is no data transfer from TDR to TSR.

Bit 4—Framing Error (FER): Bit 4 is a status flag indicating that a framing error has occurred during asynchronous receiving.

Bit 4: FER	Description
0	Indicates that data receiving is in progress or has been completed*1 (initial value) Clearing condition: After reading FER = 1, cleared by writing 0 to FER
1	Indicates that a framing error occurred in data receiving Setting condition: The stop bit at the end of receive data is checked for a value of 1 and found to be 0*2

Notes: 1. When bit RE in serial control register 3 (SCR3) is cleared to 0, FER is unaffected and keeps its previous state.
2. When two stop bits are used only the first stop bit is checked, not the second. When a framing error occurs, receive data is transferred to RDR but RDRF is not set. While FER is set to 1, data receiving cannot be continued. In synchronous mode, data transmitting cannot be continued either.

Bit 3—Parity Error (PER): Bit 3 is a status flag indicating that a parity error has occurred during asynchronous receiving.

Bit 3: PER	Description
0	Indicates that data receiving is in progress or has been completed*1 (initial value) Clearing condition: After reading PER = 1, cleared by writing 0 to PER
1	Indicates that a parity error occurred in data receiving*2 Setting condition: When the sum of 1s in received data plus the parity bit does not match the parity mode bit (PM) setting in the serial mode register (SMR)

Notes: 1. When bit RE in serial control register 3 (SCR3) is cleared to 0, PER is unaffected and keeps its previous state.
2. When a parity error occurs, receive data is transferred to RDR but RDRF is not set. While PER is set to 1, data receiving cannot be continued. In synchronous mode, data transmitting cannot be continued either.

Clock

The clock source is determined by bit COM in SMR and bits CKE1 and CKE0 in serial control register 3 (SCR3). See table 10.12 for the settings. Either an internal clock source can be used to run the built-in baud rate generator, or an external clock source can be input at pin SCK_3.

When an external clock is input at pin SCK_3, it should have a frequency 16 times the desired bit rate.

When an internal clock source is used, SCK_3 is used as the clock output pin. The clock output has the same frequency as the serial bit rate, and is synchronized as in figure 10.8 so that the rising edge of the clock occurs in the center of each bit of transmit/receive data.

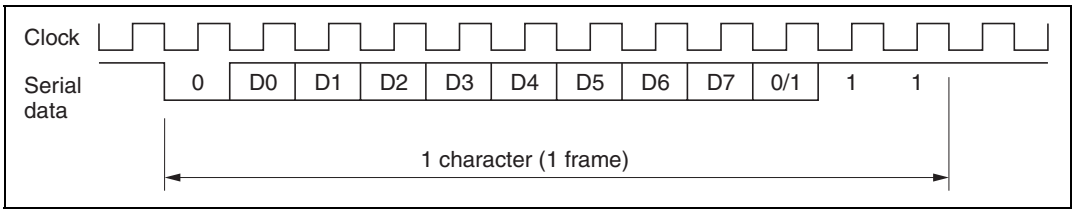


Figure 10.8 Phase Relation of Output Clock and Communication Data in Asynchronous Mode (8-Bit Data, Parity Bit Added, and 2 Stop Bits)

Data Transmit/Receive Operations

SCI3 Initialization: Before data is sent or received, bits TE and RE in serial control register 3 (SCR3) must be cleared to 0, after which initialization can be performed using the procedure shown in figure 10.9.

Note: When modifying the operation mode, transfer format or other settings, always be sure to clear bits TE and RE first. When TE is cleared to 0, bit TDRE will be set to 1. Clearing RE does not clear the status flags RDRF, PER, FER, or OER, or alter the contents of the receive data register (RDR).
When an external clock is used in asynchronous mode, do not stop the clock during operation, including during initialization. When an external clock is used in synchronous mode, do not supply the clock during initialization.

Figure 10.13 shows a typical SCI3 data receive operation in asynchronous mode.

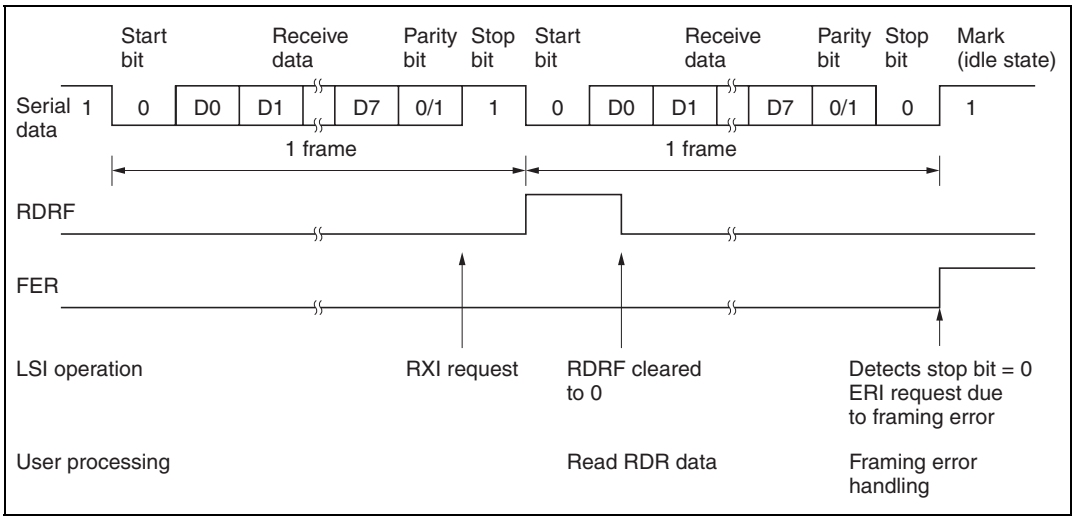


Figure 10.13 Typical Receive Operation in Asynchronous Mode (8-Bit Data, Parity Bit Added, and 1 Stop Bit)

10.3.5 Operation in Synchronous Mode

In synchronous mode, data is sent or received in synchronization with clock pulses. This mode is suited to high-speed serial communication.

SCI3 consists of independent transmit and receive modules, so full duplex communication is possible, sharing the same clock between both modules. Both the transmit and receive modules have a double-buffer configuration. This allows data to be written during a transmit operation so that data can be transmitted continuously, and enables data to be read during a receive operation so that data can be received continuously.

Transmit/Receive Format

Figure 10.14 shows the general communication data format for synchronous communication.

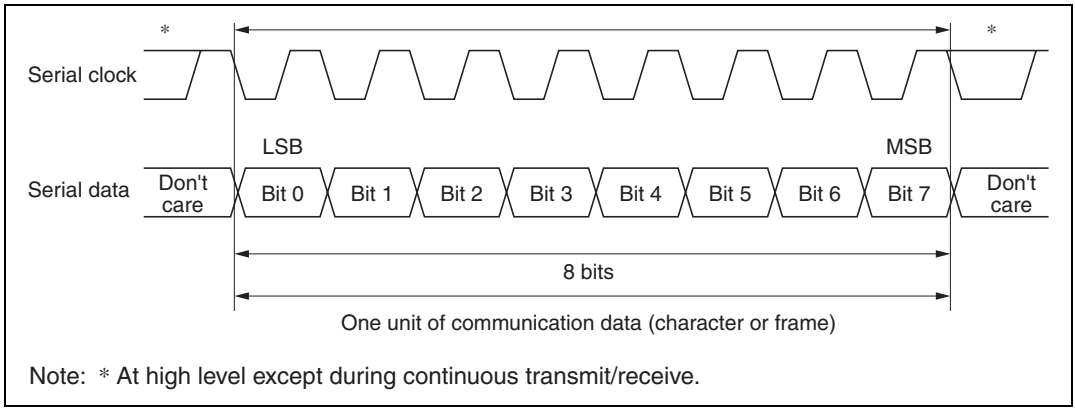


Figure 10.14 Data Format in Synchronous Communication Mode

In synchronous communication, data on the communication line is output from one falling edge of the serial clock until the next falling edge. Data is guaranteed valid at the rising edge of the serial clock.

One character of data starts from the LSB and ends with the MSB. The communication line retains the MSB state after the MSB is output.

In synchronous receive mode, SCI3 latches receive data in synchronization with the rising edge of the serial clock.

The transmit/receive format is fixed at 8-bit data. No parity bit or multiprocessor bit is added in this mode.

Clock

Either an internal clock from the built-in baud rate generator is used, or an external clock is input at pin SCK_3. The choice of clock sources is designated by bit COM in SMR and bits CKE1 and CKE0 in serial control register 3 (SCR3). See table 10.12 for details on selecting the clock source.

When operation is based on an internal clock, a serial clock is output at pin SCK_3. Eight clock pulses are output per character of transmit/receive data. When no transmit or receive operation is being performed, the pin is held at the high level.

Receiving: Figure 10.17 shows a typical flow chart for receiving data. After SCI3 initialization, follow the procedure below.

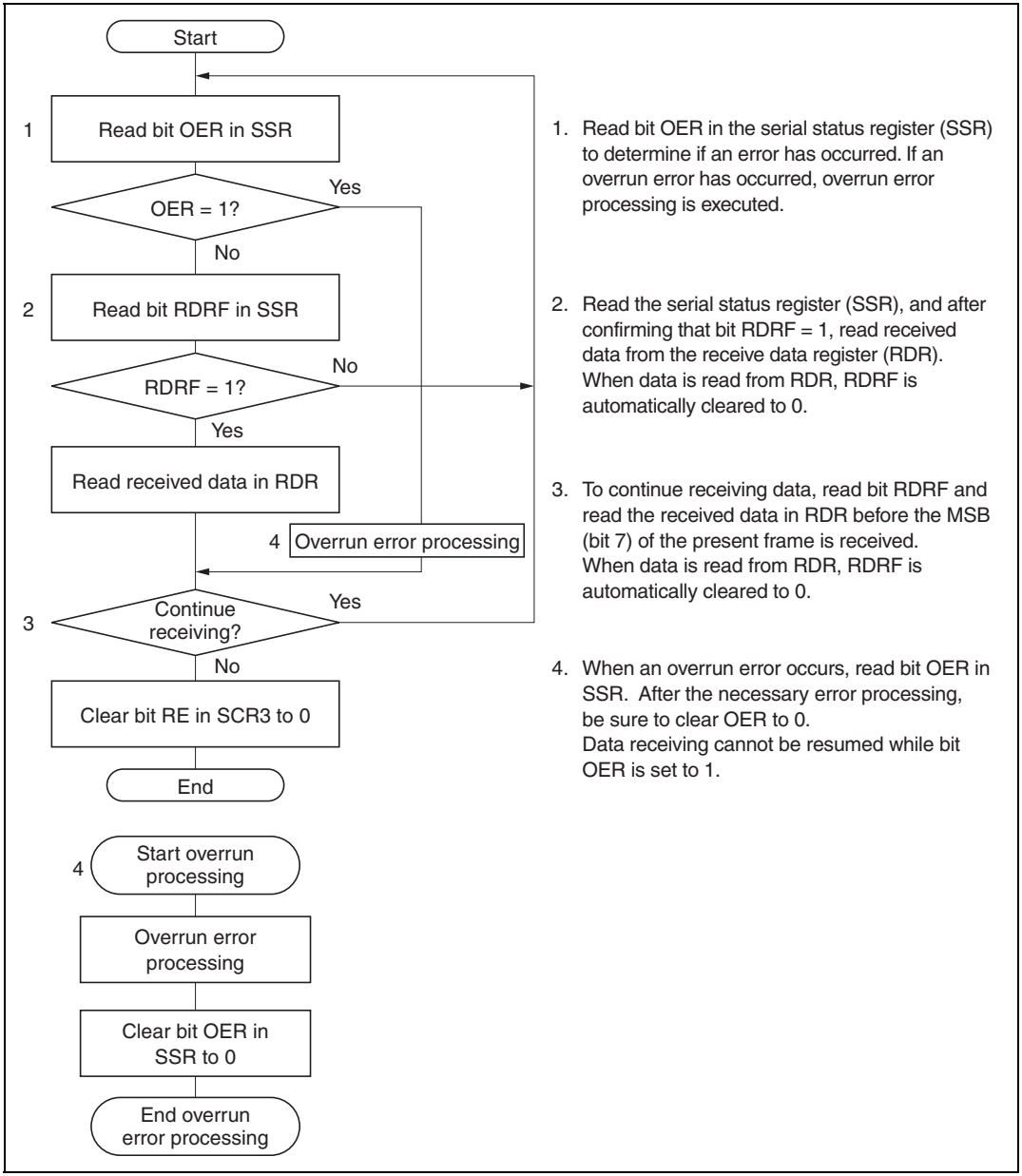


Figure 10.17 Typical Data Receiving Flow Chart in Synchronous Mode

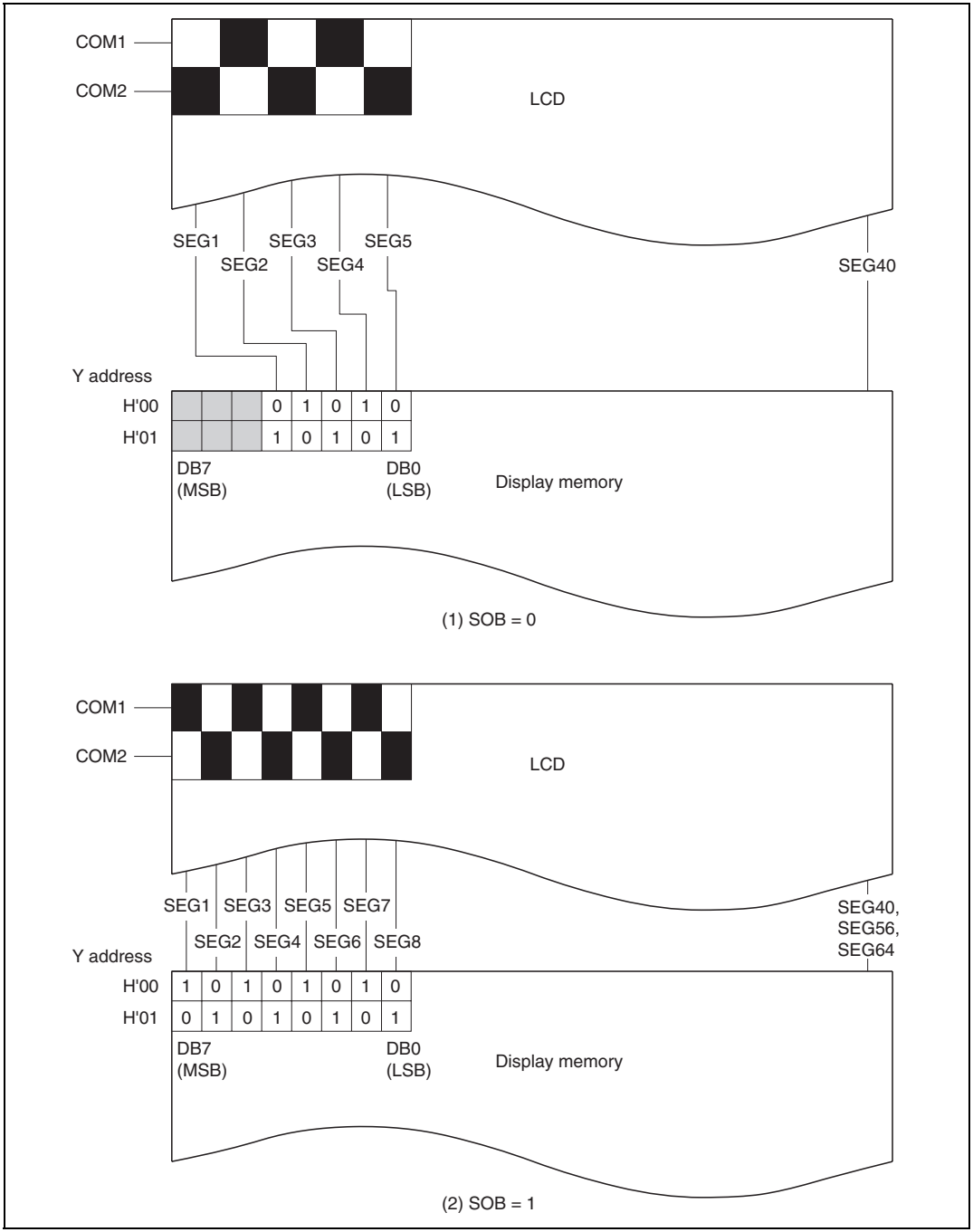


Figure 13.4 Memory Data and Display

Reading for Display

The LCD controller's display RAM is of the dual-port type, with accesses from the CPU and reads for LCD display independent of each other. This allows flexible interfacing.

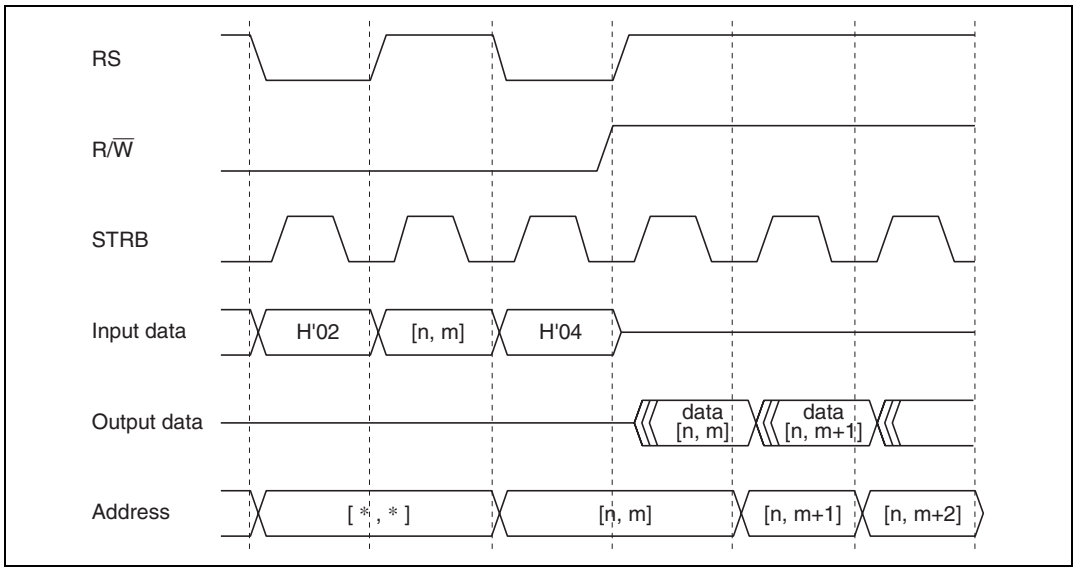
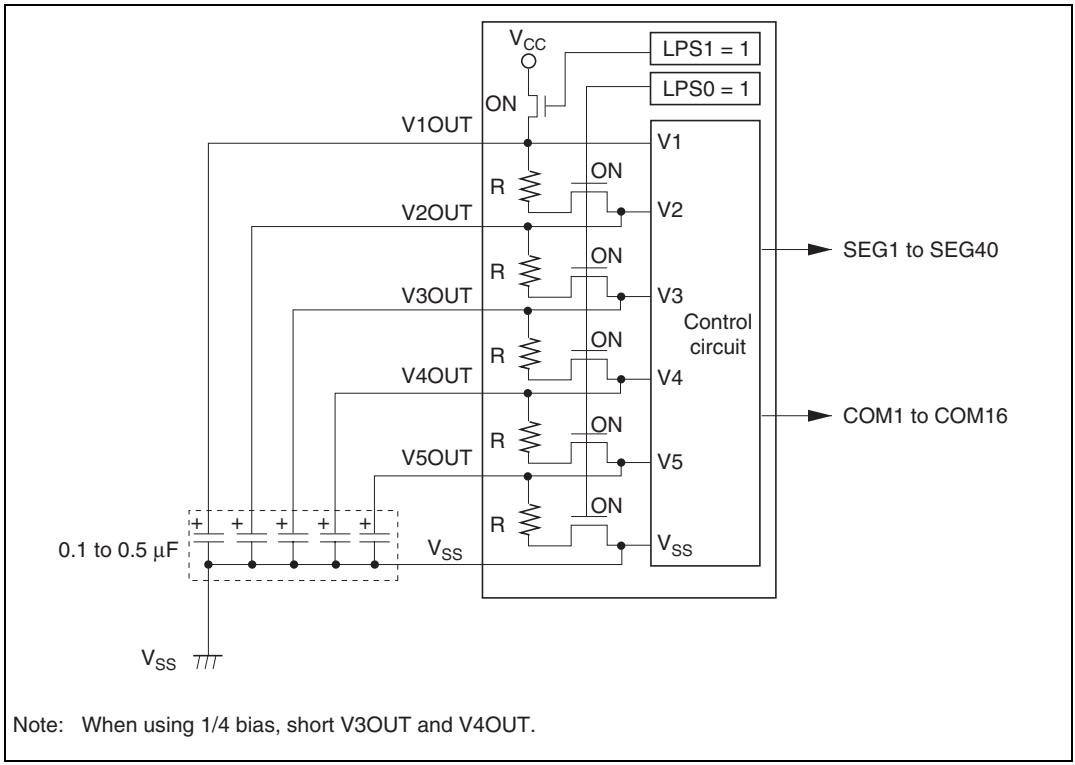


Figure 13.7 Memory Read Procedure

14.3.11 LCD Voltage Generation Circuit

When Using Internal Power Supply and Built-In Bleeder Resistances

The LCD controller includes bleeder resistances that generate levels V1 to V5. For the LCD drive power supply, drive can be performed using the internal power supply and V_{CC}, or using an external supply. When the internal power supply is used, and the built-in bleeder resistances are employed, bits LPS1 and LPS0 in control register 2 (LR1) should both be set to 1. If the capacitance of the LCD panel to be driven is large, capacitors of around 0.1 to 0.5 µF should be inserted between V1OUT to V5OUT and V_{SS} to provide stabilization.



Note: When using 1/4 bias, short V3OUT and V4OUT.

Figure 14.12 When Using Internal Power Supply and Built-In Bleeder Resistances (1/5 Bias)

Table 16.3 DC Characteristics of H8/3852, H8/3853, and H8/3854 (2)

V_{CC} = 2.7 V to 5.5 V of the mask ROM version of H8/3852, H8/3853, and H8/3854, V_{CC} = 3.0 V to 5.5 V of H8/3854F, V_{SS} = 0.0 V, T_a = –20°C to +75°C*[2], including subactive mode, unless otherwise specified.

Item	Symbol	Applicable Pins	Test Conditions	Values Min	Typ	Max	Unit	Notes
Allowable output low current (per pin)	I_{OL}	Output pins except in port 2	V_{CC} = 4.0 V to 5.5 V	—	—	2.0	mA	*[1]
		Port 2	V_{CC} = 4.0 V to 5.5 V	—	—	10.0		
		All output pins		—	—	0.5		
Allowable output low current (total)	ΣI_{OL}	Output pins except in port 2	V_{CC} = 4.0 V to 5.5 V	—	—	20.0	mA	*[1]
		Port 2	V_{CC} = 4.0 V to 5.5 V	—	—	80.0		
		All output pins		—	—	20.0		
Allowable output high current (per pin)	$-I_{OH}$	All output pins	V_{CC} = 4.0 V to 5.5 V	—	—	2.0	mA	*[1]
				—	—	0.2		
Allowable output high current (total)	$\Sigma-I_{OH}$	All output pins	V_{CC} = 4.0 V to 5.5 V	—	—	10.0	mA	*[1]
				—	—	8.0		

Notes: 1. Excludes LCD output pins.
2. The guaranteed temperature as an electrical characteristic for die type products is 75°C.

16.5 Usage Note

Although both the F-ZTAT and mask ROM versions fully meet the electrical specifications listed in this manual, there may be differences in the actual values of the electrical characteristics, operating margins, noise margins, and so forth, due to differences in the fabrication process, the on-chip ROM, and the layout patterns.

If the F-ZTAT version is used to carry out system evaluation and testing, therefore, when switching to the mask ROM version the same evaluation and testing procedures should also be conducted on the mask ROM version.

Mnemonic	Operand Size	Operation	Addressing Mode/ Instruction Length (Bytes)									Condition Code						No. of States
			#xx: 8/16	Rn	@Rn	@(d:16, Rn)	@–Rn/@Rn+	@aa: 8/16	@(d:8, PC)	@@aa	Implied	I	H	N	Z	V	C	
BSET #xx:3, Rd	B	(#xx:3 of Rd8) ← 1		2								—	—	—	—	—	—	2
BSET #xx:3, @Rd	B	(#xx:3 of @Rd16) ← 1			4							—	—	—	—	—	—	8
BSET #xx:3, @aa:8	B	(#xx:3 of @aa:8) ← 1						4				—	—	—	—	—	—	8
BSET Rn, Rd	B	(Rn8 of Rd8) ← 1		2								—	—	—	—	—	—	2
BSET Rn, @Rd	B	(Rn8 of @Rd16) ← 1			4							—	—	—	—	—	—	8
BSET Rn, @aa:8	B	(Rn8 of @aa:8) ← 1						4				—	—	—	—	—	—	8
BCLR #xx:3, Rd	B	(#xx:3 of Rd8) ← 0		2								—	—	—	—	—	—	2
BCLR #xx:3, @Rd	B	(#xx:3 of @Rd16) ← 0			4							—	—	—	—	—	—	8
BCLR #xx:3, @aa:8	B	(#xx:3 of @aa:8) ← 0						4				—	—	—	—	—	—	8
BCLR Rn, Rd	B	(Rn8 of Rd8) ← 0		2								—	—	—	—	—	—	2
BCLR Rn, @Rd	B	(Rn8 of @Rd16) ← 0			4							—	—	—	—	—	—	8
BCLR Rn, @aa:8	B	(Rn8 of @aa:8) ← 0						4				—	—	—	—	—	—	8
BNOT #xx:3, Rd	B	(#xx:3 of Rd8) ← (#xx:3 of $\overline{\text{Rd8}}$)		2								—	—	—	—	—	—	2
BNOT #xx:3, @Rd	B	(#xx:3 of @Rd16) ← (#xx:3 of $\overline{\text{@Rd16}}$)			4							—	—	—	—	—	—	8
BNOT #xx:3, @aa:8	B	(#xx:3 of @aa:8) ← (#xx:3 of $\overline{\text{@aa:8}}$)						4				—	—	—	—	—	—	8
BNOT Rn, Rd	B	(Rn8 of Rd8) ← ($\overline{\text{Rn8}}$ of $\overline{\text{Rd8}}$)		2								—	—	—	—	—	—	2
BNOT Rn, @Rd	B	(Rn8 of @Rd16) ← ($\overline{\text{Rn8}}$ of $\overline{\text{@Rd16}}$)			4							—	—	—	—	—	—	8
BNOT Rn, @aa:8	B	(Rn8 of @aa:8) ← ($\overline{\text{Rn8}}$ of $\overline{\text{@aa:8}}$)						4				—	—	—	—	—	—	8
BTST #xx:3, Rd	B	($\overline{\text{#xx:3 of Rd8}}$) → Z		2								—	—	—	↕	—	—	2
BTST #xx:3, @Rd	B	($\overline{\text{#xx:3 of @Rd16}}$) → Z			4							—	—	—	↕	—	—	6
BTST #xx:3, @aa:8	B	($\overline{\text{#xx:3 of @aa:8}}$) → Z						4				—	—	—	↕	—	—	6
BTST Rn, Rd	B	($\overline{\text{Rn8 of Rd8}}$) → Z		2								—	—	—	↕	—	—	2
BTST Rn, @Rd	B	($\overline{\text{Rn8 of @Rd16}}$) → Z			4							—	—	—	↕	—	—	6
BTST Rn, @aa:8	B	($\overline{\text{Rn8 of @aa:8}}$) → Z						4				—	—	—	↕	—	—	6

SCR1—Serial control register 1 **H'A0** **SCI1**
(H8/3857 Group only)

Bit	7	6	5	4	3	2	1	0
	SNC1	SNC0	—	—	CKS3	CKS2	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock Select (CKS2 to CKS0)

Bit 2	Bit 1	Bit 0	Prescaler Division	Serial Clock Cycle Synchronous	
CKS2	CKS1	CKS0		ϕ = 5 MHz	ϕ = 2.5 MHz
0	0	0	ϕ/1024	204.8 µs	409.6 µs
		1	ϕ/256	51.2 µs	102.4 µs
	1	0	ϕ/64	12.8 µs	25.6 µs
		1	ϕ/32	6.4 µs	12.8 µs
1	0	0	ϕ/16	3.2 µs	6.4 µs
		1	ϕ/8	1.6 µs	3.2 µs
	1	0	ϕ/4	0.8 µs	1.6 µs
		1	ϕ/2	—	0.8 µs

Clock source select

0	Clock source is prescaler S, and pin SCK_1 is output pin
1	Clock source is external clock, and pin SCK_1 is input pin

Operation mode select

0	0	8-bit synchronous transfer mode
	1	16-bit synchronous transfer mode
1	0	Continuous clock output mode
	1	Reserved

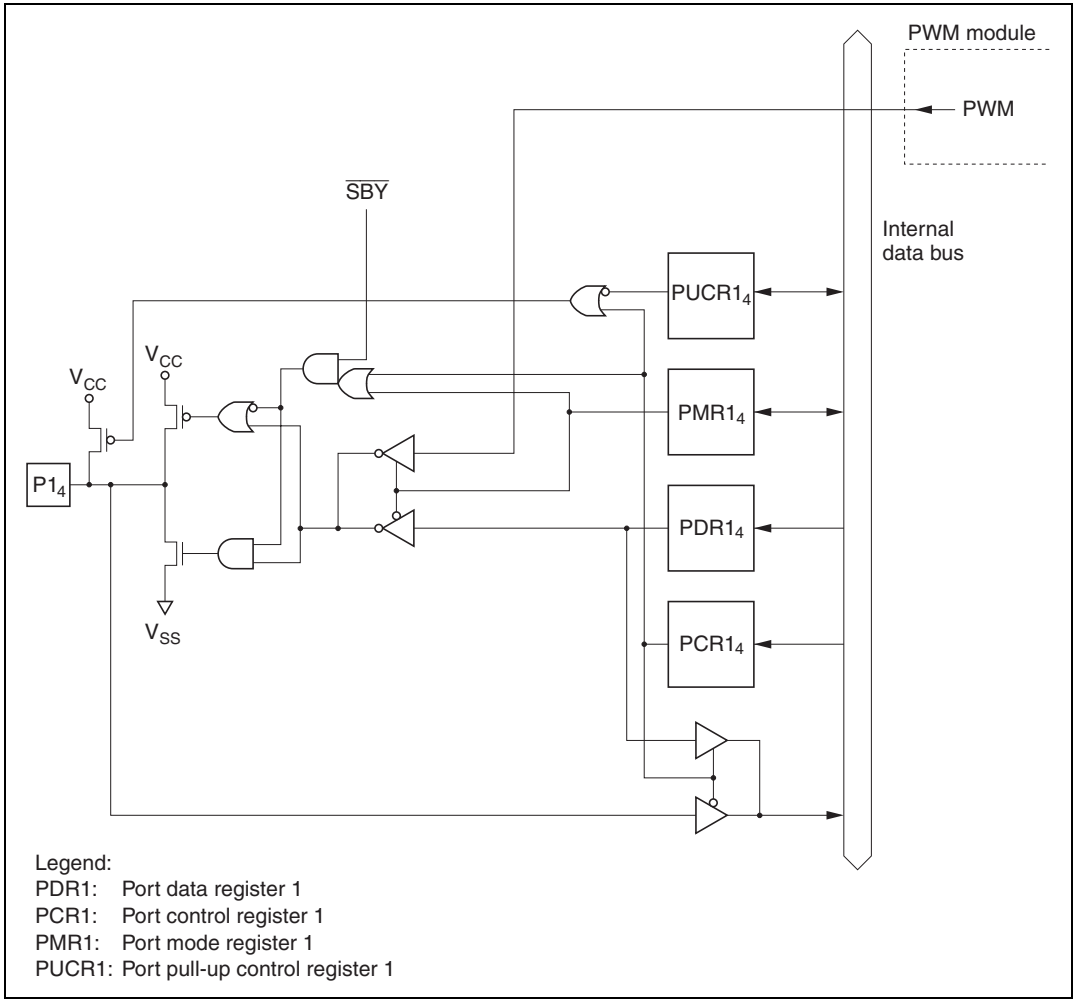


Figure C.1 (b) Port 1 Block Diagram (Pin $P1_4$: Function of H8/3857 Group Only)