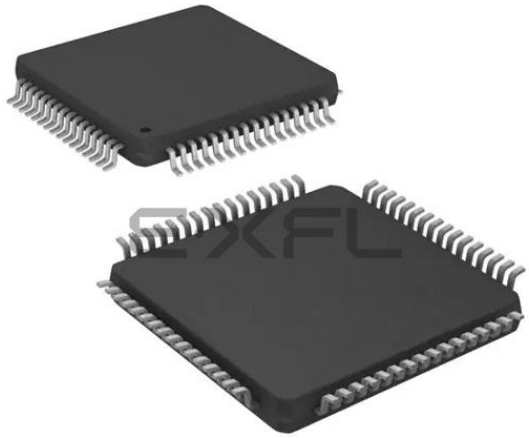
Microchip Technology - PIC18F65J50T-I/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	49
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f65j50t-i-pt

TABLE 1-4: PIC18F8XJ5X PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	80-TQFP			
				PORTE is a bidirectional I/O port (continued).
RE6/AD14/PMA10/P1B	74			
RE6		I/O	ST	Digital I/O.
AD14		I/O	TTL	External memory address/data 14.
PMA10		O	—	Parallel Master Port address.
P1B(3)		O	—	ECCP1 PWM output B.
RE7/AD15/PMA9/ ECCP2/P2A	73			
RE7		I/O	ST	Digital I/O.
AD15		I/O	TTL	External memory address/data 15.
PMA9		O	—	Parallel Master Port address.
ECCP2(4)		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
P2A(4)		O	—	ECCP2 PWM output A.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD})

Note 1: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared (Extended Microcontroller mode).

2: Default assignment for ECCP2/P2A for all devices in all operating modes (CCP2MX is set).

3: Default assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is set).

4: Alternate assignment for ECCP2/P2A when CCP2MX is cleared (Microcontroller mode).

5: Alternate assignments for P1B/P1C/P3B/P3C (ECCPMX Configuration bit is cleared).

6: Pin placement when PMPMX = 1.

7: Pin placement when PMPMX = 0.

8: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 4-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset RESET Instruction Stack Resets CM Resets	Wake-up via WDT or Interrupt
ADRESH	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADRESL	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
ADCON1	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
ANCON0	Feature1	PIC18F8XJ5X	0--0 0000	u--u uuuu	u--u uuuu
ANCON1	Feature1	PIC18F8XJ5X	0000 00--	uuuu uu--	uuuu uu--
WDTCON	Feature1	PIC18F8XJ5X	0x-0 ---0	0x-u ---0	ux-u ---u
ECCP1AS	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
ECCP1DEL	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
CCPR1H	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1L	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
ECCP2AS	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
ECCP2DEL	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
CCPR2H	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR2L	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP2CON	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
ECCP3AS	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
ECCP3DEL	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
CCPR3H	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR3L	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP3CON	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
SPBRG1	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
RCREG1	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
TXREG1	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
TXSTA1	Feature1	PIC18F8XJ5X	0000 0010	0000 0010	uuuu uuuu
RCSTA1	Feature1	PIC18F8XJ5X	0000 000x	0000 000x	uuuu uuuu
SPBRG2	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
RCREG2	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
TXREG2	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
TXSTA2	Feature1	PIC18F8XJ5X	0000 0010	0000 0010	uuuu uuuu
EECON2	Feature1	PIC18F8XJ5X	---- ----	---- ----	---- ----
EECON1	Feature1	PIC18F8XJ5X	--00 x00-	--00 u00-	--00 u00-

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 4-1 for Reset value for specific condition.

TABLE 4-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets WDT Reset RESET Instruction Stack Resets CM Resets	Wake-up via WDT or Interrupt
PMCONL	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
PMMODEH	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
PMMODEL	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
PMDOUT2H	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
PMDOUT2L	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
PMDIN2H	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
PMDIN2L	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
PMEH	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
PMEL	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
PMSTATH	Feature1	PIC18F8XJ5X	00-- 0000	00-- 0000	uu-- uuuu
PMSTATL	Feature1	PIC18F8XJ5X	10-- 1111	10-- 1111	uu-- uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 4-1 for Reset value for specific condition.

10.5 PORTD, TRISD and LATD Registers

PORTD is an 8-bit wide, bidirectional port. All pins on PORTD are digital only and tolerate voltages up to 5.5V.

All pins on PORTD are implemented with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

Note:	These pins are configured as digital inputs on any device Reset.

On 80-pin devices, PORTD is multiplexed with the system bus as part of the external memory interface. I/O port and other functions are only available when the interface is disabled by setting the EBDIS bit (MEMCON<7>). When the interface is enabled, PORTD is the low-order byte of the multiplexed address/data bus (AD7:AD0). The TRISD bits are also overridden.

PORTD can also be configured to function as an 8-bit wide Parallel Master Port data. In this mode, Parallel Master Port takes priority over the other digital I/O (but not the external memory interface). This multiplexing is available when PMPMX = 1. When the Parallel Master Port is active, the input buffers are TTL. For more information, refer to **Section 11.0 "Parallel Master Port"**

Each of the PORTD pins has a weak internal pull-up. The pull-ups are provided to keep the inputs at a known state for the external memory interface while powering up. A single control bit can turn off all the pull-ups. This is performed by clearing bit, RDPU (PORTG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on all device Resets.

EXAMPLE 10-4: INITIALIZING PORTD

```
CLRF    PORTD   ; Initialize PORTD by
                ; clearing output
                ; data latches
CLRF    LATD    ; Alternate method to clear
                ; output data latches
MOVLW   0CFh    ; Value used to initialize
                ; data direction
MOVWF   TRISD   ; Set RD<3:0> as inputs
                ; RD<5:4> as outputs
                ; RD<7:6> as inputs
```

TABLE 10-12: PORTE FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RE0/AD8/ PMRD/P2D	RE0	0	O	DIG	LATE<0> data output.
		1	I	ST	PORTE<0> data input.
	AD8(3)	x	O	DIG	External memory interface, address/data bit 8 output.(2)
		x	I	TTL	External memory interface, data bit 8 input.(2)
	PMRD(5)	x	O	DIG	Parallel Master Port read strobe pin.
		x	I	TTL	Parallel Master Port read pin.
	P2D	0	O	DIG	ECCP2 Enhanced PWM output, channel D; takes priority over port and PMP data. May be configured for tri-state during Enhanced PWM shutdown events.
RE1/AD9/ PMWR/P2C	RE1	0	O	DIG	LATE<1> data output.
		1	I	ST	PORTE<1> data input.
	AD9(3)	x	O	DIG	External memory interface, address/data bit 9 output.(2)
		x	I	TTL	External memory interface, data bit 9 input.(2)
	PMWR(5)	x	O	DIG	Parallel Master Port write strobe pin.
		x	I	TTL	Parallel Master Port write pin.
	P2C	0	O	DIG	ECCP2 Enhanced PWM output, channel C; takes priority over port and PMP data. May be configured for tri-state during Enhanced PWM shutdown events.
RE2/AD10/ PMBE/P2B	RE2	0	O	DIG	LATE<2> data output.
		1	I	ST	PORTE<2> data input.
	AD10(3)	x	O	DIG	External memory interface, address/data bit 10 output.(2)
		x	I	TTL	External memory interface, data bit 10 input.(2)
	PMBE(5)	x	O	DIG	Parallel Master Port byte enable.
	P2B	0	O	DIG	ECCP2 Enhanced PWM output, channel B; takes priority over port and PMP data. May be configured for tri-state during Enhanced PWM shutdown events.
RE3/AD11/ PMA13/P3C/ REFO	RE3	0	O	DIG	LATE<3> data output.
		1	I	ST	PORTE<3> data input.
	AD11(3)	x	O	DIG	External memory interface, address/data bit 11 output.(2)
		x	I	TTL	External memory interface, data bit 11 input.(2)
	PMA13	x	O	DIG	Parallel Master Port address.
	P3C(1)	0	O	DIG	ECCP3 Enhanced PWM output, channel C; takes priority over port and PMP data. May be configured for tri-state during Enhanced PWM shutdown events.
	REFO	x	O	DIG	Reference output clock.
RE4/AD12/ PMA12/P3B	RE4	0	O	DIG	LATE<4> data output.
		1	I	ST	PORTE<4> data input.
	AD12(3)	x	O	DIG	External memory interface, address/data bit 12 output.(2)
		x	I	TTL	External memory interface, data bit 12 input.(2)
	PMA12	x	O	DIG	Parallel Master Port address.
	P3B(1)	0	O	DIG	ECCP3 Enhanced PWM output, channel B; takes priority over port and PMP data. May be configured for tri-state during Enhanced PWM shutdown events.

Legend: O = Output, I = Input, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

Note 1: Default assignments for P1B/P1C and P3B/P3C when ECCPMX Configuration bit is set (80-pin devices only).

2: External memory interface I/O takes priority over all other digital and PMP I/O.

3: Available on 80-pin devices only.

4: Alternate assignment for ECCP2/P2A when ECCP2MX Configuration bit is cleared (all devices in Microcontroller mode).

5: Default configuration for PMP (PMPMX Configuration bit = 1).

TABLE 10-14: PORTF FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RF2/PMA5/ AN7/C2INB	RF2	0	O	DIG	LATF<2> data output; not affected by analog input.
		1	I	ST	PORTF<2> data input; disabled when analog input enabled.
	PMA5	x	O	DIG	Parallel Master Port address.
	AN7	1	I	ANA	A/D input channel 7. Default configuration on POR.
	C2INB	x	I	ANA	Comparator 2 input B.
RF3/D-	RF3	1	I	ST	PORTF<3> data input; disabled when analog input enabled.
	D-		O	XVCR	USB bus differential minus line output (internal transceiver).
			I	XVCR	USB bus differential minus line input (internal transceiver).
RF4/D+	RF4	1	I	ST	PORTF<4> data input; disabled when analog input enabled.
	D+		O	XVCR	USB bus differential plus line output (internal transceiver).
			I	XVCR	USB bus differential plus line input (internal transceiver).
RF5/PMD2/ AN10/C1INB/ CVREF	RF5	0	O	DIG	LATF<5> data output; not affected by analog input. Disabled when CVREF output enabled.
		1	I	ST	PORTF<5> data input; disabled when analog input enabled. Disabled when CVREF output enabled.
	PMD2(1)	x	O	DIG	Parallel Master Port data out.
		x	I	TTL	Parallel Master Port data input.
	AN10	1	I	ANA	A/D input channel 10 and Comparator C1+ input. Default input configuration on POR.
	C1INB	x	I	ANA	Comparator 1 input B.
	CVREF	x	O	ANA	Comparator voltage reference output. Enabling this feature disables digital I/O.
RF6/PMD1/ AN11/C1INA	RF6	0	O	DIG	LATF<6> data output; not affected by analog input.
		1	I	ST	PORTF<6> data input; disabled when analog input enabled.
	PMD1(1)	x	O	DIG	Parallel Master Port data out.
		x	I	TTL	Parallel Master Port data input.
	AN11	1	I	ANA	A/D input channel 11 and Comparator C1- input. Default input configuration on POR; does not affect digital output.
	C1INA	x	I	ANA	Comparator 1 input A.
RF7/PMD0/ $\overline{SS1}$/C1OUT	RF7	0	O	DIG	LATF<7> data output.
		1	I	ST	PORTF<7> data input.
	PMD0(1)	x	O	DIG	Parallel Master Port data out.
		x	I	TTL	Parallel Master Port data input.
	$\overline{SS1}$	1	I	TTL	Slave select input for MSSP1.
	C1OUT	x	O	DIG	Comparator 1 output.

Legend: O = Output, I = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input, XVCR = USB Transceiver, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

Note 1: Alternate PMP configuration when the PMPMX Configuration bit = 0; available on 80-pin devices only.

12.0 TIMER0 MODULE

The Timer0 module incorporates the following features:

- Software selectable operation as a timer or counter in both 8-bit or 16-bit modes
- Readable and writable registers
- Dedicated 8-bit, software programmable prescaler
- Selectable clock source (internal or external)
- Edge select for external clock
- Interrupt-on-overflow

The T0CON register (Register 12-1) controls all aspects of the module's operation, including the prescale selection. It is both readable and writable.

A simplified block diagram of the Timer0 module in 8-bit mode is shown in Figure 12-1. Figure 12-2 shows a simplified block diagram of the Timer0 module in 16-bit mode.

REGISTER 12-1: T0CON: TIMER0 CONTROL REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TMR0ON:** Timer0 On/Off Control bit
1 = Enables Timer0
0 = Stops Timer0

bit 6 **T08BIT**: Timer0 8-Bit/16-Bit Control bit
1 = Timer0 is configured as an 8-bit timer/counter
0 = Timer0 is configured as a 16-bit timer/counter

bit 5 **T0CS**: Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKO)

bit 4 **T0SE**: Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA**: Timer0 Prescaler Assignment bit
1 = TImer0 prescaler is not assigned. Timer0 clock input bypasses prescaler.
0 = Timer0 prescaler is assigned. Timer0 clock input comes from prescaler output.

bit 2-0 **T0PS2:T0PS0**: Timer0 Prescaler Select bits
111 = 1:256 Prescale value
110 = 1:128 Prescale value
101 = 1:64 Prescale value
100 = 1:32 Prescale value
011 = 1:16 Prescale value
010 = 1:8 Prescale value
001 = 1:4 Prescale value
000 = 1:2 Prescale value

15.0 TIMER3 MODULE

The Timer3 timer/counter module incorporates these features:

- Software selectable operation as a 16-bit timer or counter
- Readable and writable 8-bit registers (TMR3H and TMR3L)
- Selectable clock source (internal or external) with device clock or Timer1 oscillator internal options
- Interrupt-on-overflow
- Module Reset on ECCP Special Event Trigger

A simplified block diagram of the Timer3 module is shown in Figure 15-1. A block diagram of the module's operation in Read/Write mode is shown in Figure 15-2.

The Timer3 module is controlled through the T3CON register (Register 15-1). It also selects the clock source options for the CCP and ECCP modules; see **Section 17.1.1 "CCP Modules and Timer Resources"** for more information.

REGISTER 15-1: T3CON: TIMER3 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	$\overline{\text{T3SYNC}}$	TMR3CS	TMR3ON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **RD16:** 16-Bit Read/Write Mode Enable bit
1 = Enables register read/write of Timer3 in one 16-bit operation
0 = Enables register read/write of Timer3 in two 8-bit operations

bit 6,3 **T3CCP2:T3CCP1:** Timer3 and Timer1 to ECCPx/CCPx Enable bits
11 = Timer3 and Timer4 are the clock sources for all ECCP/CCP modules
10 = Timer3 and Timer4 are the clock sources for ECCP3, CCP4 and CCP5;
Timer1 and Timer2 are the clock sources for ECCP1 and ECCP2
01 = Timer3 and Timer4 are the clock sources for ECCP2, ECCP3, CCP4 and CCP5;
Timer1 and Timer2 are the clock sources for ECCP1
00 = Timer1 and Timer2 are the clock sources for all ECCP/CCP modules

bit 5-4 **T3CKPS1:T3CKPS0**: Timer3 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 2 **T3SYNC:** Timer3 External Clock Input Synchronization Control bit
(Not usable if the device clock comes from Timer1/Timer3.)
When TMR3CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
When TMR3CS = 0:
This bit is ignored. Timer3 uses the internal clock when TMR3CS = 0.

bit 1 **TMR3CS:** Timer3 Clock Source Select bit
1 = External clock input from Timer1 oscillator or T13CKI (on the rising edge after the first falling edge)
0 = Internal clock (FOSC/4)

bit 0 **TMR3ON:** Timer3 On bit
1 = Enables Timer3
0 = Stops Timer3

19.3.2 OPERATION

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits (SSPxCON1<5:0> and SSPxSTAT<7:6>). These control bits allow the following to be specified:

- Master mode (SCKx is the clock output)
- Slave mode (SCKx is the clock input)
- Clock Polarity (Idle state of SCKx)
- Data Input Sample Phase (middle or end of data output time)
- Clock Edge (output data on rising/falling edge of SCKx)
- Clock Rate (Master mode only)
- Slave Select mode (Slave mode only)

Each MSSP module consists of a transmit/receive shift register (SSPxSR) and a buffer register (SSPxBUF). The SSPxSR shifts the data in and out of the device, MSb first. The SSPxBUF holds the data that was written to the SSPxSR until the received data is ready. Once the 8 bits of data have been received, that byte is moved to the SSPxBUF register. Then, the Buffer Full detect bit, BF (SSPxSTAT<0>) and the interrupt flag bit, SSPxIF, are set. This double-buffering of the received data (SSPxBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPxBUF register during transmission/reception of data will be ignored and the Write Collision Detect bit, WCOL (SSPxCON1<7>), will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPxBUF register completed successfully.

When the application software is expecting to receive valid data, the SSPxBUF should be read before the next byte of data to transfer is written to the SSPxBUF. The Buffer Full bit, BF (SSPxSTAT<0>), indicates when SSPxBUF has been loaded with the received data (transmission is complete). When the SSPxBUF is read, the BF bit is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally, the MSSP interrupt is used to determine when the transmission/reception has completed. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur. Example 19-1 shows the loading of the SSPxBUF (SSPxSR) for data transmission.

The SSPxSR is not directly readable or writable and can only be accessed by addressing the SSPxBUF register. Additionally, the SSPxSTAT register indicates the various status conditions.

19.3.3 OPEN-DRAIN OUTPUT OPTION

The drivers for the SDOx output and SCKx clock pins can be optionally configured as open-drain outputs. This feature allows the voltage level on the pin to be pulled to a higher level through an external pull-up resistor, and allows the output to communicate with external circuits without the need for additional level shifters. For more information, see **Section 10.1.4 "Open-Drain Outputs"**.

The open-drain output option is controlled by the SPI2OD and SPI1OD bits (ODCON3<1:0>. Setting an SPIxOD bit configures both SDO and SCK pins for the corresponding open-drain operation.

The ODCON3 register shares the same address as the T1CON register. The ODCON3 register is accessed by setting the ADSHR bit in the WDTCON register (WDTCON<4>).

EXAMPLE 19-1: LOADING THE SSP1BUF (SSP1SR) REGISTER

```
LOOP    BTFSS   SSP1STAT, BF    ;Has data been received (transmit complete)?
        BRA     LOOP            ;No
        MOVF    SSP1BUF, W      ;WREG reg = contents of SSP1BUF
        MOVWF   RXDATA          ;Save in user RAM, if data is meaningful
        MOVF    TXDATA, W       ;W reg = contents of TXDATA
        MOVWF   SSP1BUF         ;New data to xmit
```

FIGURE 19-5: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 0)

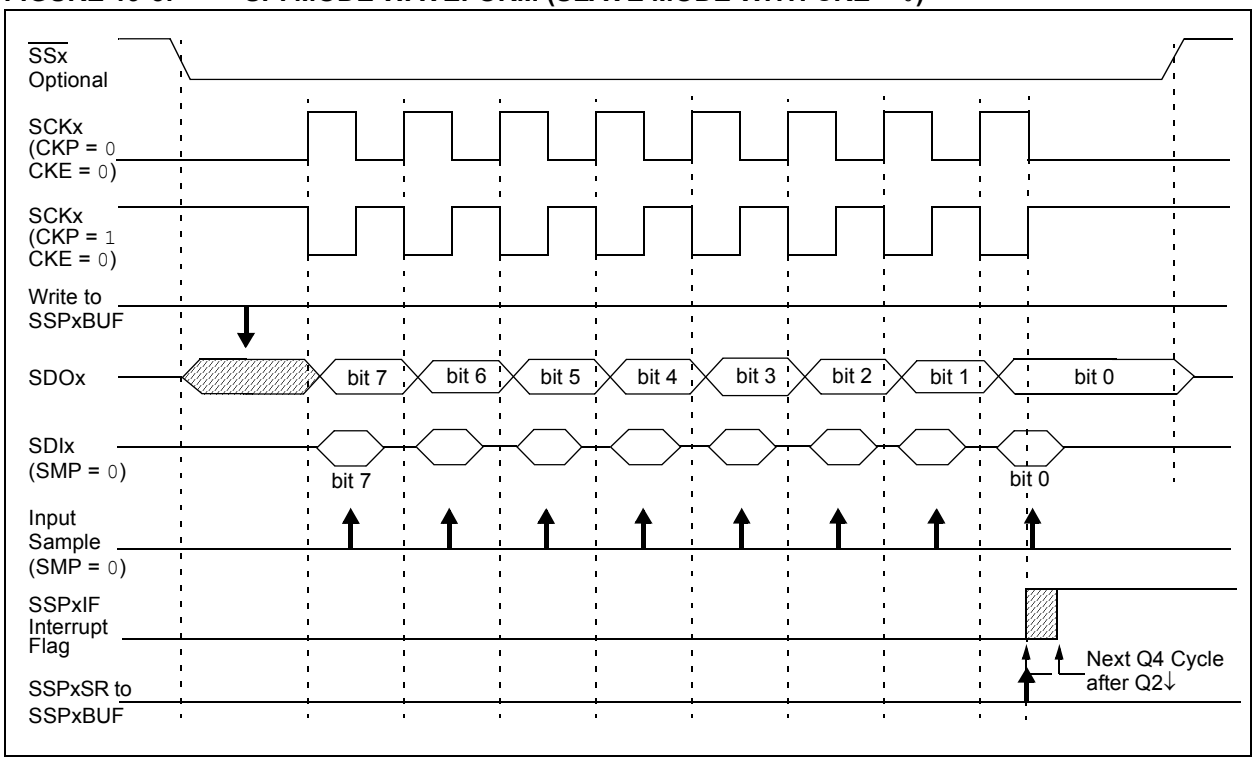
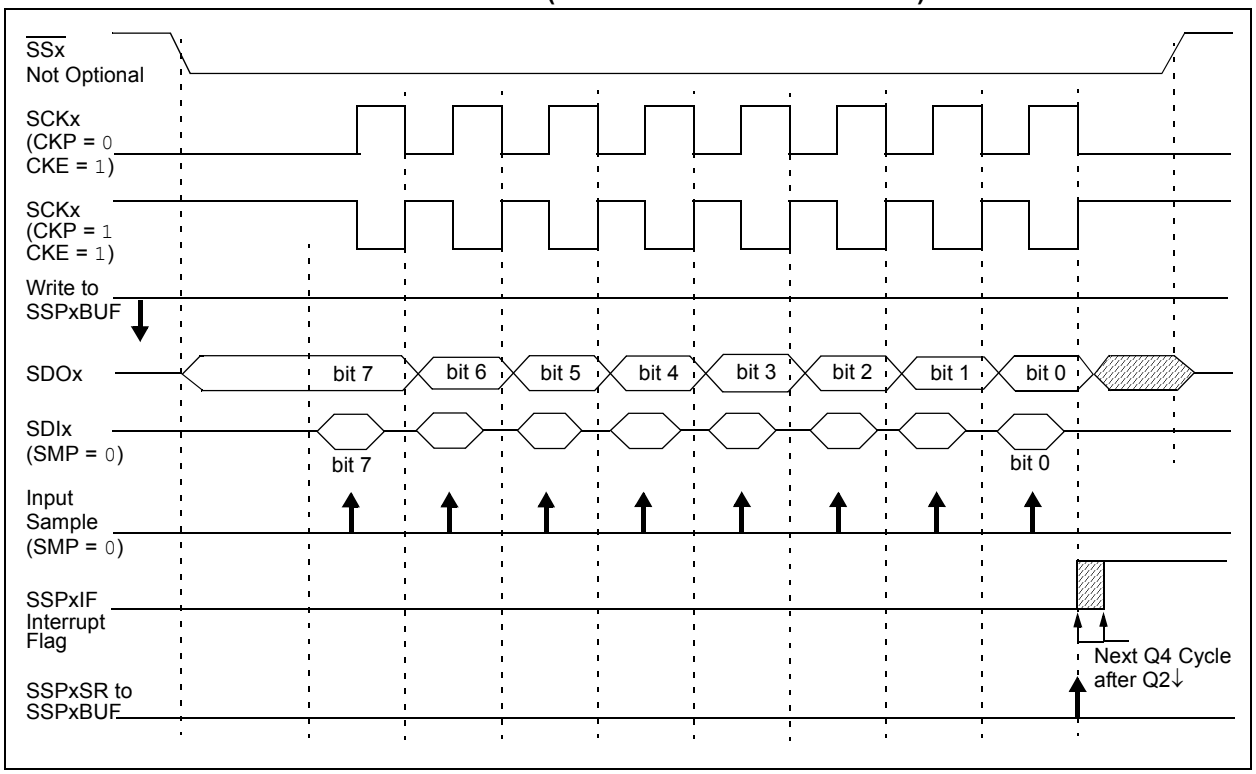


FIGURE 19-6: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)



REGISTER 19-4: SSPxCON1: MSSPx CONTROL REGISTER 1 (I²C™ MODE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN(1)	CKP	SSPM3(2)	SSPM2(2)	SSPM1(2)	SSPM0(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **WCOL:** Write Collision Detect bit

In Master Transmit mode:
1 = A write to the SSPxBUF register was attempted while the I²C conditions were not valid for a transmission to be started (must be cleared in software)
0 = No collision

In Slave Transmit mode:
1 = The SSPxBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision

In Receive mode (Master or Slave modes):
This is a "don't care" bit.

bit 6 **SSPOV:** Receive Overflow Indicator bit

In Receive mode:
1 = A byte is received while the SSPxBUF register is still holding the previous byte (must be cleared in software)
0 = No overflow

In Transmit mode:
This is a "don't care" bit in Transmit mode.

bit 5 **SSPEN:** Master Synchronous Serial Port Enable bit(1)

1 = Enables the serial port and configures the SDAx and SCLx pins as the serial port pins
0 = Disables serial port and configures these pins as I/O port pins

bit 4 **CKP:** SCKx Release Control bit

In Slave mode:
1 = Releases clock
0 = Holds clock low (clock stretch), used to ensure data setup time

In Master mode:
Unused in this mode.

bit 3-0 **SSPM3:SSPM0:** Master Synchronous Serial Port Mode Select bits(2)

1111 = I²C Slave mode, 10-bit address with Start and Stop bit interrupts enabled
1110 = I²C Slave mode, 7-bit address with Start and Stop bit interrupts enabled
1011 = I²C Firmware Controlled Master mode (Slave Idle)
1001 = Load SSPMSK register at SSPADD SFR address(3,4)
1000 = I²C Master mode, clock = FOSC/(4 * (SSPxADD + 1))
0111 = I²C Slave mode, 10-bit address
0110 = I²C Slave mode, 7-bit address

Note 1: When enabled, the SDAx and SCLx pins must be configured as inputs.
2: Bit combinations not specifically listed here are either reserved or implemented in SPI mode only.
3: When SSPM3:SSPM0 = 1001, any reads or writes to the SSPxADD SFR address actually accesses the SSPMSK register.
4: This mode is only available when 7-bit Address Masking mode is selected (MSSPMSK Configuration bit is '1').

22.2.5 USB ADDRESS REGISTER (UADDR)

The USB Address register contains the unique USB address that the peripheral will decode when active. UADDR is reset to 00h when a USB Reset is received, indicated by URSTIF, or when a Reset is received from the microcontroller. The USB address must be written by the microcontroller during the USB setup phase (enumeration) as part of the Microchip USB firmware support.

22.2.6 USB FRAME NUMBER REGISTERS (UFRMH:UFRML)

The Frame Number registers contain the 11-bit frame number. The low-order byte is contained in UFRML, while the three high-order bits are contained in UFRMH. The register pair is updated with the current frame number whenever a SOF token is received. For the microcontroller, these registers are read-only. The Frame Number registers are primarily used for isochronous transfers. The contents of the UFRMH and UFRML registers are only valid when the 48 MHz SIE clock is active (i.e., contents are inaccurate when SUSPND (UCON<1>) bit = 1).

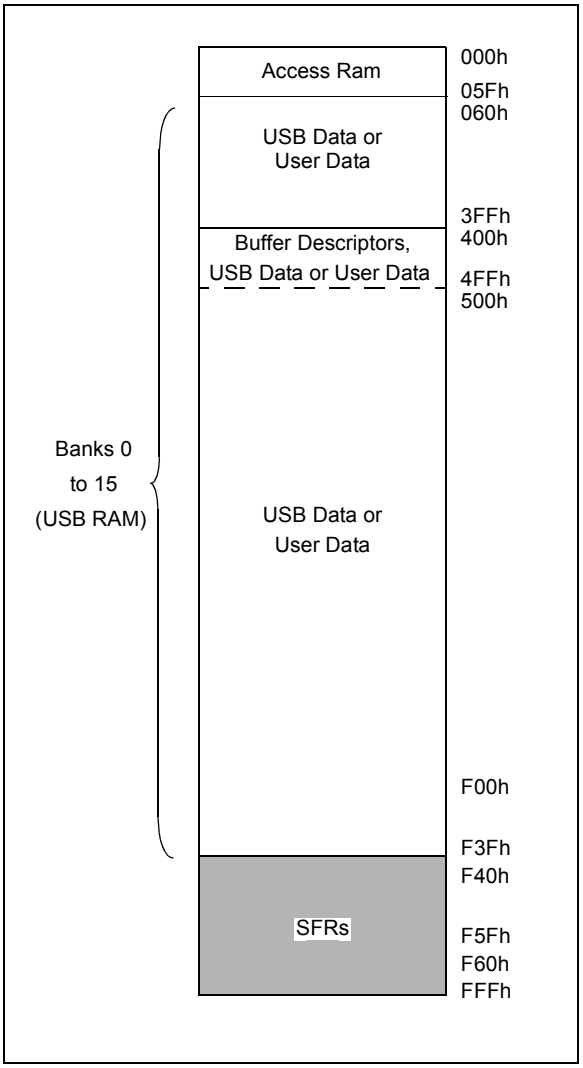
22.3 USB RAM

USB data moves between the microcontroller core and the SIE through a memory space known as the USB RAM. This is a special dual access memory that is mapped into the normal data memory space in Banks 0 through 15 (60h to F3Fh) for a total of 3.9 Kbyte (Figure 22-4).

Bank 4 (400h through 4FFh) is used specifically for endpoint buffer control, while Banks 0 through Bank3 and Banks 5 through Bank15 are available for USB data. Depending on the type of buffering being used, all but 8 bytes of Bank 4 may also be available for use as USB buffer space.

Although USB RAM is available to the microcontroller as data memory, the sections that are being accessed by the SIE should not be accessed by the microcontroller. A semaphore mechanism is used to determine the access to a particular buffer at any given time. This is discussed in **Section 22.4.1.1 "Buffer Ownership"**.

FIGURE 22-4: IMPLEMENTATION OF USB RAM IN DATA MEMORY SPACE



22.4.1.3 BDnSTAT Register (SIE Mode)

When the BD and its buffer are owned by the SIE, most of the bits in BDnSTAT take on a different meaning. The configuration is shown in Register 22-6. Once UOWN is set, any data or control settings previously written there by the user will be overwritten with data from the SIE.

The BDnSTAT register is updated by the SIE with the token Packet Identifier (PID) which is stored in BDnSTAT<5:3>. The transfer count in the corresponding BDnCNT register is updated. Values that overflow the 8-bit register carry over to the two most significant digits of the count, stored in BDnSTAT<1:0>.

22.4.2 BD BYTE COUNT

The byte count represents the total number of bytes that will be transmitted during an IN transfer. After an IN transfer, the SIE will return the number of bytes sent to the host.

For an OUT transfer, the byte count represents the maximum number of bytes that can be received and stored in USB RAM. After an OUT transfer, the SIE will return the actual number of bytes received. If the number of bytes received exceeds the corresponding byte count, the data packet will be rejected and a NAK handshake will be generated. When this happens, the byte count will not be updated.

The 10-bit byte count is distributed over two registers. The lower 8 bits of the count reside in the BDnCNT register. The upper two bits reside in BDnSTAT<1:0>. This represents a valid byte range of 0 to 1023.

22.4.3 BD ADDRESS VALIDATION

The BD Address register pair contains the starting RAM address location for the corresponding endpoint buffer. No mechanism is available in hardware to validate the BD address.

If the value of the BD address does not point to an address in the USB RAM, or if it points to an address within another endpoint's buffer, data is likely to be lost or overwritten. Similarly, overlapping a receive buffer (OUT endpoint) with a BD location in use can yield unexpected results. When developing USB applications, the user may want to consider the inclusion of software-based address validation in their code.

REGISTER 22-6: BDnSTAT: BUFFER DESCRIPTOR n STATUS REGISTER (BD0STAT THROUGH BD63STAT), SIE MODE (DATA RETURNED BY THE SIDE TO THE MCU)

R/W-x	U-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
UOWN	—	PID3	PID2	PID1	PID0	BC9	BC8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **UOWN:** USB Own bit
1 = The SIE owns the BD and its corresponding buffer

bit 6 **Reserved:** Not written by the SIE

bit 5-2 **PID3:PID0:** Packet Identifier bits
The received token PID value of the last transfer (IN, OUT or SETUP transactions only).

bit 1-0 **BC9:BC8:** Byte Count 9 and 8 bits
These bits are updated by the SIE to reflect the actual number of bytes received on an OUT transfer and the actual number of bytes transmitted on an IN transfer.

REGISTER 25-1: CONFIG1L: CONFIGURATION REGISTER 1 LOW (BYTE ADDRESS 300000h)

R/WO-1	R/WO-1	R/WO-1	U-0	R/WO-1	R/WO-1	R/WO-1	R/WO-1
$\overline{\text{DEBUG}}$	XINST	STVREN	—	PLLDIV2	PLLDIV1	PLLDIV0	WDTEN
bit 7							bit 0

Legend:			
R = Readable bit	WO = Write-Once bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{DEBUG}}$:** Background Debugger Enable bit
1 = Background debugger disabled; RB6 and RB7 configured as general purpose I/O pins
0 = Background debugger enabled; RB6 and RB7 are dedicated to In-Circuit Debug

bit 6 **XINST:** Extended Instruction Set Enable bit
1 = Instruction set extension and Indexed Addressing mode enabled
0 = Instruction set extension and Indexed Addressing mode disabled (Legacy mode)

bit 5 **STVREN**: Stack Overflow/Underflow Reset Enable bit
1 = Reset on stack overflow/underflow enabled
0 = Reset on stack overflow/underflow disabled

bit 4 **Unimplemented:** Read as '0'

bit 3-1 **PLLDIV2:PLLDIV0:** Oscillator Selection bits
Divider must be selected to provide a 4 MHz input into the 96 MHz PLL
111 = No divide - oscillator used directly (4 MHz input)
110 = Oscillator divided by 2 (8 MHz input)
101 = Oscillator divided by 3 (12 MHz input)
100 = Oscillator divided by 4 (16 MHz input)
011 = Oscillator divided by 5 (20 MHz input)
010 = Oscillator divided by 6 (24 MHz input)
001 = Oscillator divided by 10 (40 MHz input)
000 = Oscillator divided by 12 (48 MHz input)

bit 0 **WDTEN:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled (control is placed on SWDTEN bit)

REGISTER 25-2: CONFIG1H: CONFIGURATION REGISTER 1 HIGH (BYTE ADDRESS 300001h)

U-1	U-1	U-1	U-1	U-0	R/WO-1	R/WO-1	R/WO-1
—	—	—	—	—	CP0	CPDIV1	CPDIV0
bit 7							bit 0

Legend:			
R = Readable bit	WO = Write-Once bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented:** Maintain as '1'

bit 3 **Unimplemented:** Read as '0'

bit 2 **CP0:** Code Protection bit
1 = Program memory is not code-protected
0 = Program memory is code-protected

bit 1-0 **CPDIV1:CPDIV0:** CPU System Clock Selection bits
11 = No CPU system clock divide
10 = CPU system clock divided by 2
01 = CPU system clock divided by 3
00 = CPU system clock divided by 6

26.0 INSTRUCTION SET SUMMARY

The PIC18F87J10 family of devices incorporate the standard set of 75 PIC18 core instructions, as well as an extended set of 8 new instructions for the optimization of code that is recursive or that utilizes a software stack. The extended set is discussed later in this section.

26.1 Standard Instruction Set

The standard PIC18 instruction set adds many enhancements to the previous PIC® instruction sets, while maintaining an easy migration from these PIC instruction sets. Most instructions are a single program memory word (16 bits), but there are four instructions that require two program memory locations.

Each single-word instruction is a 16-bit word divided into an opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into four basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal** operations
- **Control** operations

The PIC18 instruction set summary in Table 26-2 lists **byte-oriented**, **bit-oriented**, **literal** and **control** operations. Table 26-1 shows the opcode field descriptions.

Most **byte-oriented** instructions have three operands:

1. The file register (specified by ‘f’)
2. The destination of the result (specified by ‘d’)
3. The accessed memory (specified by ‘a’)

The file register designator, ‘f’, specifies which file register is to be used by the instruction. The destination designator, ‘d’, specifies where the result of the operation is to be placed. If ‘d’ is ‘0’, the result is placed in the WREG register. If ‘d’ is ‘1’, the result is placed in the file register specified in the instruction.

All **bit-oriented** instructions have three operands:

1. The file register (specified by ‘f’)
2. The bit in the file register (specified by ‘b’)
3. The accessed memory (specified by ‘a’)

The bit field designator ‘b’ selects the number of the bit affected by the operation, while the file register designator, ‘f’, represents the number of the file in which the bit is located.

The **literal** instructions may use some of the following operands:

- A literal value to be loaded into a file register (specified by ‘k’)
- The desired FSR register to load the literal value into (specified by ‘f’)
- No operand required (specified by ‘—’)

The **control** instructions may use some of the following operands:

- A program memory address (specified by ‘n’)
- The mode of the CALL or RETURN instructions (specified by ‘s’)
- The mode of the table read and table write instructions (specified by ‘m’)
- No operand required (specified by ‘—’)

All instructions are a single word, except for four double-word instructions. These instructions were made double-word to contain the required information in 32 bits. In the second word, the 4 MSbs are ‘1’s. If this second word is executed as an instruction (by itself), it will execute as a NOP.

All single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles with the additional instruction cycle(s) executed as a NOP.

The double-word instructions execute in two instruction cycles.

One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true, or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs. Two-word branch instructions (if true) would take 3 μs.

Figure 26-1 shows the general formats that the instructions can have. All examples use the convention ‘nnh’ to represent a hexadecimal number.

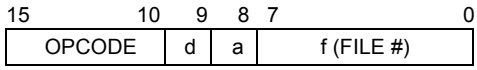
The instruction set summary, shown in Table 26-2, lists the standard instructions recognized by the Microchip MPASM™ Assembler.

Section 26.1.1 “Standard Instruction Set” provides a description of each instruction.

FIGURE 26-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations

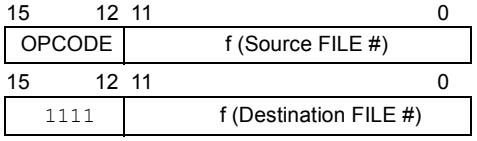
Example Instruction



ADDWF MYREG, W, B

d = 0 for result destination to be WREG register
d = 1 for result destination to be file register (f)
a = 0 to force Access Bank
a = 1 for BSR to select bank
f = 8-bit file register address

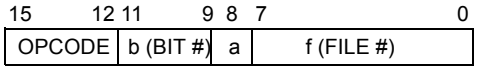
Byte to Byte move operations (2-word)



MOVFF MYREG1, MYREG2

f = 12-bit file register address

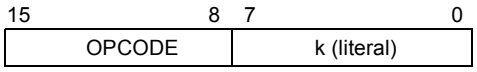
Bit-oriented file register operations



BSF MYREG, bit, B

b = 3-bit position of bit in file register (f)
a = 0 to force Access Bank
a = 1 for BSR to select bank
f = 8-bit file register address

Literal operations

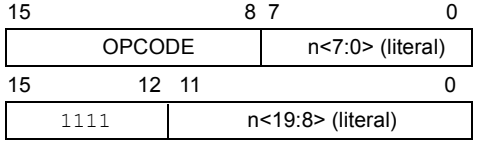


MOVLW 7Fh

k = 8-bit immediate value

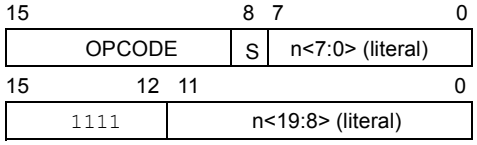
Control operations

CALL, GOTO and Branch operations



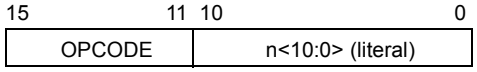
GOTO Label

n = 20-bit immediate value

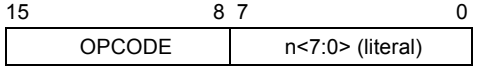


CALL MYFUNC

S = Fast bit



BRA MYFUNC



BC MYFUNC

28.2 DC Characteristics: Power-Down and Supply Current PIC18F87J50 Family (Industrial) (Continued)

PIC18F87J50 Family (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (IDD) Cont.(2)						
	All devices	0.17	0.35	mA	-40°C	VDD = 2.0V, VDDCORE = 2.0V(4)	FOSC = 1 MHz (**PRI_RUN** mode, EC oscillator)
		0.18	0.35	mA	+25°C		
		0.20	0.42	mA	+85°C		
	All devices	0.29	0.52	mA	-40°C	VDD = 2.5V, VDDCORE = 2.5V(4)	
		0.31	0.52	mA	+25°C		
		0.34	0.61	mA	+85°C		
	All devices	0.59	1.1	mA	-40°C	VDD = 3.3V(5)	
		0.44	0.85	mA	+25°C		
		0.42	0.85	mA	+85°C		
	All devices	0.70	1.25	mA	-40°C	VDD = 2.0V, VDDCORE = 2.0V(4)	FOSC = 4 MHz (**PRI_RUN** mode, EC oscillator)
		0.75	1.25	mA	+25°C		
		0.79	1.36	mA	+85°C		
	All devices	1.10	1.7	mA	-40°C	VDD = 2.5V, VDDCORE = 2.5V(4)	
		1.10	1.7	mA	+25°C		
		1.12	1.82	mA	+85°C		
	All devices	1.55	1.95	mA	-40°C	VDD = 3.3V(5)	
		1.47	1.89	mA	+25°C		
		1.54	1.92	mA	+85°C		
	All devices	9.9	14.8	mA	-40°C	VDD = 2.5V, VDDCORE = 2.5V(4)	FOSC = 48 MHz (**PRI_RUN** mode, EC oscillator)
		9.5	14.8	mA	+25°C		
		10.1	15.2	mA	+85°C		
	All devices	13.3	23.2	mA	-40°C	VDD = 3.3V(5)	
		12.2	22.7	mA	+25°C		
		12.1	22.7	mA	+85°C		

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption. All features that add delta current are disabled (USB module, WDT, etc.).
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
MCLR = VDD; WDT disabled unless otherwise specified.

3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

4: Voltage regulator disabled (ENVREG = 0, tied to VSS).

5: Voltage regulator enabled (ENVREG = 1, tied to VDD), REGSLP = 1.

6: This is the module differential current when the USB module is enabled and clocked at 48 MHz, but with no USB cable attached. When the USB cable is attached or data is being transmitted, the current consumption may be much higher (see **Section 22.6.4 "USB Transceiver Current Consumption"**). During USB Suspend mode (USBEN = 1, SUSPND = 1, bus in Idle state), the USB module current will be dominated by the D+ or D- pull-up resistor. The integrated pull-up resistors use "resistor switching" according to the resistor_ecn supplement to the USB 2.0 specifications, and therefore, may be as low as 900Ω during Idle conditions.

INDEX

A

B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	PIC18F65J50/66J50/66J55/67J50(1), PIC18F85J50/86J50/86J55/87J50(1), PIC18F65J50/66J50/66J55/67J50T(2), PIC18F85J50/86J50/86J55/87J50T(2);
Temperature Range	I = -40°C to +85°C (Industrial)
Package	PT = TQFP (Thin Quad Flatpack)
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

a) PIC18F86J50-I/PT 301 = Industrial temp., TQFP package, QTP pattern #301.

b) PIC18F66J55T-I/PT = Tape and reel, Industrial temp., TQFP package.

Note 1: F = Standard Voltage Range
2: T = In tape and reel