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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	65
Program Memory Size	96KB (48K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f86j55-i-pt

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TABLE 1-3: PIC18F6XJ5X PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	64-TQFP			
				PORTG is a bidirectional I/O port.
RG0/PMA8/ECCP3/P3A	3			
RG0		I/O	ST	Digital I/O.
PMA8		O	—	Parallel Master Port address.
ECCP3		I/O	—	Capture 3 input/Compare 3 output/PWM3 output.
P3A		O	—	ECCP3 PWM output A.
RG1/PMA7/TX2/CK2	4			
RG1		I/O	ST	Digital I/O.
PMA7		O	—	Parallel Master Port address.
TX2		O	—	EUSART2 asynchronous transmit.
CK2		I/O	ST	EUSART2 synchronous clock (see related RX2/DT2).
RG2/PMA6/RX2/DT2	5			
RG2		I/O	ST	Digital I/O.
PMA6		O	—	Parallel Master Port address.
RX2		I	ST	EUSART2 asynchronous receive.
DT2		I/O	ST	EUSART2 synchronous data (see related TX2/CK2).
RG3/PMCS1/CCP4/P3D	6			
RG3		I/O	ST	Digital I/O.
PMCS1		O	—	Parallel Master Port chip select 1.
CCP4		I/O	ST	Capture 4 input/Compare 4 output/PWM4 output.
P3D		O	—	ECCP3 PWM output D.
RG4/PMCS2/CCP5/P1D	8			
RG4		I/O	ST	Digital I/O.
PMCS2		O	—	Parallel Master Port chip select 2.
CCP5		I/O	ST	Capture 5 input/Compare 5 output/PWM5 output.
P1D		O	—	ECCP1 PWM output D.
VSS	9, 25, 41, 56	P	—	Ground reference for logic and I/O pins.
VDD	26, 38, 57	P	—	Positive supply for peripheral digital logic and I/O pins.
AVSS	20	P	—	Ground reference for analog modules.
AVDD	19	P	—	Positive supply for analog modules.
ENVREG	18	I	ST	Enable for on-chip voltage regulator.
VDDCORE/VCAP	10			Core logic power or external filter capacitor connection.
VDDCORE		P	—	Positive supply for microcontroller core logic (regulator disabled).
VCAP		P	—	External filter capacitor connection (regulator enabled).
VUSB	17	P	—	USB voltage input pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for ECCP2/P2A when CCP2MX Configuration bit is set.

2: Alternate assignment for ECCP2/P2A when CCP2MX Configuration bit is cleared.

3: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 4-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset RESET Instruction Stack Resets CM Resets	Wake-up via WDT or Interrupt
PORTJ	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTH	Feature1	PIC18F8XJ5X	0000 xxxx	uuuu uuuu	uuuu uuuu
PORTG	Feature1	PIC18F8XJ5X	000x xxxx	000u uuuu	uuuu uuuu
PORTF	Feature1	PIC18F8XJ5X	x00x x0--	u00u u0--	u00u u0--
PORTE	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTD	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTB	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	Feature1	PIC18F8XJ5X	--0x 0000	--0u 0000	--uu uuuu
SPBRGH1	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
BAUDCON1	Feature1	PIC18F8XJ5X	0100 0-00	0100 0-00	uuuu u-uu
SPBRGH2	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
BAUDCON2	Feature1	PIC18F8XJ5X	0100 0-00	0100 0-00	uuuu u-uu
TMR3H	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR3L	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
T3CON	Feature1	PIC18F8XJ5X	0000 0000	uuuu uuuu	uuuu uuuu
TMR4	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
PR4	Feature1	PIC18F8XJ5X	1111 1111	1111 1111	1111 1111
CVRCON	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
T4CON	Feature1	PIC18F8XJ5X	-000 0000	-000 0000	-uuu uuuu
CCPR4H	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR4L	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP4CON	Feature1	PIC18F8XJ5X	--00 0000	--00 0000	--uu uuuu
CCPR5H	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR5L	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP5CON	Feature1	PIC18F8XJ5X	--00 0000	--00 0000	--uu uuuu
SSP2BUF	Feature1	PIC18F8XJ5X	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSP2ADD	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
SSP2MSK	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
SSP2STAT	Feature1	PIC18F8XJ5X	1111 1111	1111 1111	uuuu uuuu
SSP2CON1	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
SSP2CON2	Feature1	PIC18F8XJ5X	0000 0000	0000 0000	uuuu uuuu
CMSTAT	Feature1	PIC18F8XJ5X	---- --11	---- --11	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 4-1 for Reset value for specific condition.

TABLE 5-5: REGISTER FILE SUMMARY (PIC18F87J50 FAMILY) (CONTINUED)

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on Page:
ECCP1AS	ECCP1ASE	ECCP1AS2	ECCP1AS1	ECCP1AS0	PSS1AC1	PSS1AC0	PSS1BD1	PSS1BD0	0000 0000	63, 232
ECCP1DEL	P1RSEN	P1DC6	P1DC5	P1DC4	P1DC3	P1DC2	P1DC1	P1DC0	0000 0000	63, 232
CCPR1H	Capture/Compare/PWM Register 1 HIgh Byte								xxxx xxxx	63, 232
CCPR1L	Capture/Compare/PWM Register 1 Low Byte								xxxx xxxx	63, 232
CCP1CON	P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	63, 232
ECCP2AS	ECCP2ASE	ECCP2AS2	ECCP2AS1	ECCP2AS0	PSS2AC1	PSS2AC0	PSS2BD1	PSS2BD0	0000 0000	63, 232
ECCP2DEL	P2RSEN	P2DC6	P2DC5	P2DC4	P2DC3	P2DC2	P2DC1	P2DC0	0000 0000	63, 232
CCPR2H	Capture/Compare/PWM Register 2 High Byte								xxxx xxxx	63, 232
CCPR2L	Capture/Compare/PWM Register 2 Low Byte								xxxx xxxx	63, 232
CCP2CON	P2M1	P2M0	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	0000 0000	63, 232
ECCP3AS	ECCP3ASE	ECCP3AS2	ECCP3AS1	ECCP3AS0	PSS3AC1	PSS3AC0	PSS3BD1	PSS3BD0	0000 0000	63, 232
ECCP3DEL	P3RSEN	P3DC6	P3DC5	P3DC4	P3DC3	P3DC2	P3DC1	P3DC0	0000 0000	63, 232
CCPR3H	Capture/Compare/PWM Register 3 High Byte								xxxx xxxx	63, 232
CCPR3L	Capture/Compare/PWM Register 3 Low Byte								xxxx xxxx	63, 232
CCP3CON	P3M1	P3M0	DC3B1	DC3B0	CCP3M3	CCP3M2	CCP3M1	CCP3M0	0000 0000	63, 232
SPBRG1	EUSART1 Baud Rate Generator Register Low Byte								0000 0000	63, 283
RCREG1	EUSART1 Receive Register								0000 0000	63, 291, 292
TXREG1	EUSART1 Transmit Register								xxxx xxxx	63, 289, 290
TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	63, 289
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	63, 291
SPBRG2	EUSART2 Baud Rate Generator Register Low Byte								0000 0000	63, 283
RCREG2	EUSART2 Receive Register								0000 0000	63, 291, 292
TXREG2	EUSART2 Transmit Register								0000 0000	63, 289, 290
TXSTA2	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	63, 289
EECON2	Program Memory Control Register 2 (not a physical register)								---- ----	63, 98
EECON1	—	—	WPROG	FREE	WRERR	WREN	WR	—	--00 x00-	63, 98
IPR3	SSP2IP	BCL2IP	RC2IP	TX2IP	TMR4IP	CCP5IP	CCP4IP	CCP3IP	1111 1111	64, 132
PIR3	SSP2IF	BCL2IF	RC2IF	TX2IF	TMR4IF	CCP5IF	CCP4IF	CCP3IF	0000 0000	64, 126
PIE3	SSP2IE	BCL2IE	RC2IE	TX2IE	TMR4IE	CCP5IE	CCP4IE	CCP3IE	0000 0000	64, 129
IPR2	OSCFIP	CM2IP	CM1IP	USBIP	BCL1IP	LVDIP	TMR3IP	CCP2IP	1111 1111	64, 132
PIR2	OSCFIF	CM2IF	CM1IF	USBIF	BCL1IF	LVDIF	TMR3IF	CCP2IF	0000 0000	64, 126
PIE2	OSCFIE	CM2IE	CM1IE	USBIE	BCL1IE	LVDIE	TMR3IE	CCP2IE	0000 0000	64, 129
IPR1	PMPIP	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	1111 1111	64, 132
PIR1	PMPIF	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	0000 0000	64, 126
PIE1	PMPIE	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	0000 0000	64, 129
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	64, 291
OSCTUNE	INTSRC	PLLEN	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0	0000 0000	64, 39

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition. **Bold** indicates shared-access SFRs.

Note 1: Bit 21 of the PC is only available in Serial Programming modes.

2: Default (legacy) SFR at this address, available when WDTCON<4> = 0.

3: Configuration SFR, overlaps with default SFR at this address; available only when WDTCON<4> = 1.

4: Reset value is '0' when Two-Speed Start-up is enabled and '1' if disabled.

5: The SSPxMSK registers are only accessible when SSPxCON2<3:0> = 1001.

6: Alternate names and definitions for these bits when the MSSP module is operating in I^2C™ Slave mode. See **Section 19.4.3.2 "Address Masking Modes"** for details

7: These bits and/or registers are only available in 80-pin devices; otherwise, they are unimplemented and read as '0'. Reset values are shown for 80-pin devices.

8: The PMADDRH/PMDOUT1H and PMADDRL/PMDOUT1L register pairs share the physical registers and addresses, but have different functions determined by the module's operating mode. See **Section 11.1.2 "Data Registers"** for more information.

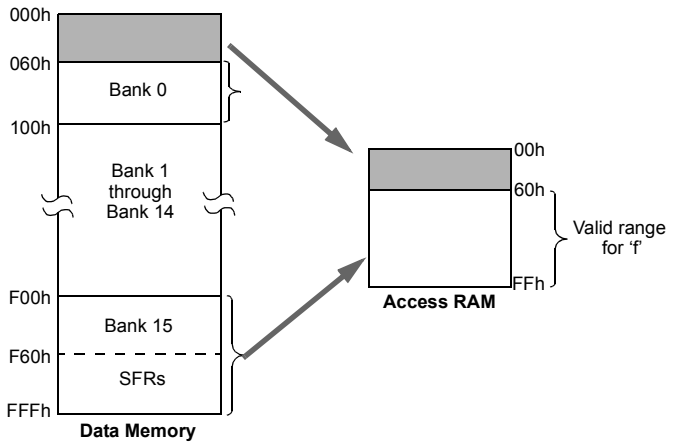
FIGURE 5-10: COMPARING ADDRESSING OPTIONS FOR BIT-ORIENTED AND BYTE-ORIENTED INSTRUCTIONS (EXTENDED INSTRUCTION SET ENABLED)

EXAMPLE INSTRUCTION: `ADDWF, f, d, a` (Opcode: `0010 01da ffff ffff`)

When a = 0 and f ≥ 60h:

The instruction executes in Direct Forced mode. 'f' is interpreted as a location in the Access RAM between 060h and FFFh. This is the same as locations F60h to FFFh (Bank 15) of data memory.

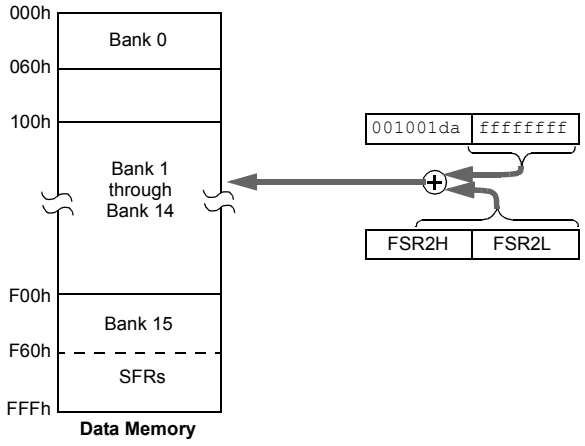
Locations below 060h are not available in this addressing mode.



When a = 0 and f ≤ 5Fh:

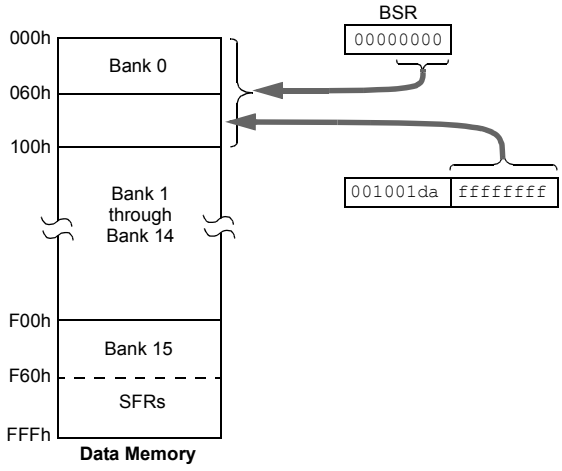
The instruction executes in Indexed Literal Offset mode. 'f' is interpreted as an offset to the address value in FSR2. The two are added together to obtain the address of the target register for the instruction. The address can be anywhere in the data memory space.

Note that in this mode, the correct syntax is now:
`ADDWF [k], d`
where 'k' is the same as 'f'.



When a = 1 (all values of f):

The instruction executes in Direct mode (also known as Direct Long mode). 'f' is interpreted as a location in one of the 16 banks of the data memory space. The bank is designated by the Bank Select Register (BSR). The address can be in any implemented bank in the data memory space.



NOTES:

TABLE 11-3: REGISTERS ASSOCIATED WITH PMP MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	61
PIR1	PMPIF	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	64
PIE1	PMPIE	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	64
IPR1	PMPIP	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	64
PMCONH	PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	PTBEEN	PTWREN	PTRDEN	66
PMCONL	CSF1	CSF0	ALP	CS2P	CS1P	BEP	WRSP	RDSP	67
PMADDRH(1)/	CS2	CS1	Parallel Master Port Address, High Byte						66
PMDOUT1H(1)	Parallel Port Out Data, High Byte (Buffer 1)								66
PMADDRL(1)/	Parallel Master Port Address, Low Byte								66
PMDOUT1L(1)	Parallel Port Out Data, Low Byte (Buffer 0)								66
PMDOUT2H	Parallel Port Out Data, High Byte (Buffer 3)								66
PMDOUT2L	Parallel Port Out Data, Low Byte (Buffer 2)								66
PMDIN1H	Parallel Port In Data, High Byte (Buffer 1)								66
PMDIN1L	Parallel Port In Data, Low Byte (Buffer 0)								66
PMDIN2H	Parallel Port In Data, High Byte (Buffer 3)								67
PMDIN2L	Parallel Port In Data, Low Byte (Buffer 2)								67
PMMODEH	BUSY	IRQM1	IRQM0	INCM1	INCM0	MODE16	MODE1	MODE0	67
PMMODEL	WAITB1	WAITB0	WAITM3	WAITM2	WAITM1	WAITM0	WAITE1	WAITE0	67
PMEH	PTEN15	PTEN14	PTEN13	PTEN12	PTEN11	PTEN10	PTEN9	PTEN8	67
PMEL	PTEN7	PTEN6	PTEN5	PTEN4	PTEN3	PTEN2	PTEN1	PTEN0	67
PMSTATH	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	67
PMSTATL	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	67
PADCFG1(2)	—	—	—	—	—	—	—	PMPTTL	62

Legend: — = unimplemented, read as '0'. Shaded cells are not used during ECCP operation.

Note 1: The PMADDRH/PMDOUT1H and PMADDRL/PMDOUT1L register pairs share the physical registers and addresses, but have different functions determined by the module's operating mode.

2: Configuration SFR, overlaps with default SFR at this address; available only when WDTCON<4> = 1.

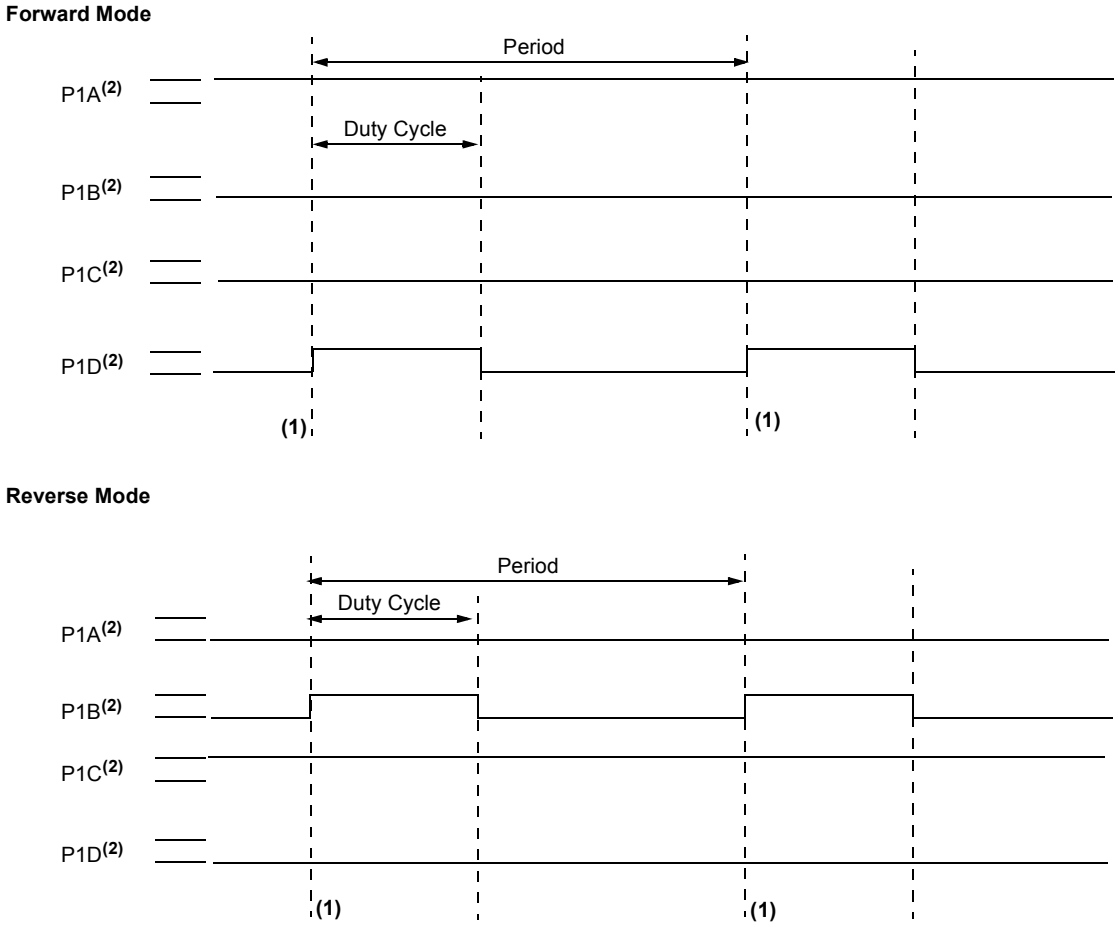
NOTES:

18.4.5 FULL-BRIDGE MODE

In Full-Bridge Output mode, four pins are used as outputs; however, only two outputs are active at a time. In the Forward mode, pin P1A is continuously active and pin P1D is modulated. In the Reverse mode, pin P1C is continuously active and pin P1B is modulated. These are illustrated in Figure 18-6.

P1A, P1B, P1C and P1D outputs are multiplexed with the port pins as described in Table 18-1, Table 18-2 and Table 18-3. The corresponding TRIS bits must be cleared to make the P1A, P1B, P1C and P1D pins outputs.

FIGURE 18-6: FULL-BRIDGE PWM OUTPUT



Note 1: At this time, the TMR2 register is equal to the PR2 register.
2: Output signal is shown as active-high.

REGISTER 20-1: TXSTAx: TRANSMIT STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN(1)	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **CSRC:** Clock Source Select bit

Asynchronous mode:
Don't care.

Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

bit 6 **TX9:** 9-Bit Transmit Enable bit

1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5 **TXEN:** Transmit Enable bit(1)

1 = Transmit enabled
0 = Transmit disabled

bit 4 **SYNC:** EUSART Mode Select bit

1 = Synchronous mode
0 = Asynchronous mode

bit 3 **SENDB:** Send Break Character bit

Asynchronous mode:
1 = Send Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission completed

Synchronous mode:
Don't care.

bit 2 **BRGH:** High Baud Rate Select bit

Asynchronous mode:
1 = High speed
0 = Low speed

Synchronous mode:
Unused in this mode.

bit 1 **TRMT:** Transmit Shift Register Status bit

1 = TSR empty
0 = TSR full

bit 0 **TX9D:** 9th bit of Transmit Data

Can be address/data bit or a parity bit.

Note 1: SREN/CREN overrides TXEN in Sync mode.

REGISTER 20-2: RCSTAx: RECEIVE STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **SPEN:** Serial Port Enable bit
1 = Serial port enabled (configures RXx/DTx and TXx/CKx pins as serial port pins)
0 = Serial port disabled (held in Reset)

bit 6 **RX9:** 9-Bit Receive Enable bit
1 = Selects 9-bit reception
0 = Selects 8-bit reception

bit 5 **SREN:** Single Receive Enable bit
Asynchronous mode:
Don't care.
Synchronous mode – Master:
1 = Enables single receive
0 = Disables single receive
This bit is cleared after reception is complete.
Synchronous mode – Slave:
Don't care.

bit 4 **CREN:** Continuous Receive Enable bit
Asynchronous mode:
1 = Enables receiver
0 = Disables receiver
Synchronous mode:
1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
0 = Disables continuous receive

bit 3 **ADDEN:** Address Detect Enable bit
Asynchronous mode 9-Bit (RX9 = 1):
1 = Enables address detection, enables interrupt and loads the receive buffer when RSR<8> is set
0 = Disables address detection, all bytes are received and ninth bit can be used as parity bit
Asynchronous mode 9-Bit (RX9 = 0):
Don't care.

bit 2 **FERR:** Framing Error bit
1 = Framing error (can be updated by reading RCREGx register and receiving next valid byte)
0 = No framing error

bit 1 **OERR:** Overrun Error bit
1 = Overrun error (can be cleared by clearing bit CREN)
0 = No overrun error

bit 0 **RX9D:** 9th bit of Received Data
This can be address/data bit or a parity bit and must be calculated by user firmware.

20.3.2 EUSART SYNCHRONOUS MASTER RECEPTION

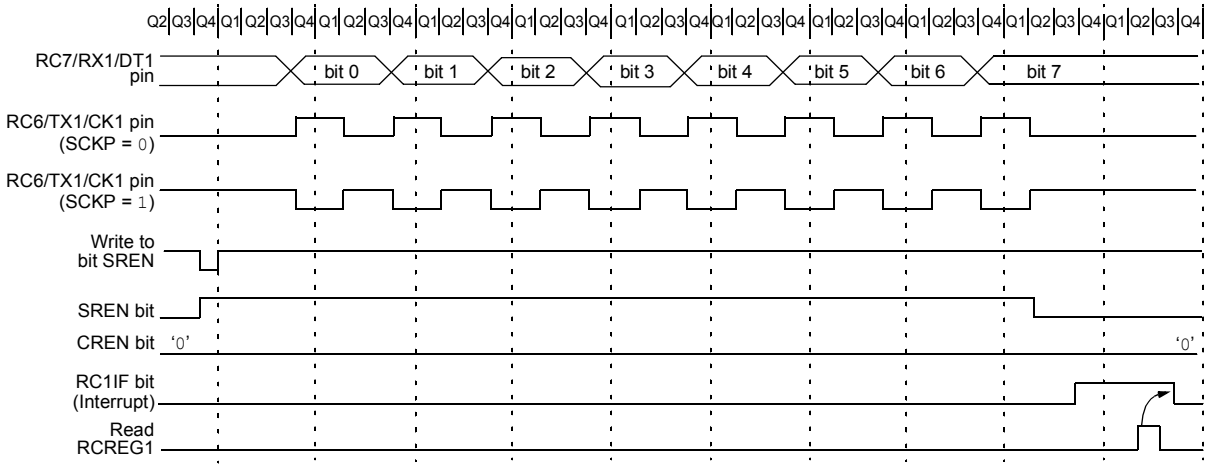
Once Synchronous mode is selected, reception is enabled by setting either the Single Receive Enable bit, SREN (RCSTAx<5>) or the Continuous Receive Enable bit, CREN (RCSTAx<4>). Data is sampled on the RXx pin on the falling edge of the clock.

If enable bit, SREN, is set, only a single word is received. If enable bit, CREN, is set, the reception is continuous until CREN is cleared. If both bits are set, then CREN takes precedence.

To set up a Synchronous Master Reception:

1. Initialize the SPBRGHx:SPBRGx registers for the appropriate baud rate. Set or clear the BRG16 bit, as required, to achieve the desired baud rate.
2. Enable the synchronous master serial port by setting bits, SYNC, SPEN and CSRC.
3. Ensure bits, CREN and SREN, are clear.
4. If interrupts are desired, set enable bit, RCxIE.
5. If 9-bit reception is desired, set bit, RX9.
6. If a single reception is required, set bit, SREN. For continuous reception, set bit, CREN.
7. Interrupt flag bit, RCxIF, will be set when reception is complete and an interrupt will be generated if the enable bit, RCxIE, was set.
8. Read the RCSTAx register to get the 9th bit (if enabled) and determine if any error occurred during reception.
9. Read the 8-bit received data by reading the RCREGx register.
10. If any error occurred, clear the error by clearing bit, CREN.
11. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

FIGURE 20-13: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



Note: Timing diagram demonstrates Sync Master mode with bit SREN = 1 and bit BRGH = 0. This example is equally applicable to EUSART2 (RG1/TX2/CK2 and RG2/RX2/DT2).

NOTES:

TABLE 25-1: MAPPING OF THE FLASH CONFIGURATION WORDS TO THE CONFIGURATION REGISTERS

Configuration Byte	Code Space Address	Configuration Register Address
CONFIG1L	XXXF8h	300000h
CONFIG1H	XXXF9h	300001h
CONFIG2L	XXXFAh	300002h
CONFIG2H	XXXFBh	300003h
CONFIG3L	XXXFCh	300004h
CONFIG3H	XXXFDh	300005h
CONFIG4L(1)	XXXFEh	300006h
CONFIG4H(1)	XXXFFh	300007h

Note 1: Unimplemented in PIC18F87J10 family devices.

TABLE 25-2: CONFIGURATION BITS AND DEVICE IDs

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value(1)
300000h	CONFIG1L	$\overline{\text{DEBUG}}$	XINST	STVREN	—	PLLDIV2	PLLDIV1	PLLDIV0	WDTEN	111- 1111
300001h	CONFIG1H	—(2)	—(2)	—(2)	—(2)	—	CP0	CPDIV1	CPDIV0	1111 -111
300002h	CONFIG2L	IESO	FCMEN	—	—	—	FOSC2	FOSC1	FOSC0	11-- -111
300003h	CONFIG2H	—(2)	—(2)	—(2)	—(2)	WDTPS3	WDTPS2	WDTPS1	WDTPS0	1111 1111
300004h	CONFIG3L	WAIT(3)	BW(3)	EMB1(3)	EMB0(3)	EASHFT(3)	—	—	—	1111 1---
300005h	CONFIG3H	—(2)	—(2)	—(2)	—(2)	MSSPMSK	PMPMX(3)	ECCPMX(3)	CCP2MX	1111 1111
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxx0 0000(4)
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	0100 00xx(4)

Legend: x = unknown, u = unchanged, - = unimplemented. Shaded cells are unimplemented, read as '0'.

Note 1: Values reflect the unprogrammed state as received from the factory and following Power-on Resets. In all other Reset states, the configuration bytes maintain their previously programmed states.

2: The value of these bits in program memory should always be '1'. This ensures that the location is executed as a NOP if it is accidentally executed.

3: Implemented in 80-pin devices only.

4: See Register 25-7 and Register 25-8 for DEVID values. These registers are read-only and cannot be programmed by the user.

REGISTER 25-2: CONFIG1H: CONFIGURATION REGISTER 1 HIGH (BYTE ADDRESS 300001h)

U-1	U-1	U-1	U-1	U-0	R/WO-1	R/WO-1	R/WO-1
—	—	—	—	—	CP0	CPDIV1	CPDIV0
bit 7							bit 0

Legend:			
R = Readable bit	WO = Write-Once bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented:** Maintain as '1'

bit 3 **Unimplemented:** Read as '0'

bit 2 **CP0:** Code Protection bit
1 = Program memory is not code-protected
0 = Program memory is code-protected

bit 1-0 **CPDIV1:CPDIV0:** CPU System Clock Selection bits
11 = No CPU system clock divide
10 = CPU system clock divided by 2
01 = CPU system clock divided by 3
00 = CPU system clock divided by 6

25.2 Watchdog Timer (WDT)

For PIC18F87J10 family devices, the WDT is driven by the INTRC oscillator. When the WDT is enabled, the clock source is also enabled. The nominal WDT period is 4 ms and has the same stability as the INTRC oscillator.

The 4 ms period of the WDT is multiplied by a 16-bit postscaler. Any output of the WDT postscaler is selected by a multiplexor, controlled by the WDTPS bits in Configuration Register 2H. Available periods range from about 4 ms to 135 seconds (2.25 minutes depending on voltage, temperature and WDT postscaler). The WDT and postscaler are cleared whenever a `SLEEP` or `CLRWDT` instruction is executed, or a clock failure (primary or Timer1 oscillator) has occurred.

Note 1: The `CLRWDT` and `SLEEP` instructions clear the WDT and postscaler counts when executed.

2: When a `CLRWDT` instruction is executed, the postscaler count will be cleared.

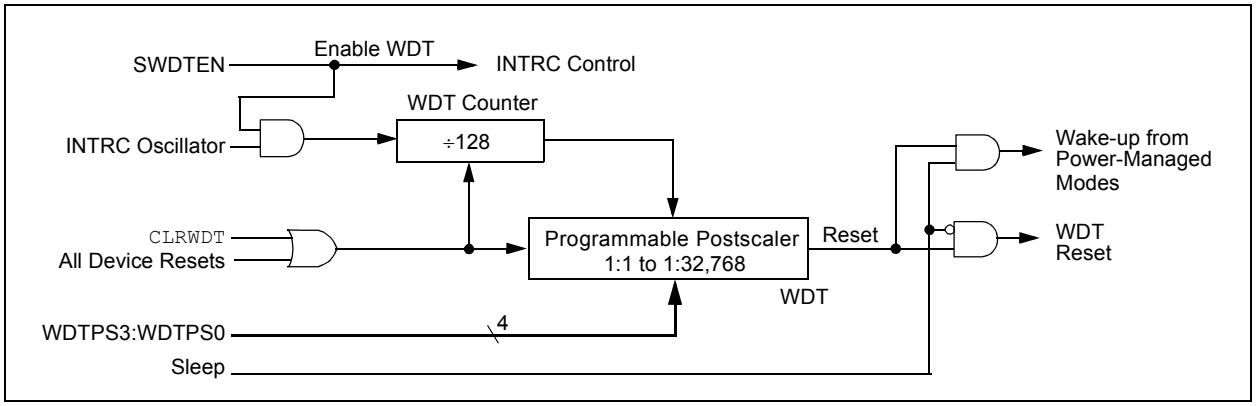
25.2.1 CONTROL REGISTER

The WDTCON register (Register 25-9) is a readable and writable register. The SWDTEN bit enables or disables WDT operation. This allows software to override the WDTEN Configuration bit and enable the WDT only if it has been disabled by the Configuration bit.

The ADSHR bit selects which SFRs currently are selected and accessible. For additional details, see **Section 5.3.5.1 "Shared Address SFRs"**.

LVDSTAT is a read-only status bit that is continuously updated and provides information about the current level of V_{DDCORE}. This bit is only valid when the on-chip voltage regulator is enabled.

FIGURE 25-1: WDT BLOCK DIAGRAM



BTFSC **Bit Test File, Skip if Clear**

Syntax: BTFSC f, b {,a}

Operands: $0 \le f \le 255$
$0 \le b \le 7$
$a \in [0,1]$

Operation: skip if (f<b>) = 0

Status Affected: None

Encoding:

1011	bbba	ffff	ffff

Description: If bit 'b' in register 'f' is '0', then the next instruction is skipped. If bit 'b' is '0', then the next instruction fetched during the current instruction execution is discarded and a NOP is executed instead, making this a two-cycle instruction.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 26.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1(2)
Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:
```
HERE    BTFSC   FLAG, 1, 0
FALSE   :
TRUE    :
```

Before Instruction
PC = address (HERE)
After Instruction
If FLAG<1> = 0;
PC = address (TRUE)
If FLAG<1> = 1;
PC = address (FALSE)

BTFSS **Bit Test File, Skip if Set**

Syntax: BTFSS f, b {,a}

Operands: $0 \le f \le 255$
$0 \le b < 7$
$a \in [0,1]$

Operation: skip if (f<b>) = 1

Status Affected: None

Encoding:

1010	bbba	ffff	ffff

Description: If bit 'b' in register 'f' is '1', then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution is discarded and a NOP is executed instead, making this a two-cycle instruction.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 26.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1(2)
Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

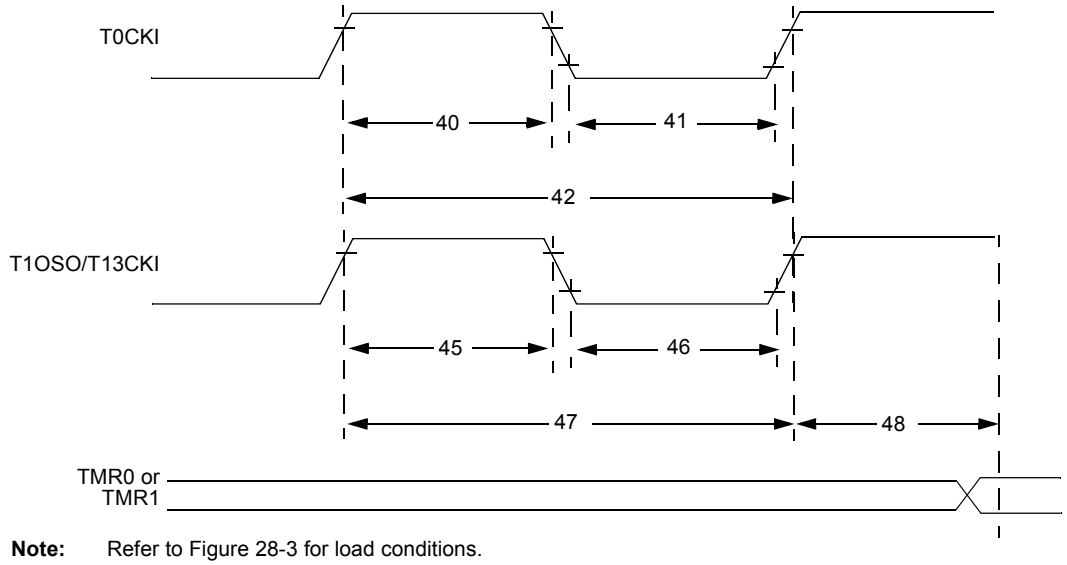
If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:
```
HERE    BTFSS   FLAG, 1, 0
FALSE   :
TRUE    :
```

Before Instruction
PC = address (HERE)
After Instruction
If FLAG<1> = 0;
PC = address (FALSE)
If FLAG<1> = 1;
PC = address (TRUE)

FIGURE 28-9: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS



Note: Refer to Figure 28-3 for load conditions.

TABLE 28-14: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
40	TT0H	T0CKI High Pulse Width	No prescaler	0.5 TCY + 20	—	ns	
			With prescaler	10	—	ns	
41	TT0L	T0CKI Low Pulse Width	No prescaler	0.5 TCY + 20	—	ns	
			With prescaler	10	—	ns	
42	TT0P	T0CKI Period	No prescaler	TCY + 10	—	ns	
			With prescaler	Greater of: 20 ns or (TCY + 40)/N	—	ns	N = prescale value (1, 2, 4,..., 256)
45	TT1H	T13CKI High Time	Synchronous, no prescaler	0.5 TCY + 20	—	ns	
			Synchronous, with prescaler	10	—	ns	
			Asynchronous	30	—	ns	
46	TT1L	T13CKI Low Time	Synchronous, no prescaler	0.5 TCY + 5	—	ns	
			Synchronous, with prescaler	10	—	ns	
			Asynchronous	30	—	ns	
47	TT1P	T13CKI Input Period	Synchronous	Greater of: 20 ns or (TCY + 40)/N	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	60	—	ns	
	FT1	T13CKI Oscillator Input Frequency Range		DC	50	kHz	
48	TCKE2TMRI	Delay from External T13CKI Clock Edge to Timer Increment		2 TOSC	7 TOSC	—	

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