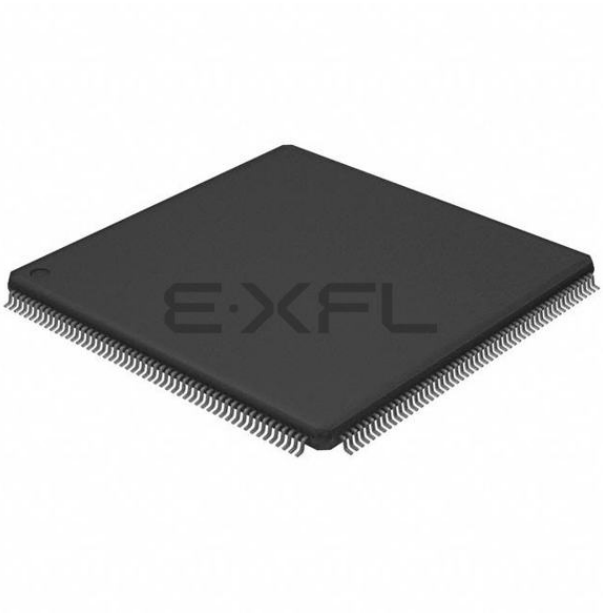

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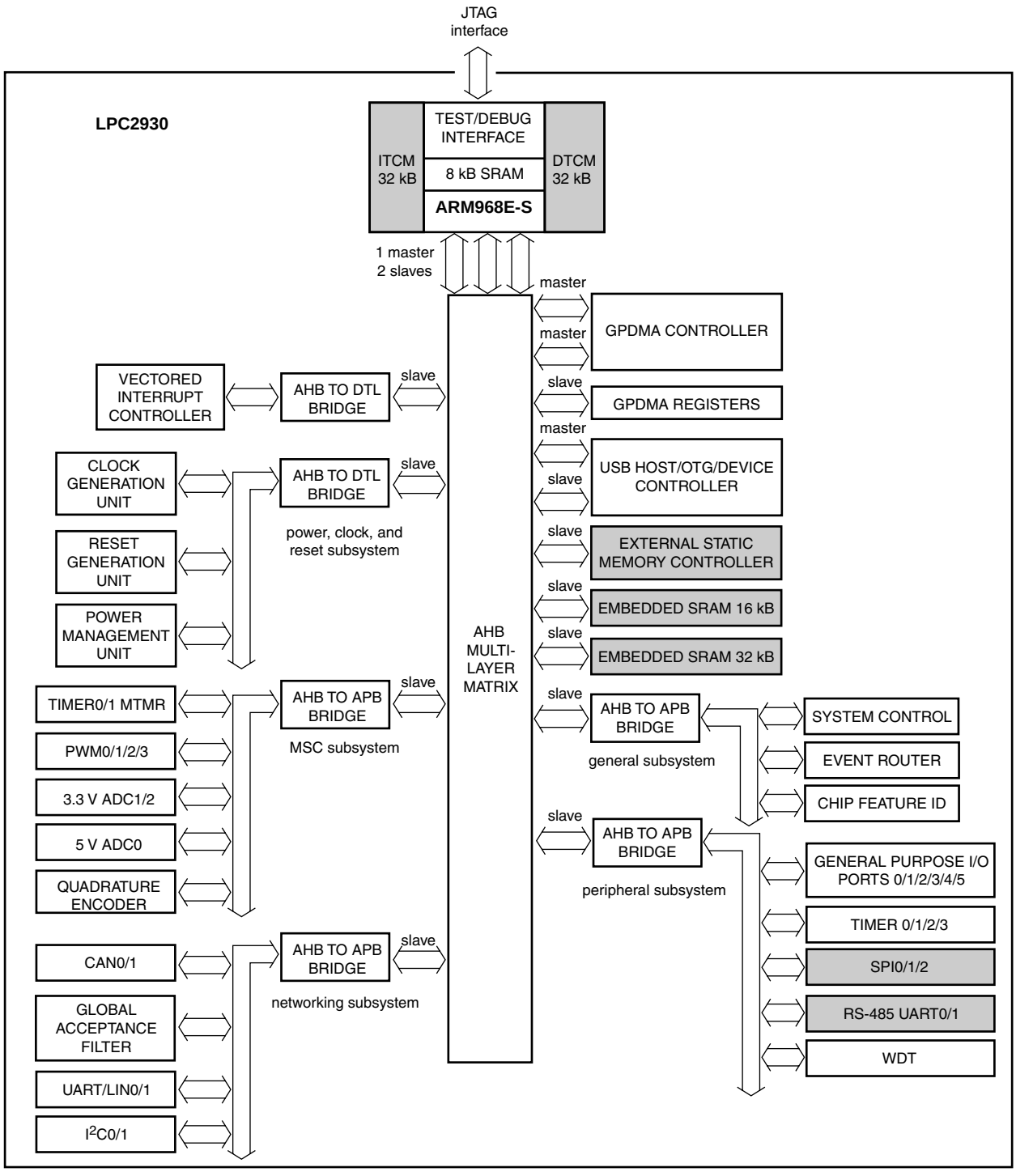
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM968E-S
Core Size	16/32-Bit
Speed	125MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, POR, PWM, WDT
Number of I/O	152
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2930fbd208-551

4. Block diagram



Grey-shaded blocks represent peripherals and memory regions accessible by the GPDMA.

Fig 1. LPC2930 block diagram

Table 3. LQFP208 pin assignment *…continued*

Pin name	Pin	Description			
		Function 0 (default)	Function 1	Function 2	Function 3
P2[4]/MAT1[0]/ EI0/D12	94[1]	GPIO 2, pin 4	TIMER1 MAT0	EXTINT0	EXTBUS D12
P2[5]/MAT1[1]/ EI1/D13	95[1]	GPIO 2, pin 5	TIMER1 MAT1	EXTINT1	EXTBUS D13
P1[9]/SDO1/ RXDL1/$\overline{CS1}$	96[1]	GPIO 1, pin 9	SPI1 SDO	LIN1 RXD/UART RXD	EXTBUS $\overline{CS1}$
$V_{SS(IO)}$	97	ground for I/O			
P1[8]/SCS1[0]/ TXDL1/$\overline{CS0}$	98[1]	GPIO 1, pin 8	SPI1 SCS0	LIN1 TXD/ UART TXD	EXTBUS $\overline{CS0}$
P1[7]/SCS1[3]/ RXD1/A7	99[1]	GPIO 1, pin 7	SPI1 SCS3	UART1 RXD	EXTBUS A7
P1[6]/SCS1[2]/ TXD1/A6	100[1]	GPIO 1, pin 6	SPI1 SCS2	UART1 TXD	EXTBUS A6
P2[6]/MAT1[2]/ EI2/D14	101[1]	GPIO 2, pin 6	TIMER1 MAT2	EXTINT2	EXTBUS D14 (BOOT0)[3]
P1[5]/SCS1[1]/ PMAT3[5]/A5	102[1]	GPIO 1, pin 5	SPI1 SCS1	PWM3 MAT5	EXTBUS A5
P1[4]/SCS2[2]/ PMAT3[4]/A4	103[1]	GPIO 1, pin 4	SPI2 SCS2	PWM3 MAT4	EXTBUS A4
$\overline{TRST}$	104[1]	IEEE 1149.1 test reset NOT; active LOW; pulled up internally			
$\overline{RST}$	105[1]	asynchronous device reset; active LOW; pulled up internally			
$V_{SS(OSC)}$	106	ground for oscillator			
XOUT_OSC	107[4]	crystal out for oscillator			
XIN_OSC	108[4]	crystal in for oscillator			
$V_{DD(OSC\_PLL)}$	109	1.8 V supply for oscillator and PLL			
$V_{SS(PLL)}$	110	ground for PLL			
P2[7]/MAT1[3]/ EI3/D15	111[1]	GPIO 2, pin 7	TIMER1 MAT3	EXTINT3	EXTBUS D15 (BOOT1)[3]
P3[14]/SDI1/ EI6/TXDC0	112[1]	GPIO 3, pin 14	SPI1 SDI	EXTINT6	CAN0 TXD
P3[15]/SCK1/ EI7/RXDC0	113[1]	GPIO 3, pin 15	SPI1 SCK	EXTINT7	CAN0 RXD
$V_{DD(IO)}$	114	3.3 V power supply for I/O			
P2[8]/CLK_OUT/ PMAT0[0]/SCS0[2]	115[1]	GPIO 2, pin 8	CLK_OUT	PWM0 MAT0	SPI0 SCS2
P2[9]/ $\overline{USB\_UP\_LED1}$/ PMAT0[1]/SCS0[1]	116[1]	GPIO 2, pin 9	$\overline{USB\_UP\_LED1}$	PWM0 MAT1	SPI0 SCS1
P1[3]/SCS2[1]/ PMAT3[3]/A3	117[1]	GPIO 1, pin 3	SPI2 SCS1	PWM3 MAT3	EXTBUS A3
P1[2]/SCS2[3]/ PMAT3[2]/A2	118[1]	GPIO 1, pin 2	SPI2 SCS3	PWM3 MAT2	EXTBUS A2
P1[1]/EI1/ PMAT3[1]/A1	119[1]	GPIO 1, pin 1	EXTINT1	PWM3 MAT1	EXTBUS A1

Table 3. LQFP208 pin assignment *…continued*

Pin name	Pin	Description			
		Function 0 (default)	Function 1	Function 2	Function 3
P5[6]/D18/RI0	148[1]	GPIO 5, pin 6	EXTBUS D18	UART0 RI	-
P4[14]/$\overline{\text{BLS2}}$	149[1]	GPIO 4, pin 14	EXTBUS $\overline{\text{BLS2}}$	-	-
P0[5]/IN0[1]/ PMAT0[3]/D29	150[1]	GPIO 0, pin 5	ADC0 IN1	PWM0 MAT3	EXTBUS D29
P5[14]/ USB_SSPND1/RTS0	151[1]	GPIO 5, pin 14	USB_SSPND1	UART0 RS	-
$V_{DD(IO)}$	152	3.3 V power supply for I/O			
P0[6]/IN0[2]/ PMAT0[4]/D30	153[1]	GPIO 0, pin 6	ADC0 IN2	PWM0 MAT4	EXTBUS D30
P0[7]/IN0[3]/ PMAT0[5]/D31	154[1]	GPIO 0, pin 7	ADC0 IN3	PWM0 MAT5	EXTBUS D31
$V_{DDA(ADC3V3)}$	155	3.3 V power supply for ADC			
JTAGSEL	156[1]	TAP controller select input; LOW-level selects the ARM debug mode; HIGH-level selects boundary scan; pulled up internally.			
$V_{DDA(ADC5V0)}$	157	5 V supply voltage for ADC0 and 5 V reference for ADC0.			
VREFP	158[4]	HIGH reference for ADC			
VREFN	159[4]	LOW reference for ADC			
P0[8]/IN1[0]/TXDL0/ A20	160[5]	GPIO 0, pin 8	ADC1 IN0	LIN0 TXD/ UART TXD	EXTBUS A20
P0[9]/IN1[1]/ RXDL0/A21	161[5]	GPIO 0, pin 9	ADC1 IN1	LIN0 RXD/ UART TXD	EXTBUS A21
P0[10]/IN1[2]/ PMAT1[0]/A8	162[5]	GPIO 0, pin 10	ADC1 IN2	PWM1 MAT0	EXTBUS A8
P0[11]/IN1[3]/ PMAT1[1]/A9	163[5]	GPIO 0, pin 11	ADC1 IN3	PWM1 MAT1	EXTBUS A9
P2[14]/SDA1/ PCAP0[0]/$\overline{\text{BLS0}}$	164[1]	GPIO 2, pin 14	I^2C1 SDA	PWM0 CAP0	EXTBUS $\overline{\text{BLS0}}$
P2[15]/SCL1/ PCAP0[1]/$\overline{\text{BLS1}}$	165[1]	GPIO 2, pin 15	I^2C1 SCL	PWM0 CAP1	EXTBUS $\overline{\text{BLS1}}$
P3[2]/MAT3[0]/ PMAT2[2]/ USB_SDA1	166[1]	GPIO 3, pin 2	TIMER3 MAT0	PWM2 MAT2	USB_SDA1
$V_{DD(CORE)}$	167	1.8 V power supply for digital core			
$V_{SS(CORE)}$	168	ground for digital core			
$V_{SS(IO)}$	169	ground for I/O			
P4[3]/A11	170[1]	GPIO 4, pin 3	EXTBUS A11	-	-
P3[3]/MAT3[1]/ PMAT2[3]/ USB_SCL1	171[1]	GPIO 3, pin 3	TIMER3 MAT1	PWM2 MAT3	USB_SCL1
P5[3]/D11	172[1]	GPIO 5, pin 3	EXTBUS D11	-	-
P0[12]/IN1[4]/ PMAT1[2]/A10	173[5]	GPIO 0, pin 12	ADC1 IN4	PWM1 MAT2	EXTBUS A10
P4[19]/ $\overline{\text{USB\_CONNECT2}}$	174[1]	GPIO 4, pin 19	$\overline{\text{USB\_CONNECT2}}$	-	-

Table 3. LQFP208 pin assignment *…continued*

Pin name	Pin	Description			
		Function 0 (default)	Function 1	Function 2	Function 3
P0[13]/IN1[5]/ PMAT1[3]/A11	175[5]	GPIO 0, pin 13	ADC1 IN5	PWM1 MAT3	EXTBUS A11
$V_{DD(IO)}$	176	3.3 V power supply for I/O			
P4[11]/$\overline{WE}$/CTS0	177[1]	GPIO 4, pin 11	EXTBUS $\overline{WE}$	UART0 CTS	-
P0[14]/IN1[6]/ PMAT1[4]/A12	178[5]	GPIO 0, pin 14	ADC1 IN6	PWM1 MAT4	EXTBUS A12
P5[11]/D23/DCD0	179[1]	GPIO 5, pin 11	EXTBUS D23	UART0 DCD	-
P0[15]/IN1[7]/ PMAT1[5]/A13	180[5]	GPIO 0, pin 15	ADC1 IN7	PWM1 MAT5	EXTBUS A13
P4[23]/ $\overline{USB\_PWRD2}$	181[1]	GPIO 4, pin 23	$\overline{USB\_PWRD2}$	-	-
P0[16]IN2[0]/ TXD0/A22	182[5]	GPIO 0, pin 16	ADC2 IN0	UART0 TXD	EXTBUS A22
P4[7]/A21/DTR1	183[1]	GPIO 4, pin 7	EXTBUS A21	UART1 DTR	-
$V_{SS(IO)}$	184	ground for I/O			
P5[7]/D19/ U0OUT1	185[1]	GPIO 5, pin 7	EXTBUS D19	UART0 OUT1	-
P0[17]/IN2[1]/ RXD0/A23	186[5]	GPIO 0, pin 17	ADC2 IN1	UART0 RXD	EXTBUS A23
P4[15]/$\overline{BLS3}$	187[1]	GPIO 4, pin 15	EXTBUS $\overline{BLS3}$	-	-
P5[15]/ $\overline{USB\_UP\_LED1}$/ RTS1	188[1]	GPIO 5, pin 15	$\overline{USB\_UP\_LED1}$	UART1 RTS	-
$V_{DD(CORE)}$	189	1.8 V power supply for digital core			
$V_{SS(CORE)}$	190	ground for digital core			
P2[16]/TXD1/ PCAP0[2]/$\overline{BLS2}$	191[1]	GPIO 2, pin 16	UART1 TXD	PWM0 CAP2	EXTBUS $\overline{BLS2}$
P2[17]/RXD1/ PCAP1[0]/$\overline{BLS3}$	192[1]	GPIO 2, pin 17	UART1 RXD	PWM1 CAP0	EXTBUS $\overline{BLS3}$
$V_{DD(IO)}$	193	3.3 V power supply for I/O			
P0[18]/IN2[2]/ PMAT2[0]/A14	194[5]	GPIO 0, pin 18	ADC2 IN2	PWM2 MAT0	EXTBUS A14
P0[19]/IN2[3]/ PMAT2[1]/A15	195[5]	GPIO 0, pin 19	ADC2 IN3	PWM2 MAT1	EXTBUS A15
P3[4]/MAT3[2]/ PMAT2[4]/TXDC1	196[1]	GPIO 3, pin 4	TIMER3 MAT2	PWM2 MAT4	CAN1 TXD
P3[5]/MAT3[3]/ PMAT2[5]/RXDC1	197[1]	GPIO 3, pin 5	TIMER3 MAT3	PWM2 MAT5	CAN1 RXD
P2[18]/SCS2[1]/ PCAP1[1]/D16	198[1]	GPIO 2, pin 18	SPI2 SCS1	PWM1 CAP1	EXTBUS D16
P2[19]/SCS2[0]/ PCAP1[2]/D17	199[1]	GPIO 2, pin 19	SPI2 SCS0	PWM1 CAP2	EXTBUS D17
P0[20]/IN2[4]/ PMAT2[2]/A16	200[5]	GPIO 0, pin 20	ADC2 IN4	PWM2 MAT2	EXTBUS A16

Table 7. CGU0 base clock and branch clock overview *...continued*

Base clock	Branch clock name	Parts of the device clocked by this branch clock	Remark
BASE_MSCSS_CLK	CLK_MSCSS_APB	APB side of the MSCSS	
	CLK_MSCSS_MTMR0	timer 0 in the MSCSS	
	CLK_MSCSS_MTMR1	timer 1 in the MSCSS	
	CLK_MSCSS_PWM0	PWM 0	
	CLK_MSCSS_PWM1	PWM 1	
	CLK_MSCSS_PWM2	PWM 2	
	CLK_MSCSS_PWM3	PWM 3	
	CLK_MSCSS_ADC0_APB	APB side of ADC 0	
	CLK_MSCSS_ADC1_APB	APB side of ADC 1	
	CLK_MSCSS_ADC2_APB	APB side of ADC 2	
	CLK_MSCSS_QEI	quadrature encoder	
BASE_UART_CLK	CLK_UART0	UART 0 interface clock	
	CLK_UART1	UART 1 interface clock	
BASE_ICLK0_CLK	-	CGU1 input clock	
BASE_SPI_CLK	CLK_SPI0	SPI 0 interface clock	
	CLK_SPI1	SPI 1 interface clock	
	CLK_SPI2	SPI 2 interface clock	
BASE_TMR_CLK	CLK_TMR0	timer 0 clock for counter part	
	CLK_TMR1	timer 1 clock for counter part	
	CLK_TMR2	timer 2 clock for counter part	
	CLK_TMR3	timer 3 clock for counter part	
BASE_ADC_CLK	CLK_ADC0	control of ADC 0, capture sample result	
	CLK_ADC1	control of ADC 1, capture sample result	
	CLK_ADC2	control of ADC 2, capture sample result	
-	reserved		
BASE_ICLK1_CLK	-	CGU1 input clock	

[1] This clock is always on (cannot be switched off for system safety reasons)

[2] The boot ROM clock can be turned off to conserve power once the boot process has completed.

[3] In the peripheral subsystem parts of the Timers, watchdog timer, SPI and UART have their own clock source. See Section 6.11 for details.

[4] In the Power Clock and Reset Control subsystem parts of the CGU, RGU, and PMU have their own clock source. See Section 6.14 for details.

[5] The clock should remain activated when system wake-up on timer or UART is required.

- Up to four 32-bit capture channels per timer. These take a snapshot of the timer value when an external signal connected to the TIMERx CAPn input changes state. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs per timer corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Pause input pin (MSCSS timers only).

The timers are designed to count cycles of the clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. They also include capture inputs to trap the timer value when an input signal changes state, optionally generating an interrupt. The core function of the timers consists of a 32 bit prescale counter triggering the 32 bit timer counter. Both counters run on clock CLK_TMRx (x runs from 0 to 3) and all time references are related to the period of this clock. Note that each timer has its individual clock source within the Peripheral SubSystem. In the Modulation and Sampling SubSystem each timer also has its own individual clock source. See section Section 6.14.5 for information on generation of these clocks.

6.11.3.1 Pin description

The four timers in the peripheral subsystem of the LPC2930 have the pins described below. The two timers in the modulation and sampling subsystem have no external pins except for the pause pin on MSCSS timer 1. See Section 6.13.6 for a description of these timers and their associated pins. The timer pins are combined with other functions on the port pins of the LPC2930, see Section 6.10.3. Table 15 shows the timer pins (x runs from 0 to 3).

Table 15. Timer pins

Symbol	Pin name	Direction	Description
TIMERx CAP[0]	CAPx[0]	IN	TIMER x capture input 0
TIMERx CAP[1]	CAPx[1]	IN	TIMER x capture input 1
TIMERx CAP[2]	CAPx[2]	IN	TIMER x capture input 2
TIMERx CAP[3]	CAPx[3]	IN	TIMER x capture input 3
TIMERx MAT[0]	MATx[0]	OUT	TIMER x match output 0
TIMERx MAT[1]	MATx[1]	OUT	TIMER x match output 1
TIMERx MAT[2]	MATx[2]	OUT	TIMER x match output 2
TIMERx MAT[3]	MATx[3]	OUT	TIMER x match output 3

6.11.3.2 Clock description

The timer modules are clocked by two different clocks; CLK_SYS_PESS and CLK_TMRx (x = 0 to 3), see Section 6.6.2. Note that each timer has its own CLK_TMRx branch clock for power management. The frequency of all these clocks is identical as they are derived from the same base clock BASE_CLK_TMR. The register interface towards the system bus is clocked by CLK_SYS_PESS. The timer and prescale counters are clocked by CLK_TMRx.

6.11.4 UARTs

The LPC2930 contains two identical UARTs located at different peripheral base addresses. The key features are:

- 16-byte receive and transmit FIFOs.
- Register locations conform to 550 industry standard.
- Receiver FIFO trigger points at 1 byte, 4 bytes, 8 bytes and 14 bytes.
- Built-in baud rate generator.
- Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.
- Both UARTs equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).

The UART is commonly used to implement a serial interface such as RS232. The LPC2930 contains two industry-standard 550 UARTs with 16-byte transmit and receive FIFOs, but they can also be put into 450 mode without FIFOs.

Remark: The LIN controller can be configured to provide two additional standard UART interfaces (see Section 6.12.2).

6.11.4.1 Pin description

The UART pins are combined with other functions on the port pins of the LPC2930. Table 16 shows the UART pins (x runs from 0 to 1).

Table 16. UART pins

Symbol	Pin name	Direction	Description
UARTx TXD	TXDx	OUT	UART channel x transmit data output
UARTx RXD	RXDx	IN	UART channel x receive data input
UARTx CTS	CTSx	IN	UART channel x Clear To Send (modem)
UARTx DCD	DCDx	IN	UART channel x Data Carrier Detect (modem)
UARTx DSR	DSRx	IN	UART channel x Data Set Ready (modem)
UARTx DTR	DTRx	OUT	UART channel x Data Terminal Ready (modem)
UARTx RI	RIx	IN	UART Ring Indicator (modem)
UARTx RTS	RTSx	OUT	UART Request To Send (modem)
UARTx OUT1	UxOUT1	OUT	UART channel x user designated output 1
UARTx OUT2	UxOUT2	OUT	UART channel x user designated output 2

6.11.4.2 Clock description

The UART modules are clocked by two different clocks; CLK_SYS_PESS and CLK_UARTx (x = 0 to 1), see Section 6.6.2. Note that each UART has its own CLK_UARTx branch clock for power management. The frequency of all CLK_UARTx clocks is identical since they are derived from the same base clock BASE_CLK_UART. The register interface towards the system bus is clocked by CLK_SYS_PESS. The baud generator is clocked by the CLK_UARTx.

6.11.5 Serial peripheral interface (SPI)

The LPC2930 contains three Serial Peripheral Interface modules (SPIs) to allow synchronous serial communication with slave or master peripherals.

The key features are:

- Master or slave operation.
- Each SPI supports up to four slaves in sequential multi-slave operation.
- Supports timer-triggered operation.
- Programmable clock bit rate and prescale based on SPI source clock (BASE_SPI_CLK), independent of system clock.
- Separate transmit and receive FIFO memory buffers; 16 bits wide, 32 locations deep.
- Programmable choice of interface operation: Motorola SPI or Texas Instruments Synchronous Serial Interfaces.
- Programmable data-frame size from 4 to 16 bits.
- Independent masking of transmit FIFO, receive FIFO and receive overrun interrupts.
- Serial clock-rate master mode: fserial_clk $\leq f_{clk(SPI)}/2$.
- Serial clock-rate slave mode: fserial_clk = $f_{clk(SPI)}/4$.
- Internal loopback test mode.

The SPI module can operate in:

- Master mode:
  - Normal transmission mode
  - Sequential slave mode
- Slave mode

6.11.5.1 Functional description

The SPI module is a master or slave interface for synchronous serial communication with peripheral devices that have either Motorola SPI or Texas Instruments Synchronous Serial Interfaces.

The SPI module performs serial-to-parallel conversion on data received from a peripheral device. The transmit and receive paths are buffered with FIFO memories (16 bits wide $\times$ 32 words deep). Serial data is transmitted on pins SDOx and received on pins SDIx.

The SPI module includes a programmable bit-rate clock divider and prescaler to generate the SPI serial clock from the input clock CLK_SPIx.

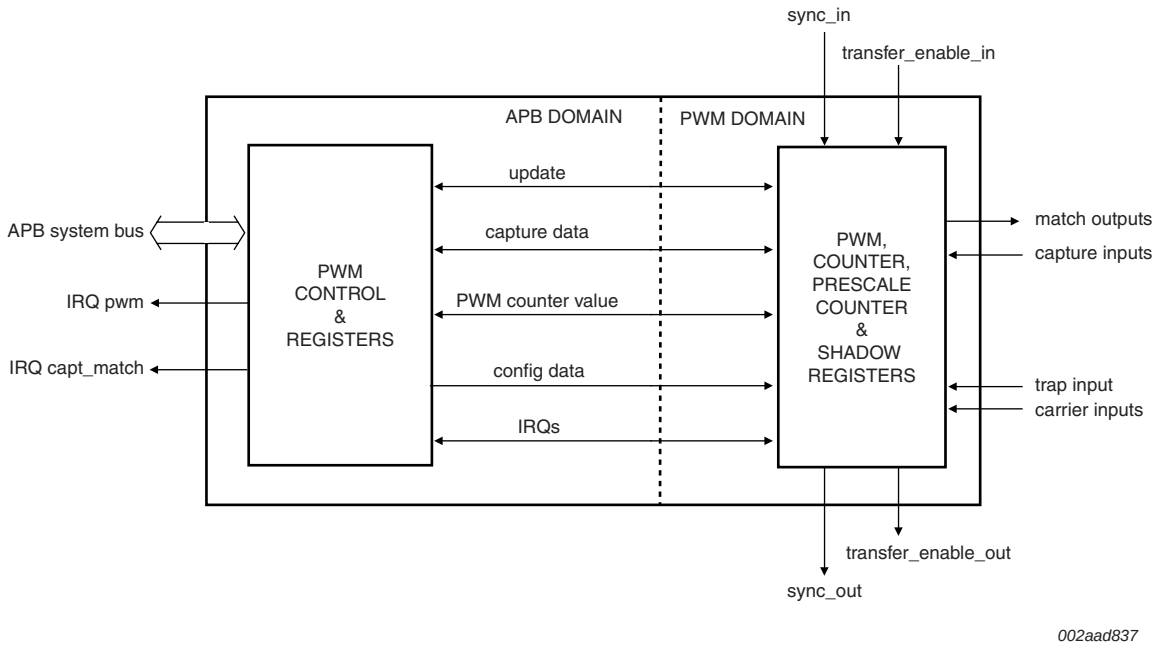


Fig 10. PWM block diagram

The PWM block diagram in Figure 10 shows the basic architecture of each PWM. PWM functionality is split into two major parts, a APB domain and a PWM domain, both of which run on clocks derived from the BASE_MSCSS_CLK. This split into two domains affects behavior from a system-level perspective. The actual PWM and prescale counters are located in the PWM domain but system control takes place in the APB domain.

The actual PWM consists of two counters; a 16-bit prescale counter and a 16-bit PWM counter. The position of the rising and falling edges of the PWM outputs can be programmed individually. The prescale counter allows high system bus frequencies to be scaled down to lower PWM periods. Registers are available to capture the PWM counter values on external events.

Note that in the Modulation and Sampling SubSystem, each PWM has its individual clock source CLK_MSCSS_PWMx (x runs from 0 to 3). Both the prescale and the timer counters within each PWM run on this clock CLK_MSCSS_PWMx, and all time references are related to the period of this clock. See Section 6.14 for information on generation of these clocks.

6.13.5.2 Synchronizing the PWM counters

A mechanism is included to synchronize the PWM period to other PWMs by providing a sync input and a sync output with programmable delay. Several PWMs can be synchronized using the trans_enable_in/trans_enable_out and sync_in/sync_out ports. See Figure 8 for details of the connections of the PWM modules within the MSCSS in the LPC2930. PWM 0 can be master over PWM 1; PWM 1 can be master over PWM 2, etc.

6.13.7.1 Pin description

The QEI module in the MSCSS has the following pins. These are combined with other functions on the port pins of the LPC2930. Table 25 shows the QEI pins.

Table 25. QEI pins

Symbol	Pin name	Direction	Description
QEI0 IDX	IDX0	IN	Index signal. Can be used to reset the position.
QEI0 PHA	PHA0	IN	Sensor signal. Corresponds to PHA in quadrature mode and to direction in clock/direction mode.
QEI0 PHB	PHB0	IN	Sensor signal. Corresponds to PHB in quadrature mode and to clock signal in clock/direction mode.

6.13.7.2 Clock description

The QEI module is clocked by CLK_MSCSS_QEI, see Section 6.6.2. The frequency of this clock is identical to CLK_MSCSS_APB since they are derived from the same base clock BASE_MSCSS_CLK.

If the QEI is not used its CLK_MSCSS_QEI branch clock can be switched off.

6.14 Power, Clock and Reset Control SubSystem (PCRSS)

The Power, Clock and Reset Control Subsystem (PCRSS) in the LPC2930 includes a Clock Generator Unit (CGU), a Reset Generator Unit (RGU) and a Power Management Unit (PMU).

Figure 11 provides an overview of the PCRSS. An AHB-to-DTL bridge controls the communication with the AHB system bus.

Configuration of the CGU0: For every output generator generating the base clocks a choice can be made from the primary and secondary clock generators according to Figure 13.

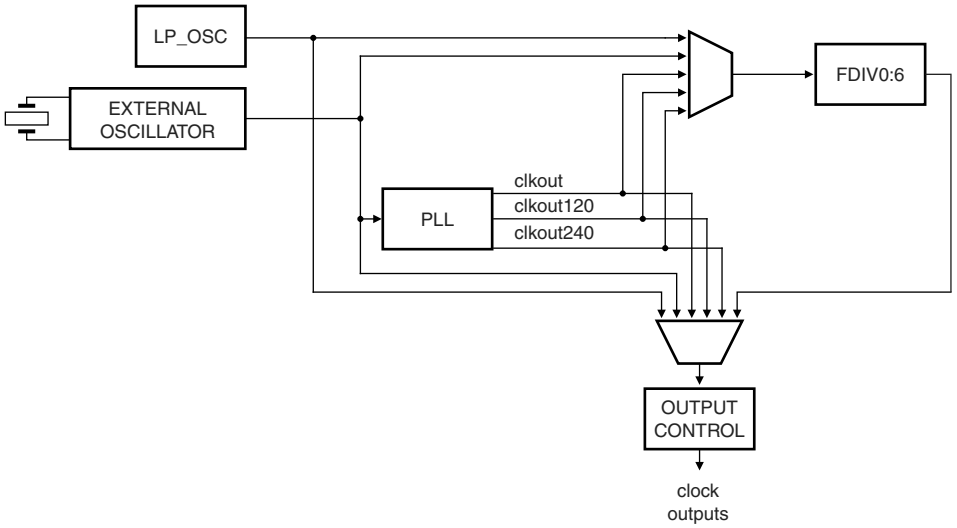


Fig 13. Structure of the clock generation scheme

Any output generator (except for BASE_SAFE_CLK and BASE_PCR_CLK) can be connected to either a fractional divider (FDIV0:6) or to one of the outputs of the PLL or to LP_OSC/crystal oscillator directly. BASE_SAFE_CLK and BASE_PCR_CLK can use only LP_OSC as source.

The fractional dividers can be connected to one of the outputs of the PLL or directly to LP_OSC/crystal Oscillator.

The PLL is connected to the crystal oscillator.

In this way every output generating the base clocks can be configured to get the required clock. Multiple output generators can be connected to the same primary or secondary clock source, and multiple secondary clock sources can be connected to the same PLL output or primary clock source.

Invalid selections/programming - connecting the PLL to an FDIV or to one of the PLL outputs itself for example - will be blocked by hardware. The control register will not be written, the previous value will be kept, although all other fields will be written with new data. This prevents clocks being blocked by incorrect programming.

Default Clock Sources: Every secondary clock generator or output generator is connected to LP_OSC at reset. In this way the device runs at a low frequency after reset. It is recommended to switch BASE_SYS_CLK to a high-frequency clock generator as (one of) the first step(s) in the boot code after verifying that the high-frequency clock generator is running.

Clock Activity Detection: Clocks that are inactive are automatically regarded as invalid, and values of ‘CLK_SEL’ that would select those clocks are masked and not written to the control registers. This is accomplished by adding a clock detector to every clock

- Automatic reset stretching and release
- Monitor function to trace resets back to source
- Register write-protection mechanism to prevent unintentional resets

6.14.4.1 Functional description

Each reset output is defined as a combination of reset input sources including the external reset input pins and internal power-on reset, see Table 29. The first five resets listed in this table form a sort of cascade to provide the multiple levels of impact that a reset may have. The combined input sources are logically OR-ed together so that activating any of the listed reset sources causes the output to go active.

Table 29. Reset output configuration

Reset output	Reset source	Parts of the device reset when activated
POR_RST	power-on reset module	LP_OSC; source for RGU_RST
RGU_RST	POR_RST, $\overline{\text{RST}}$ pin	RGU internal; source for PCR_RST
PCR_RST	RGU_RST, WATCHDOG	PCR internal; source for COLD_RST
COLD_RST	PCR_RST	parts with COLD_RST as reset source below
WARM_RST	COLD_RST	parts with WARM_RST as reset source below
SCU_RST	COLD_RST	SCU
CFID_RST	COLD_RST	CFID
EMC_RST	COLD_RST	embedded SRAM-Memory Controller
SMC_RST	COLD_RST	external Static-Memory Controller (SMC)
GESS_A2V_RST	WARM_RST	GeSS AHB-to-APB bridge
PESS_A2V_RST	WARM_RST	PeSS AHB-to-APB bridge
GPIO_RST	WARM_RST	all GPIO modules
UART_RST	WARM_RST	all UART modules
TMR_RST	WARM_RST	all Timer modules in PeSS
SPI_RST	WARM_RST	all SPI modules
IVNSS_A2V_RST	WARM_RST	IVNSS AHB-to-APB bridge
IVNSS_CAN_RST	WARM_RST	all CAN modules including Acceptance filter
IVNSS_LIN_RST	WARM_RST	all LIN modules
MSCSS_A2V_RST	WARM_RST	MSCSS AHB to APB bridge
MSCSS_PWM_RST	WARM_RST	all PWM modules
MSCSS_ADC_RST	WARM_RST	all ADC modules
MSCSS_TMR_RST	WARM_RST	all Timer modules in MSCSS
I2C_RST	WARM_RST	all I^2C modules
QEI_RST	WARM_RST	Quadrature encoder
DMA_RST	WARM_RST	GPDMA controller
USB_RST	WARM_RST	USB controller
VIC_RST	WARM_RST	Vectored Interrupt Controller (VIC)
AHB_RST	WARM_RST	CPU and AHB Bus infrastructure

6.14.4.2 Pin description

The RGU module in the LPC2930 has the following pins. Table 30 shows the RGU pins.

Table 33. Static characteristics *…continued*

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; $V_{DDA(ADC5V0)}$ = 3.0 V to 5.5 V; T_{vj} = −40 °C to +85 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	all port pins, $\overline{RST}$, $\overline{TRST}$, TDI, JTAGSEL, TMS, TCK		2.0	-	-	V
V_{IL}	LOW-level input voltage	all port pins, $\overline{RST}$, $\overline{TRST}$, TDI, JTAGSEL, TMS, TCK		-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
I_{LIH}	HIGH-level input leakage current			-	-	1	μA
I_{LIL}	LOW-level input leakage current			-	-	1	μA
$I_{I(pd)}$	pull-down input current	all port pins, V_I = 3.3 V; V_I = 5.5 V; see Figure 23		25	50	100	μA
$I_{I(pu)}$	pull-up input current	all port pins, $\overline{RST}$, $\overline{TRST}$, TDI, JTAGSEL, TMS: V_I = 0 V; V_I > 3.6 V is not allowed; see Figure 24		−25	−50	−115	μA
C_i	input capacitance		[8]	-	3	8	pF
Output pins and I/O pins configured as output							
V_O	output voltage			0	-	$V_{DD(IO)}$	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA; see Figure 22		$V_{DD(IO)}$ −0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; see Figure 21		-	-	0.4	V
C_L	load capacitance			-	-	25	pF
USB pins USB_D+ and USB_D−							
Input characteristics							
V_{IH}	HIGH-level input voltage			1.5	-	-	V
V_{IL}	LOW-level input voltage			-	-	1.3	V
V_{hys}	hysteresis voltage			0.4	-	-	V
Output characteristics							
Z_o	output impedance	with 33 Ω series resistor		36.0	-	44.1	Ω
V_{OH}	HIGH-level output voltage	(driven) for low-/full-speed; R_L of 15 kΩ to GND		2.9	-	3.5	V
V_{OL}	LOW-level output voltage	(driven) for low-/full-speed; with 1.5 kΩ resistor to 3.6 V external pull-up		-	-	0.18	V

Table 33. Static characteristics *…continued*

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; $V_{DDA(ADC5V0)}$ = 3.0 V to 5.5 V; T_{vj} = −40 °C to +85 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{OH}	HIGH-level output current	at V_{OH} = $V_{DD(IO)}$ − 0.3 V; without 33 Ω external series resistor		20.8	-	41.7	mA
		at V_{OH} = $V_{DD(IO)}$ − 0.3 V; with 33 Ω external series resistor		4.8	-	5.3	mA
I_{OL}	LOW-level output current	at V_{OL} = 0.3 V; without 33 Ω external series resistor		26.7	-	57.2	mA
		at V_{OL} = 0.3 V; with 33 Ω external series resistor		5.0	-	5.5	mA
I_{OHS}	HIGH-level short-circuit output current	drive high; pad connected to ground		-	-	90.0	mA
I_{OLS}	LOW-level short-circuit output current	drive high; pad connected to $V_{DD(IO)}$		-	-	95.1	mA
Oscillator							
V_{XIN_OSC}	voltage on pin XIN_OSC			0	-	1.8	V
$R_{s(xtal)}$	crystal series resistance	f_{osc} = 10 MHz to 15 MHz	[9]				
		C_{xtal} = 10 pF; C_{ext} = 18 pF		-	-	160	Ω
		C_{xtal} = 20 pF; C_{ext} = 39 pF		-	-	60	Ω
		f_{osc} = 15 MHz to 20 MHz	[9]				
		C_{xtal} = 10 pF; C_{ext} = 18 pF		-	-	80	Ω
C_i	input capacitance	of XIN_OSC	[10]	-	-	2	pF
Power-up reset							
$V_{trip(high)}$	high trip level voltage		[11]	1.1	1.4	1.6	V
$V_{trip(low)}$	low trip level voltage		[11]	1.0	1.3	1.5	V
$V_{trip(dif)}$	difference between high and low trip level voltage		[11]	50	120	180	mV

[1] All parameters are guaranteed over the virtual junction temperature range by design. Pre-testing is performed at T_{amb} = 85 °C on wafer level. Cased products are tested at T_{amb} = 25 °C (final testing). Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power-supply voltage range.

[2] The Boot ROM can be powered down by setting the FS_PD bit in the FCTR register for additional power savings in active mode (see *LPC29xx user manual UM10316)*.

[3] Leakage current is exponential to temperature; worst-case value is at 85 °C T_{vj}. All clocks off. Analog modules powered down.

[4] $V_{DDA(ADC3V3)}$ must correlate with $V_{DDA(ADC5V0)}$: $V_{DDA(ADC3V3)}$ = $V_{DDA(ADC5V0)}$ / 1.5.

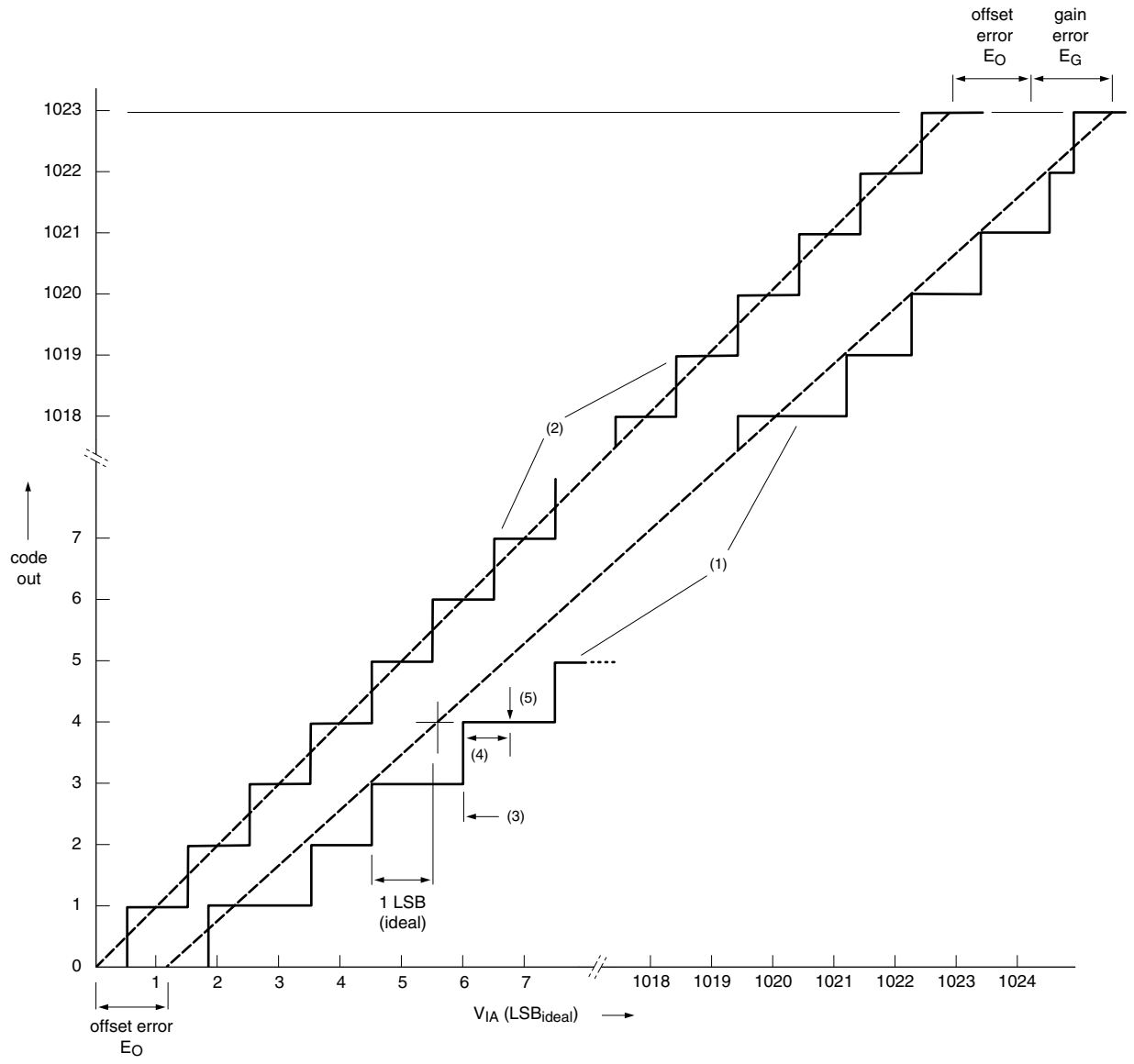
[5] $V_{DDA(ADC5V0)}$ must correlate with $V_{DDA(ADC3V3)}$: $V_{DDA(ADC5V0)}$ = $V_{DDA(ADC3V3)}$ × 1.5.

[6] Not 5 V-tolerant when pull-up is on.

[7] For I/O Port 0, the maximum input voltage is defined by $V_{I(ADC)}$.

[8] For Port 0, pin 0 to pin 15 add maximum 1.5 pF for input capacitance to ADC. For Port 0, pin 16 to pin 31 add maximum 1.0 pF for input capacitance to ADC.

[9] C_{xtal} is crystal load capacitance and C_{ext} are the two external load capacitors.



(1) Example of an actual transfer curve.

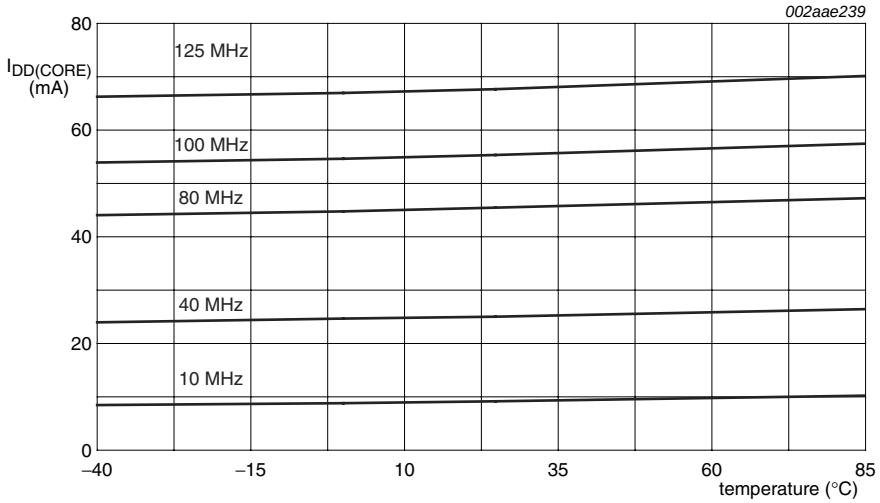
(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

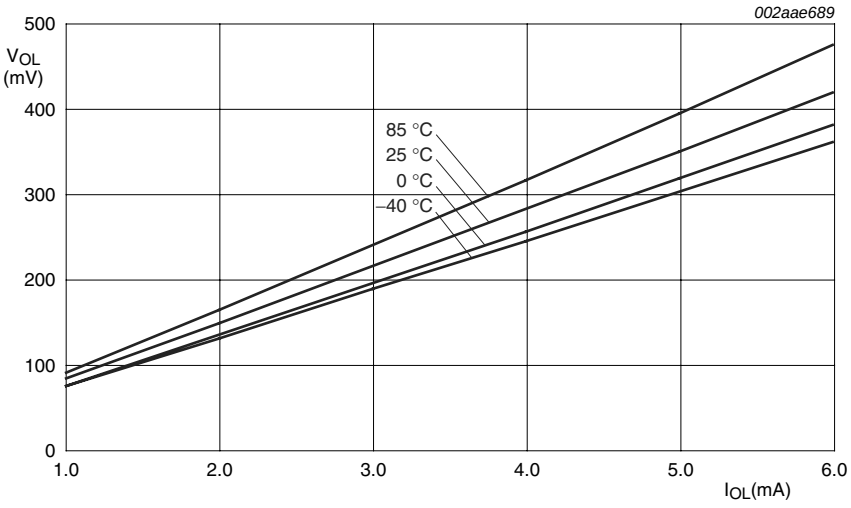
Fig 17. ADC characteristics



Conditions: active mode entered executing code from external memory; core voltage 1.8 V; all peripherals enabled but not configured to run.

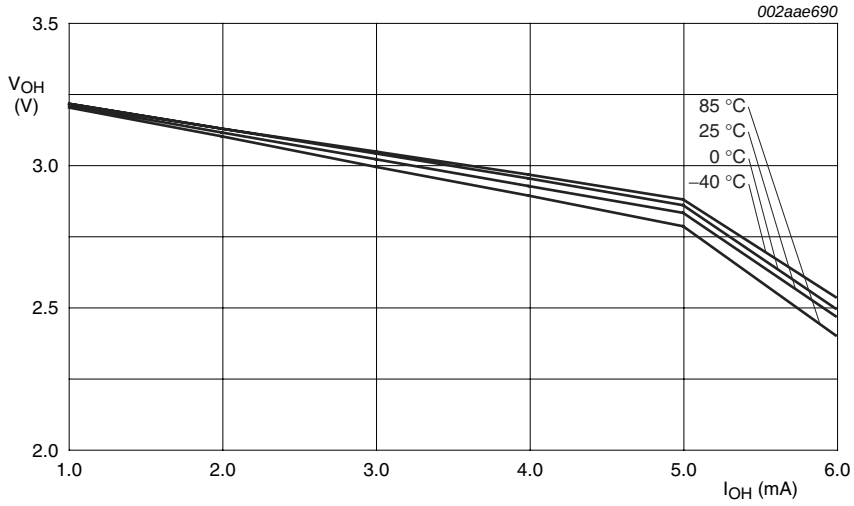
Fig 20. $I_{DD(CORE)}$ at different temperatures (active mode)

8.2 Electrical pin characteristics



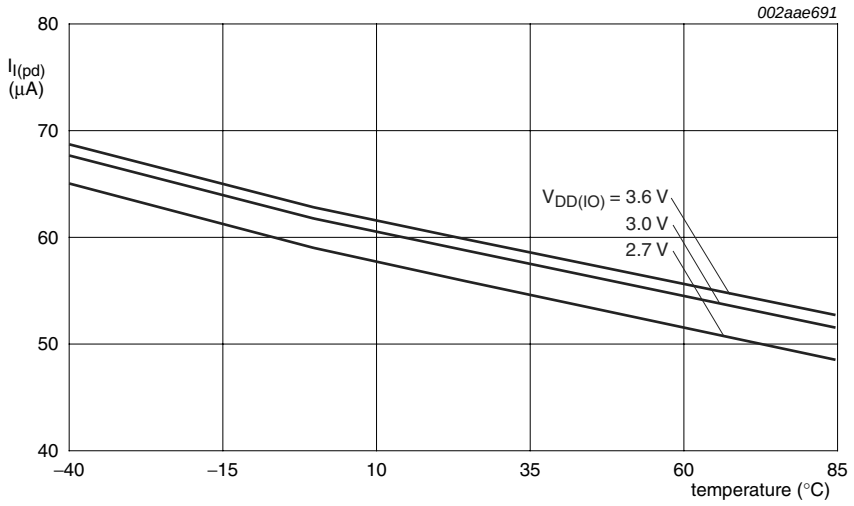
$V_{DD(IO)}$ = 3.3 V.

Fig 21. Typical LOW-level output voltage versus LOW-level output current



$V_{DD(IO)}$ = 3.3 V.

Fig 22. Typical HIGH-level output voltage versus HIGH-level output current



V_I = 3.3 V.

Fig 23. Typical pull-down current versus temperature

9.3 Dynamic characteristics: I²C-bus interface

Table 37. Dynamic characteristic: I²C-bus pins

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$[3]	-	-	ns

[1] All parameters are guaranteed over the virtual junction temperature range by design. Pre-testing is performed at T_{amb} = 85 °C ambient temperature on wafer level. Cased products are tested at T_{amb} = 25 °C (final testing). Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

9.4 Dynamic characteristics: SPI

Table 38. Dynamic characteristics of SPI pins

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; $V_{DDA(ADC5V0)}$ = 3.0 V to 5.5 V; T_{vj} = −40 °C to +85 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SPI}	SPI operating frequency	master operation	$^1/_{65024} f_{clk(SPI)}$	-	$^1/_2 f_{clk(SPI)}$	MHz
		slave operation	$^1/_{65024} f_{clk(SPI)}$	-	$^1/_4 f_{clk(SPI)}$	MHz
$t_{su(SPI\_MISO)}$	SPI_MISO set-up time	T_{amb} = 25 °C; measured in SPI Master mode; see Figure 27	-	11	-	ns

[1] All parameters are guaranteed over the virtual junction temperature range by design. Pre-testing is performed at T_{amb} = 85 °C ambient temperature on wafer level. Cased products are tested at T_{amb} = 25 °C (final testing). Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power supply voltage range.

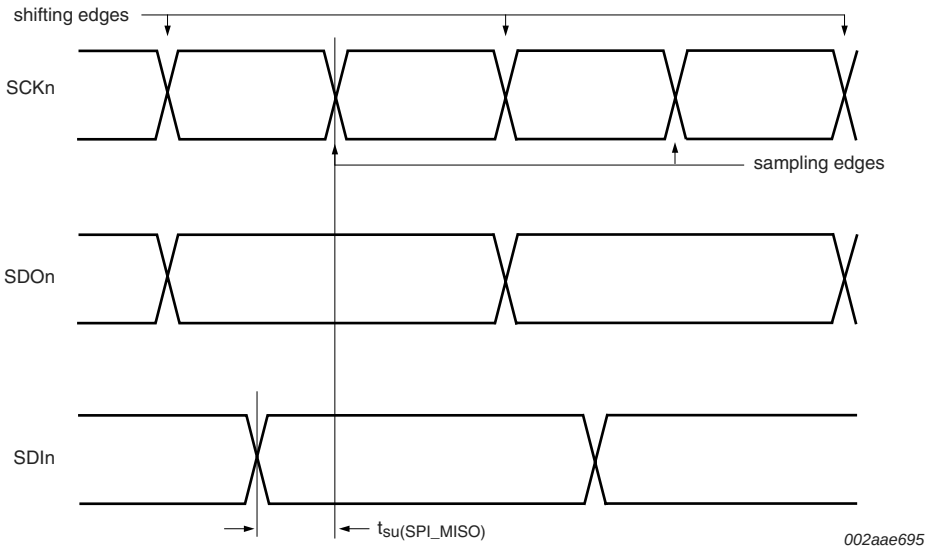


Fig 27. SPI data input set-up time in SSP Master mode

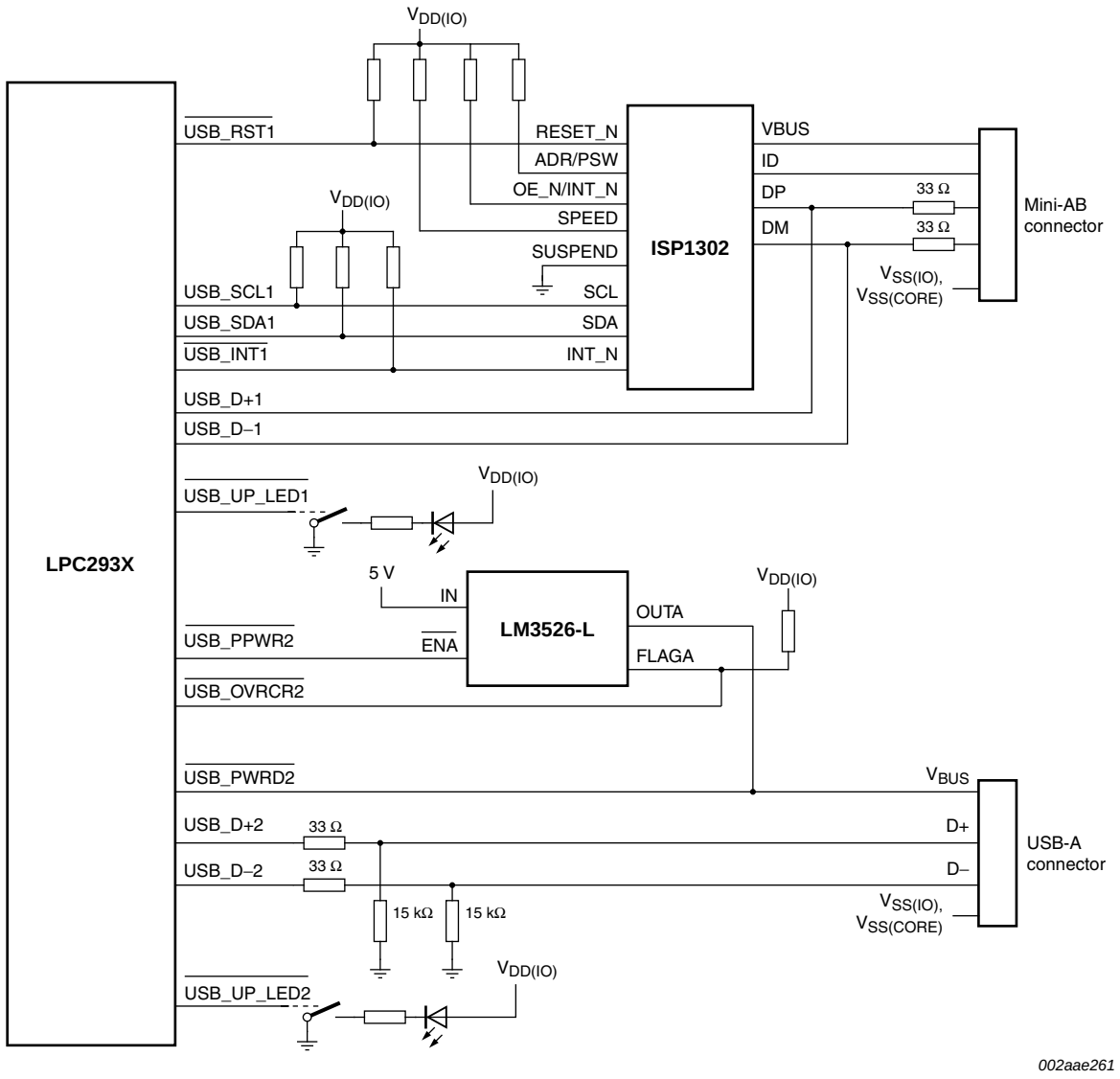


Fig 34. LPC2930 USB OTG port configuration: USB port 1 OTG dual-role device, USB port 2 host

18. Contents

continued >>