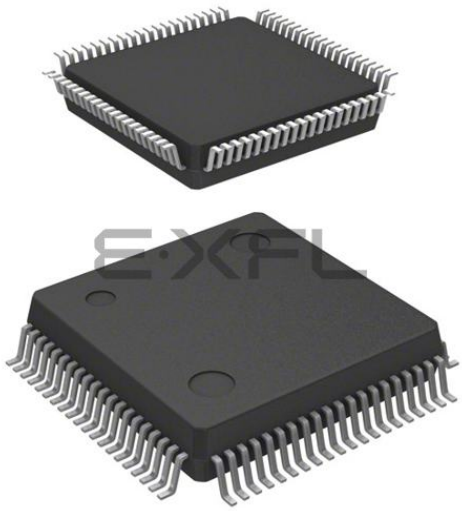

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300
Core Size	8-Bit
Speed	16MHz
Connectivity	Host Interface, I²C, SCI
Peripherals	POR, PWM, WDT
Number of I/O	74
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f3337sf16v

2.5.3 Logic Operations

Table 2.6 describes the four instructions that perform logic operations. See figure 2.6 in section 2.5.4, Shift Operations, for their object codes.

Table 2.6 Logic Operation Instructions

Instruction	Size*	Function
AND	B	Rd ∧ Rs → Rd, Rd ∧ #imm → Rd Performs a logical AND operation on a general register and another general register or immediate data.
OR	B	Rd ∨ Rs → Rd, Rd ∨ #imm → Rd Performs a logical OR operation on a general register and another general register or immediate data.
XOR	B	Rd ⊕ Rs → Rd, Rd ⊕ #imm → Rd Performs a logical exclusive OR operation on a general register and another general register or immediate data.
NOT	B	¬ (Rd) → (Rd) Obtains the one's complement (logical complement) of general register contents.

Note: * Size: Operand size
B: Byte

2.5.4 Shift Operations

Table 2.7 describes the eight shift instructions. Figure 2.6 shows the object code formats of the arithmetic, logic, and shift instructions.

Table 2.7 Shift Instructions

Instruction	Size*	Function
SHAL	B	Rd shift → Rd
SHAR		Performs an arithmetic shift operation on general register contents.
SHLL	B	Rd shift → Rd
SHLR		Performs a logical shift operation on general register contents.
ROTL	B	Rd rotate → Rd
ROTR		Rotates general register contents.
ROTXL	B	Rd rotate through carry → Rd
ROTXR		Rotates general register contents through the C (carry) bit.

Note: * Size: Operand size
B: Byte

Bit 0—RAM Enable (RAME): Enables or disables the on-chip RAM. The RAME bit is initialized by a reset, but is not initialized in the software standby mode.

Bit 0: RAME	Description	
0	The on-chip RAM is disabled.	
1	The on-chip RAM is enabled.	(Initial value)

3.3 Mode Control Register (MDCR)

Bit	7	6	5	4	3	2	1	0
	EXPE*1	—	—	—	—	—	MDS1	MDS0
Initial value	—*2	1	1	0	0	1	—*2	—*2
Read/Write	R/W*2	—	—	—	—	—	R	R

Notes: *1 H8/3337SF (S-mask model, single-power-supply on-chip flash memory version) only. Otherwise, this is a reserved bit that is always read as 1.

*2 Determined by the mode pins (MD_1 and MD_0).

The mode control register (MDCR) is an 8-bit register that indicates the operating mode of the chip.

Bit 7—Expanded Mode Enable (EXPE): Functions only in the H8/3337SF (S-mask model, single-power-supply on-chip flash memory version). For details, see section 21.1.6, Mode Control Register (MDCR).

In models other than the H8/3337SF, this is a reserved bit that cannot be modified and is always read as 1.

Bits 6 and 5—Reserved: These bits cannot be modified and are always read as 1.

Bits 4 and 3—Reserved: These bits cannot be modified and are always read as 0.

Bit 2—Reserved: This bit cannot be modified and is always read as 1.

Bits 1 and 0—Mode Select 1 and 0 (MDS1 and MDS0): These bits indicate the values of the mode pins (MD_1 and MD_0), thereby indicating the current operating mode of the chip. MDS1 corresponds to MD_1 and MDS0 to MD_0. These bits can be read but not written. When the mode control register is read, the levels at the mode pins (MD_1 and MD_0) are latched in these bits.

3.4 Address Space Map in Each Operating Mode

Figures 3.1 to 3.3 show memory maps of the H8/3337Y, H8/3336Y, H8/3334Y, H8/3397, H8/3396, and H8/3394 in modes 1, 2, and 3.

Bit 5—Input Capture Flag C (ICFC): This status bit is set to 1 to flag input of a rising or falling edge of FTIC as selected by the IEDGC bit. When BUFEA = 0, this indicates capture of the FRC count in ICRC. When BUFEA = 1, however, the FRC count is not captured, so ICFC becomes simply an external interrupt flag. In other words, the buffer mode frees FTIC for use as a general-purpose interrupt signal (which can be enabled or disabled by the ICICE bit).

ICFC must be cleared by software. It is set by hardware, however, and cannot be set by software.

Bit 5: ICFC	Description
0	To clear ICFC, the CPU must read ICFC after it has been set to 1, then write a 0 in this bit. (Initial value)
1	This bit is set to 1 when an FTIC input signal is received.

Bit 4—Input Capture Flag D (ICFD): This status bit is set to 1 to flag input of a rising or falling edge of FTID as selected by the IEDGD bit. When BUFEB = 0, this indicates capture of the FRC count in ICRD. When BUFEB = 1, however, the FRC count is not captured, so ICFD becomes simply an external interrupt flag. In other words, the buffer mode frees FTID for use as a general-purpose interrupt signal (which can be enabled or disabled by the ICIDE bit).

ICFD must be cleared by software. It is set by hardware, however, and cannot be set by software.

Bit 4: ICFD	Description
0	To clear ICFD, the CPU must read ICFD after it has been set to 1, then write a 0 in this bit. (Initial value)
1	This bit is set to 1 when an FTID input signal is received.

Bit 3—Output Compare Flag A (OCFA): This status flag is set to 1 when the FRC value matches the OCRA value. This flag must be cleared by software. It is set by hardware, however, and cannot be set by software.

Bit 3: OCFA	Description
0	To clear OCFA, the CPU must read OCFA after it has been set to 1, then write a 0 in this bit. (Initial value)
1	This bit is set to 1 when FRC = OCRA.

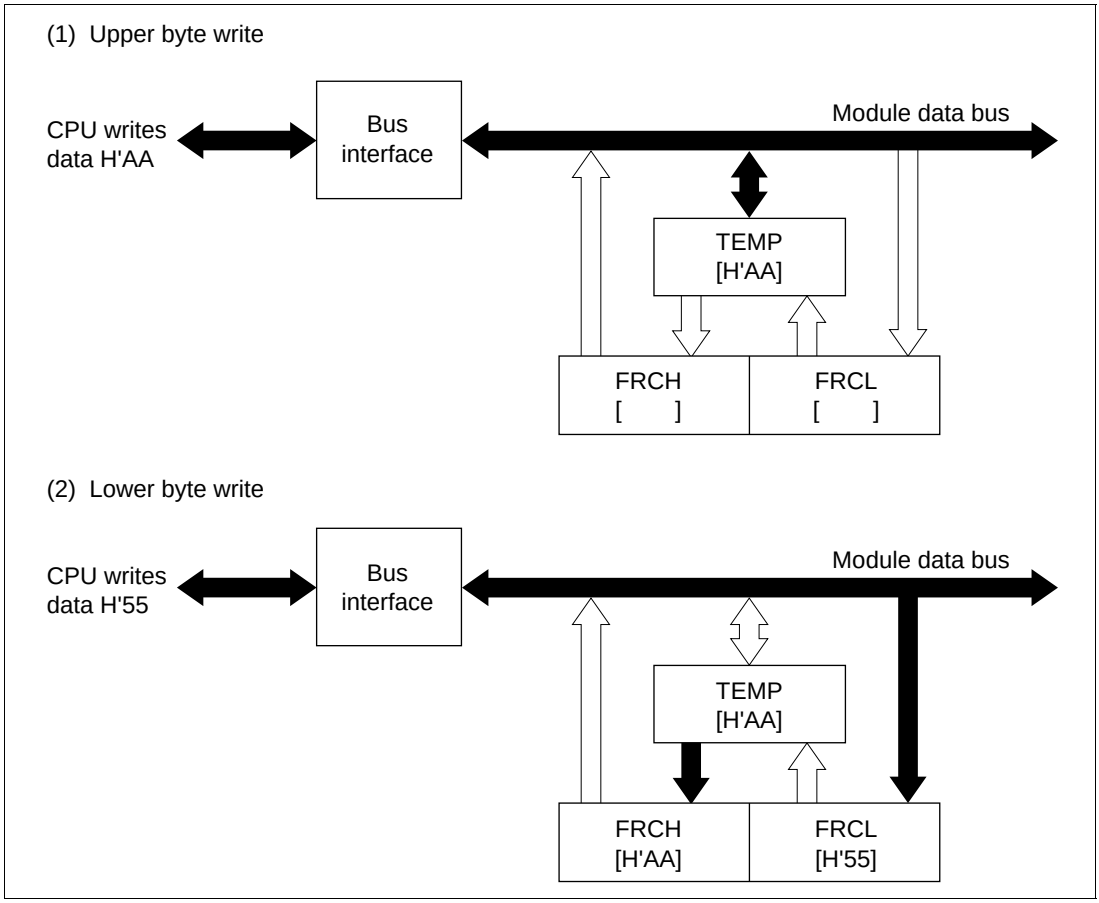

Figure 8.3 (a) Write Access to FRC (when CPU Writes H'AA55)

9.2 Register Descriptions

9.2.1 Timer Counter (TCNT)

Bit	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Each timer counter (TCNT) is an 8-bit up-counter that increments on a pulse generated from an internal or external clock source selected by clock select bits 2 to 0 (CKS2 to CKS0) of the timer control register (TCR). The CPU can always read or write the timer counter.

The timer counter can be cleared by an external reset input or by an internal compare-match signal generated at a compare-match event. Clock clear bits 1 and 0 (CCLR1 and CCLR0) of the timer control register select the method of clearing.

When a timer counter overflows from H'FF to H'00, the overflow flag (OVF) in the timer control/status register (TCSR) is set to 1.

The timer counters are initialized to H'00 by a reset and in the standby modes.

9.2.2 Time Constant Registers A and B (TCORA and TCORB)

Bit	7	6	5	4	3	2	1	0
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TCORA and TCORB are 8-bit readable/writable registers. The timer count is continually compared with the constants written in these registers (except during the T_3 state of a write cycle to TCORA or TCORB). When a match is detected, the corresponding compare-match flag (CMFA or CMFB) is set in the timer control/status register (TCSR).

The timer output signal is controlled by these compare-match signals as specified by output select bits 3 to 0 (OS3 to OS0) in the timer control/status register (TCSR).

TCORA and TCORB are initialized to H'FF by a reset and in the standby modes.

Section 10 PWM Timers

10.1 Overview

The H8/3337 Series and H8/3397 Series have an on-chip pulse-width modulation (PWM) timer module with two independent channels (PWM0 and PWM1). Both channels are functionally identical. Each PWM channel generates a rectangular output pulse with a duty cycle of 0 to 100%. The duty cycle is specified in an 8-bit duty register (DTR).

10.1.1 Features

The PWM timer module has the following features:

- Selection of eight clock sources
- Duty cycles from 0 to 100% with 1/250 resolution
- Direct or inverted PWM output, and software enable/disable control

6. To continue transmitting, write the next transmit data in ICDR. Transmission of the next byte will begin in synchronization with the internal clock.

Steps 4 to 6 can be repeated to transmit data continuously. To end the transmission, write 0 in BBSY and 0 in SCP in ICSR. This generates a stop condition by causing a low-to-high transition of SDA while SCL is high.

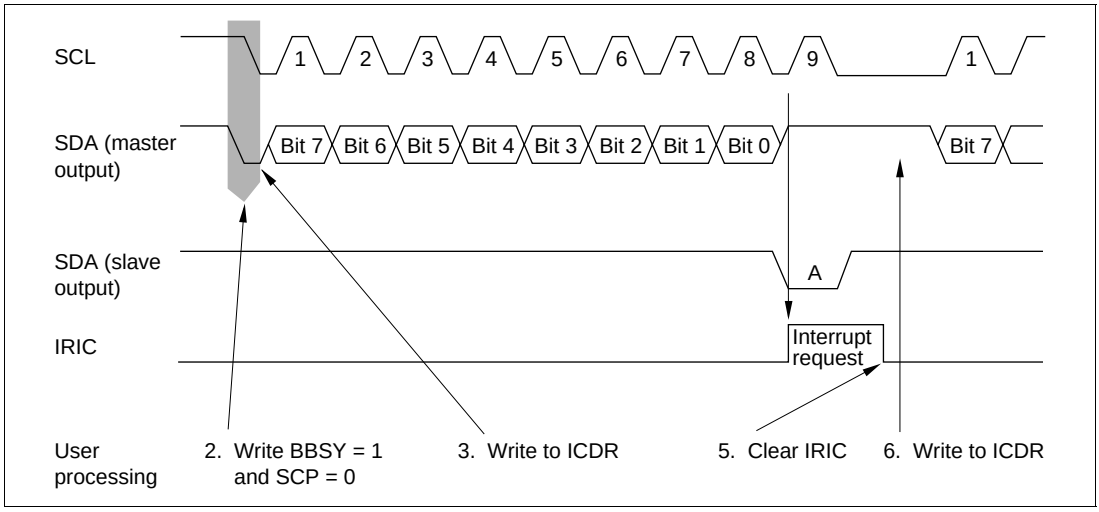

Figure 13.6 Operation Timing in Master Transmit Mode (MLS = WAIT = ACK = 0)

14.2.7 Output Data Register 2 (ODR2)

Bit	7	6	5	4	3	2	1	0
	ODR7	ODR6	ODR5	ODR4	ODR3	ODR2	ODR1	ODR0
Initial value	—	—	—	—	—	—	—	—
Slave Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Host Read/Write	R	R	R	R	R	R	R	R

ODR2 is an 8-bit read/write register to the slave processor, and an 8-bit read-only register to the host processor. The ODR2 contents are output on the host data bus when HA_0 is low, $\overline{CS}_2$ is low, and $\overline{IOR}$ is low.

The initial values of ODR2 after a reset or standby are undetermined.

14.2.8 Status Register 2 (STR2)

Bit	7	6	5	4	3	2	1	0
	DBU	DBU	DBU	DBU	C/$\overline{D}$	DBU	IBF	OBF
Initial value	0	0	0	0	0	0	0	0
Slave Read/Write	R/W	R/W	R/W	R/W	R	R/W	R	R
Host Read/Write	R	R	R	R	R	R	R	R

STR2 is an 8-bit register that indicates status information during host interface processing. Bits 3, 1, and 0 are read-only bits to both the host and slave processors.

STR2 is initialized to H'00 by a reset and in hardware standby mode.

Bits 7 to 4 and Bit 2—Defined by User (DBU): The user can use these bits as necessary.

Bit 3—Command/Data (C/$\overline{D}$): Receives the HA_0 input when the host processor writes to IDR2, and indicates whether IDR2 contains data or a command.

Bit 3: C/$\overline{D}$	Description	
0	Contents of IDR2 are data	(Initial value)
1	Contents of IDR2 are a command	

```
            CMP.B     #H'32,    R6L     ; Program-verify executed 50 times?
            BEQ       NGEND             ; If program-verify executed 50 times, branch to NGEND
            BRA       PRGMS             ; Program again

PVOK:       BCLR      #2,       @FLMCR:8      ;       Clear PV bit
            MOV.B     #H'00,    R6L     ;
            MOV.B     R6L,      @EBR*:8 ;     Clear EBR*

            One byte programmed

NGEND:      Programming error
```

19.4.4 Erase Mode

To erase the flash memory, follow the erasing algorithm shown in figure 19.11. This erasing algorithm can erase data without subjecting the device to voltage stress or impairing the reliability of programmed data.

To erase flash memory, before starting to erase, first place all memory data in all blocks to be erased in the programmed state (program all memory data to H'00). If all memory data is not in the programmed state, follow the sequence described later (figure 18-17) to program the memory data to zero. Select the flash memory areas to be erased with erase block registers 1 and 2 (EBR1 and EBR2). Next set the E bit in FLMCR, selecting erase mode. The erase time is the time during which the E bit is set. To prevent overerasing, use a software timer to divide the erase time into repeated 10 ms intervals, and perform erase operations a maximum of 3000 times so that the total erase time does not exceed 30 seconds. Overerasing, due to program runaway for example, can give memory cells a negative threshold voltage and cause them to operate incorrectly. Before selecting erase mode, set up the watchdog timer so as to prevent overerasing.

19.4.5 Erase-Verify Mode

In erase-verify mode, after data has been erased, it is read to check that it has been erased correctly. After the erase time has elapsed, exit erase mode (clear the E bit to 0) and select erase-verify mode (set the EV bit to 1). Before reading data in erase-verify mode, write H'FF dummy data to the address to be read. This dummy write applies an erase-verify voltage to the memory cells at the latched address. If the flash memory is read in this state, the data at the latched address will be read. After the dummy write, wait 2 µs or more before reading. When performing the initial dummy write, wait 4 µs or more after selecting erase-verify mode. If the read data has been successfully erased, perform an erase-verify (dummy write, wait 2 µs or more, then read) for the next address. If the read data has not been erased, select erase mode again and repeat the same erase and erase-verify sequence through the last address. Do not repeat the erase and erase-verify sequence more than 3000 times, however.

19.5 Flash Memory Emulation by RAM

Erasing and programming flash memory takes time, which can make it difficult to tune parameters and other data in real time. If necessary, real-time updates of flash memory can be emulated by overlapping the small-block flash-memory area with part of the RAM (H'FC00 to H'FD7F). This RAM reassignment is performed using bits 7 and 6 of the wait-state control register (WSCR).

After a flash memory area has been overlapped by RAM, the RAM area can be accessed from two address areas: the overlapped flash memory area, and the original RAM area (H'FC00 to H'FD7F). Table 19.11 indicates how to reassign RAM.

Wait-State Control Register (WSCR)[*2]

Bit	7	6	5	4	3	2	1	0
	RAMS	RAM0	CKDBL	—	WMS1	WMS0	WC1	WC0
Initial value[*1]	0	0	0	0	1	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Notes: *1 WSCR is initialized by a reset and in hardware standby mode. It is not initialized in software standby mode.

*2 For details of WSCR settings, see section 19.2.4, Wait-State Control Register (WSCR).

Table 19.11 RAM Area Selection

Bit 7: RAMS	Bit 6: RAMO	RAM Area	ROM Area
0	0	None	—
	1	H'FC80 to H'FCFF	H'0080 to H'00FF
1	0	H'FC80 to H'FD7F	H'0080 to H'017F
	1	H'FC00 to H'FC7F	H'0000 to H'007F

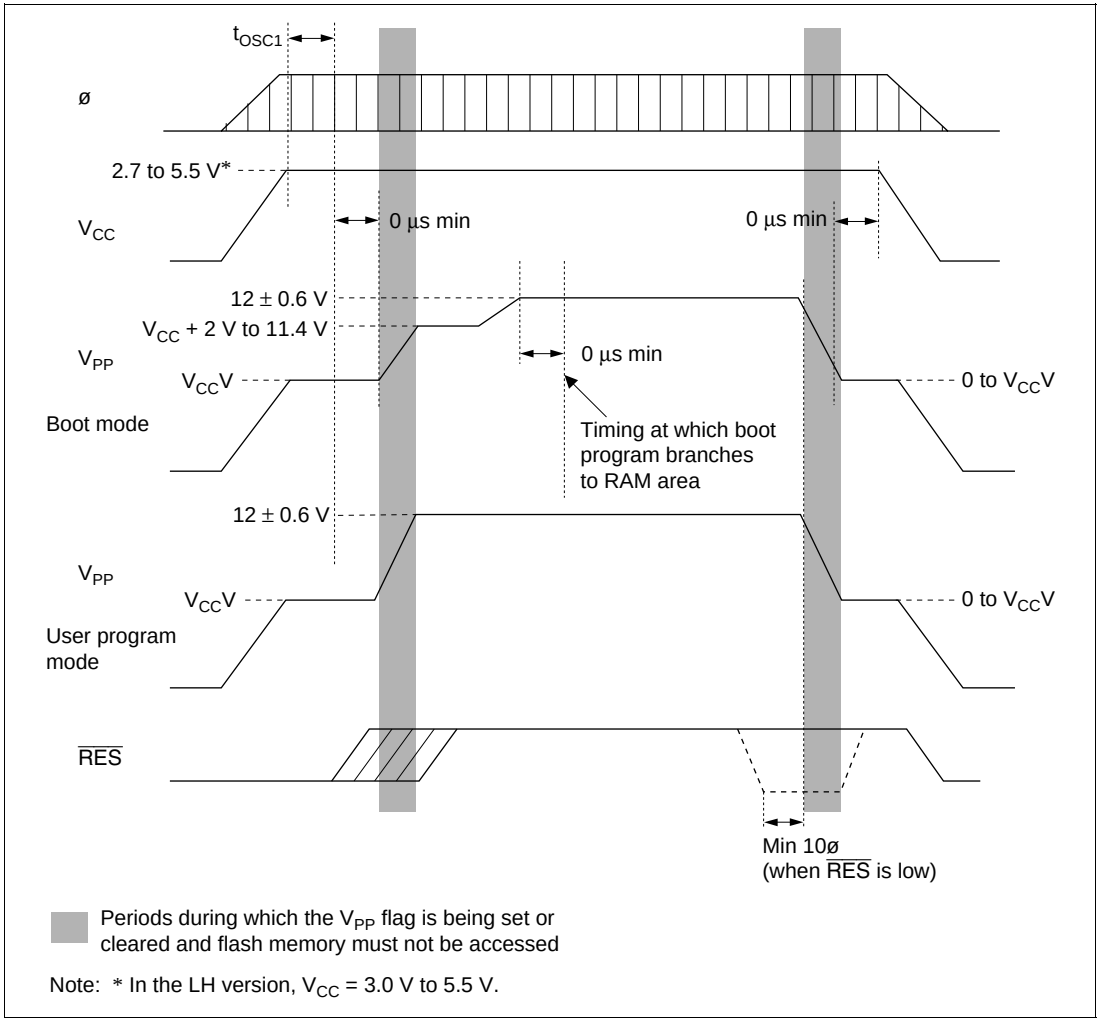

Figure 19.20 V_{PP} Power-On and Power-Off Timing

(6) Do not apply 12 V to the FV_{PP} pin during normal operation.

To prevent accidental programming or erasing due to microcontroller program runaway etc., apply 12 V to the V_{PP} pin only when the flash memory is programmed or erased, or when flash memory is emulated by RAM. Overprogramming or overerasing due to program runaway can cause memory cells to malfunction. Avoid system configurations in which 12 V is always applied to the FV_{PP} pin.

While 12 V is applied, the watchdog timer should be running and enabled to halt runaway program execution, so that program runaway will not lead to overprogramming or overerasing.

20.2.4 Wait-State Control Register (WSCR)

WSCR is an 8-bit readable/writable register that enables flash-memory updates to be emulated in RAM. It also controls frequency division of clock signals supplied to the on-chip supporting modules and insertion of wait states by the wait-state controller.

WSCR is initialized to H'08 by a reset and in hardware standby mode. It is not initialized in software standby mode.

Bit	7	6	5	4	3	2	1	0
	RAMS	RAM0	CKDBL	—	WMS1	WMS0	WC1	WC0
Initial value	0	0	0	0	1	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 and 6—RAM Select and RAM0 (RAMS and RAM0): These bits are used to reassign an area to RAM (see table 20.5). These bits are write-enabled and their initial value is 0. They are initialized by a reset and in hardware standby mode. They are not initialized in software standby mode.

If only one of bits 7 and 6 is set, part of the RAM area can be overlapped onto the small-block flash memory area. In that case, access is to RAM, not flash memory, and all flash memory blocks are write/erase-protected (emulation protect[*1]). In this state, the mode cannot be changed to program or erase mode, even if the P bit or E bit in the flash memory control register (FLMCR) is set (although verify mode can be selected). Therefore, clear both of bits 7 and 6 before programming or erasing the flash memory area.

If both of bits 7 and 6 are set, part of the RAM area can be overlapped onto the small-block flash memory area, but this overlapping begins only when an interrupt signal is input while 12 V is being applied to the FV_{PP} pin. Up until that point, flash memory is accessed. Use this setting for interrupt handling while flash memory is being programmed or erased.[*2]

Table 20.5 RAM Area Reassignment[*3]

Bit 7: RAMS	Bit 6: RAM0	RAM Area	ROM Area
0	0	None	—
	1	H'F880 to H'F8FF	H'0080 to H'00FF
1	0	H'F880 to H'F97F	H'0080 to H'017F
	1	H'F800 to H'F87F	H'0000 to H'007F

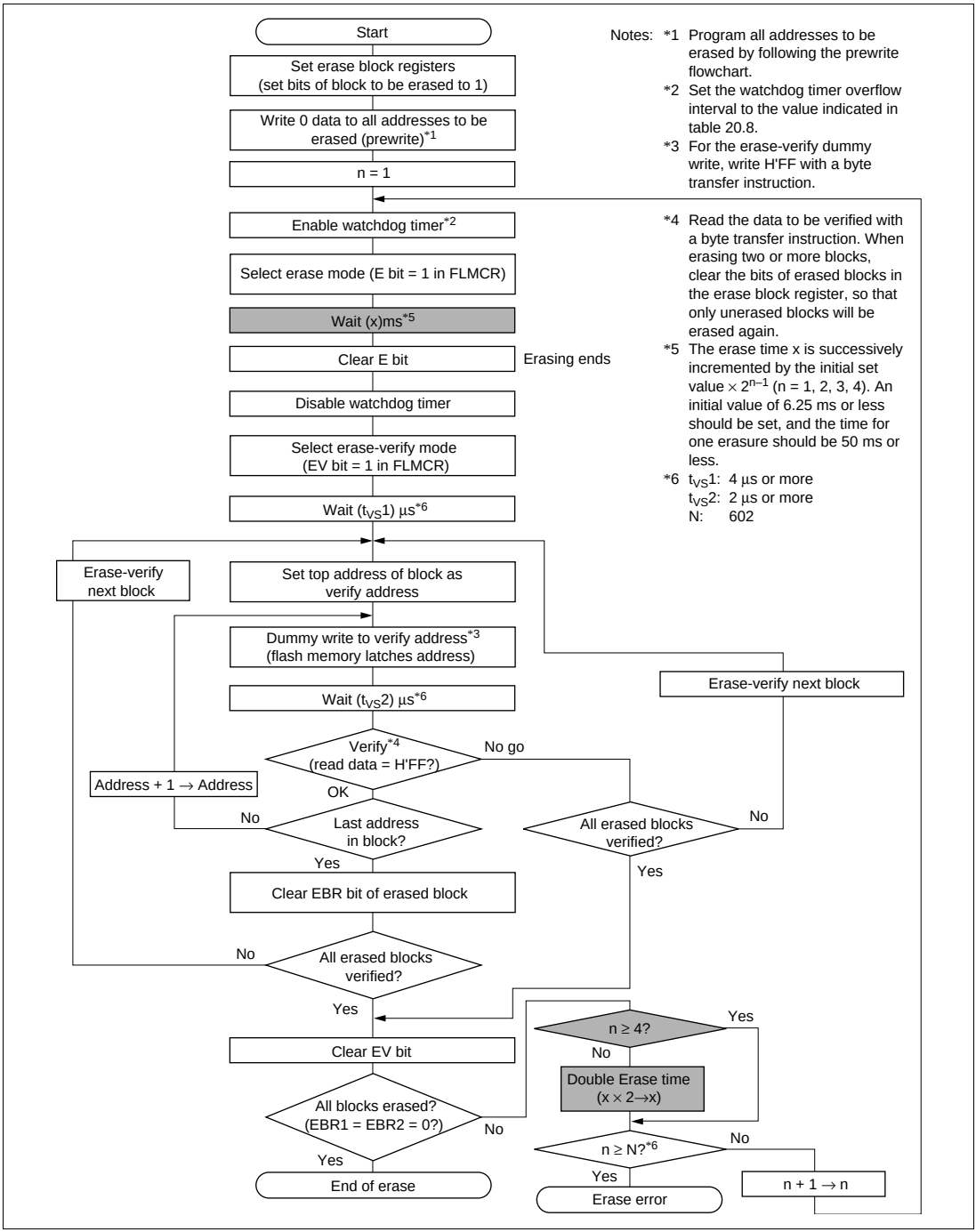

Figure 20.11 Multiple-Block Erase Flowchart

Table 21.22 Area Accessed in Each Mode with FLSHE = 0 and FLSHE = 1

	Mode 1	Mode 2	Mode 3
FLSHE = 1	Reserved area (always H'FF)	Flash memory control register initial values FLLMCR1 = H'80 FLMCR2 = H'00 EBR2 = H'00	
FLSHE = 0	External address space	External address space	Reserved area (always H'FF)

2. When a flash memory control register is accessed in mode 2 (expanded mode with on-chip ROM enabled)

   When a flash memory control register is accessed in mode 2, it can be read or written to if FLSHE = 1, but if FLSHE = 0, external address space will be accessed. It is therefore essential to confirm that FLSHE is set to 1 before accessing these registers.

3. To check whether FLSHE = 0 or 1 in mode 3 (single-chip mode)

   When address H'FF80 is accessed in mode 3, if FLSHE = 1, FLMCR1 is read/written to, and its initial value after a reset is H'80. When FLSHE = 0, however, this address is a reserved area that cannot be modified and always reads H'FF.

22.3.3 Clock Settling Time for Exit from Software Standby Mode

Set bits STS2 to STS0 in SYSCR as follows:

- Crystal oscillator

  Set STS2 to STS0 for a settling time of at least 8 ms. Table 22.3 lists the settling times selected by these bits at several clock frequencies.

- External clock

  The STS bits can be set to any value. The shortest time setting (STS2=STS1=STS0=0) is recommended in most cases. When 1,024 states (STS2 to STS0 = 101) is selected, the following points should be noted.
  If a period exceeding øp/1,024 (e.g. øp/2,048) is specified when selecting the 8-bit timer, PWM timer, or watchdog timer clock, the counter in the timer will not count up normally when 1,024 states is specified for the setting time. To avoid this problem, set the STS value just before the transition to software standby mode (before executing the SLEEP instruction), and re-set the value of STS2 to STS0 to a value from 000 to 100 directly after software standby mode is cleared by an interrupt.

Table 22.3 Times Set by Standby Timer Select Bits (Unit: ms)

			Settling Time	System Clock Frequency (MHz)								
STS2	**STS1**	**STS0**	**(States)**	**16**	**12**	**10**	**8**	**6**	**4**	**2**	**1**	**0.5**
0	0	0	8,192	0.51	0.65	0.8	1.0	1.3	2.0	4.1	**8.2**	**16.4**
0	0	1	16,384	1.0	1.3	1.6	2.0	2.7	4.1	**8.2**	16.4	32.8
0	1	0	32,768	2.0	2.7	3.3	4.1	5.5	**8.2**	16.4	32.8	65.5
0	1	1	65,536	4.1	5.5	6.6	**8.2**	**10.9**	16.4	32.8	65.5	131.1
1	0	0/—*	131,072	**8.2**	**10.9**	**13.1**	16.4	21.8	32.8	65.5	131.1	262.1

Note: Recommended values are printed in boldface.
* F-ZTAT version/ZTAT and mask-ROM versions.

Table 23.3 DC Characteristics (4-V Version)

Conditions: V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V[*1], V_{SS} = AV_{SS} = 0 V, Ta = –20°C to +75°C (regular specifications), Ta = –40°C to +85°C (wide-range specifications)

Item			Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	$P6_7$ to $P6_0$[*4], $\overline{IRQ_2}$ to $\overline{IRQ_0}$[*5], $\overline{IRQ_7}$ to $\overline{IRQ_3}$	(1)	V_T^-	1.0	—	—	V	V_{CC} = 4.5 V to 5.5 V
			V_T^+	—	—	$V_{CC} \times 0.7$		
			$V_T^+ - V_T^-$	0.4	—	—		
			V_T^-	0.8	—	—		V_{CC} = 4.0 V to 4.5 V
			V_T^+	—	—	$V_{CC} \times 0.7$		
			$V_T^+ - V_T^-$	0.3	—	—		
Input high voltage	$\overline{RES}$, $\overline{STBY}$, MD_1, MD_0, EXTAL, $\overline{NMI}$	(2)	V_{IH}	V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	SCL, SDA			$V_{CC} \times 0.7$	—	V_{CC} + 0.3		
	$P7_7$ to $P7_0$			2.0	—	AV_{CC} + 0.3		
	All input pins other than (1) and (2) above			2.0	—	V_{CC} + 0.3		
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD_1, MD_0	(3)	V_{IL}	–0.3	—	0.5	V	
	SCL, SDA			–0.3	—	1.0		V_{CC} = 4.5 V to 5.5 V
				–0.3	—	0.8		V_{CC} = 4.0 V to 4.5 V
	All input pins other than (1) and (3) above			–0.3	—	0.8		V_{CC} = 4.5 V to 5.5 V
				–0.3	—	0.6		V_{CC} = 4.0 V to 4.5 V
Output high voltage	All output pins[*6]		V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
				3.5	—	—		I_{OH} = –1.0 mA, V_{CC} = 4.5 V to 5.5 V
				2.8	—	—		I_{OH} = –1.0 mA, V_{CC} = 4.0 V to 4.5 V

Table 23.18 Allowable Output Current Values (3-V Version)

Conditions: V_{CC} = 3.0 to 5.5 V, AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = –20˚C to +75˚C (regular specifications), Ta = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit
Allowable output low current (per pin)	SCL, SDA (bus drive selection)	I_{OL}	—	—	10	mA
	Ports 1 and 2		—	—	2	
	Other output pins		—	—	1	
Allowable output low current (total)	Ports 1 and 2, total	ΣI_{OL}	—	—	40	mA
	Total of all output		—	—	60	
Allowable output high current (per pin)	All output pins	$-I_{OH}$	—	—	2	mA
Allowable output high current (total)	Total of all output	$\Sigma -I_{OH}$	—	—	30	mA

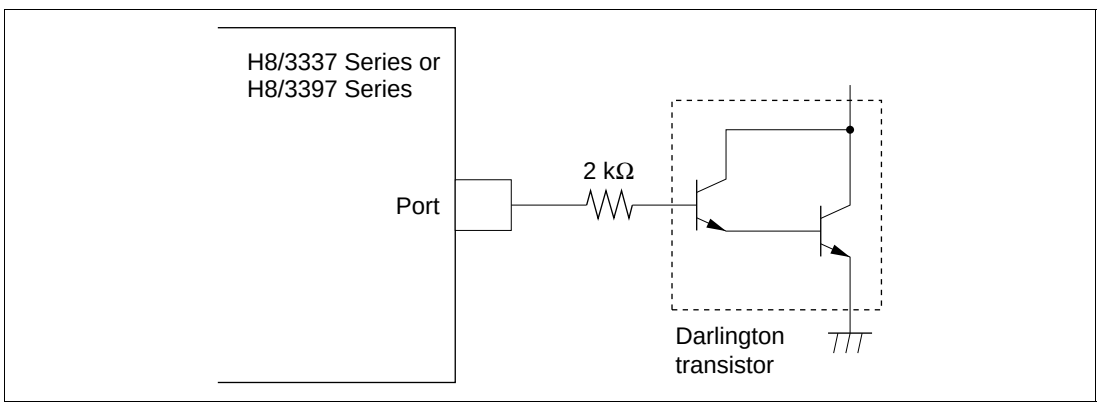

Figure 23.4 Example of Circuit for Driving a Darlington Transistor (5-V Version)

Bit	7	6	5	4	3	2	1	0
	ICIAE	ICIBE	ICICE	ICIDE	OCIAE	OCIBE	OVIE	—
Initial value	0	0	0	0	0	0	0	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—

Timer Overflow Interrupt Enable

0	Timer Overflow interrupt request is disabled.
1	Timer Overflow interrupt request is enabled.

Output Compare Interrupt B Enable

0	Output compare interrupt request B is disabled.
1	Output compare interrupt request B is enabled.

Output Compare Interrupt A Enable

0	Output compare interrupt request A is disabled.
1	Output compare interrupt request A is enabled.

Input Capture Interrupt D Enable

0	Input capture interrupt request D is disabled.
1	Input capture interrupt request D is enabled.

Input Capture Interrupt C Enable

0	Input capture interrupt request C is disabled.
1	Input capture interrupt request C is enabled.

Input Capture Interrupt B Enable

0	Input capture interrupt request B is disabled.
1	Input capture interrupt request B is enabled.

Input Capture Interrupt A Enable

0	Input capture interrupt request A is disabled.
1	Input capture interrupt request A is enabled.

Bit	7	6	5	4	3	2	1	0
	—	—	—	OCRS	OEA	OEB	OLVLA	OLVLB
Initial value	1	1	1	0	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

Output Level B

0	Compare-match B causes 0 output.
1	Compare-match B causes 1 output.

Output Level A

0	Compare-match A causes 0 output.
1	Compare-match A causes 1 output.

Output Enable B

0	Output compare B output is disabled.
1	Output compare B output is enabled.

Output Enable A

0	Output compare A output is disabled.
1	Output compare A output is enabled.

Output Compare Register Select

0	OCRA is selected.
1	OCRB is selected.

ICRA (H and L)—Input Capture Register A H'98, H'99 FRT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Contains FRC count captured on FTIA input.

Bit	7	6	5	4	3	2	1	0
	$P9_7$	$P9_6$	$P9_5$	$P9_4$	$P9_3$	$P9_2$	$P9_1$	$P9_0$
Initial value	0	—*	0	0	0	0	0	0
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Depends on the level of pin $P9_6$.