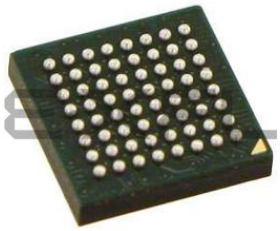

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 22x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LFBGA
Supplier Device Package	64-MAPBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk22fn512vmp12

A/D Converter (Max eight channels)

[12-bit A/D Converter]

- Successive Approximation type
- Conversion time: 0.8 µs @ 5 V
- Priority conversion available (priority at 2 levels)
- Scanning conversion mode

  Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4 steps)

D/A Converter (Max one channel)

- R-2R type
- 10-bit resolution

Base Timer (Max eight channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General-Purpose I/O Port

This series can use its pins as general-purpose I/O ports when they are not used for peripherals. Moreover, the port relocate function is built-in. It can set which I/O port the peripheral function can be allocated to.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 51 high-speed general-purpose I/O Ports@64 pin Package
- Some ports are 5V tolerant

See List of Pin Functions and I/O Circuit Type to confirm the corresponding pins.

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.

Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Multi-function Timer

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3 ch.
- Input capture × 3 ch.
- Output compare × 6 ch.
- A/D activation compare × 1 ch.
- Waveform generator × 3 ch.
- 16-bit PPG timer × 3 ch.

  IGBT mode is contained

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

Real-time clock (RTC)

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

- The interrupt function with specifying date and time (Year/Month/Day/Hour/Minute) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

External Interrupt Controller Unit

- Up to 19 external interrupt input pins @ 64 pin Package
- Include one non-maskable interrupt (NMI) input pin

Watchdog Timer (Two channels)

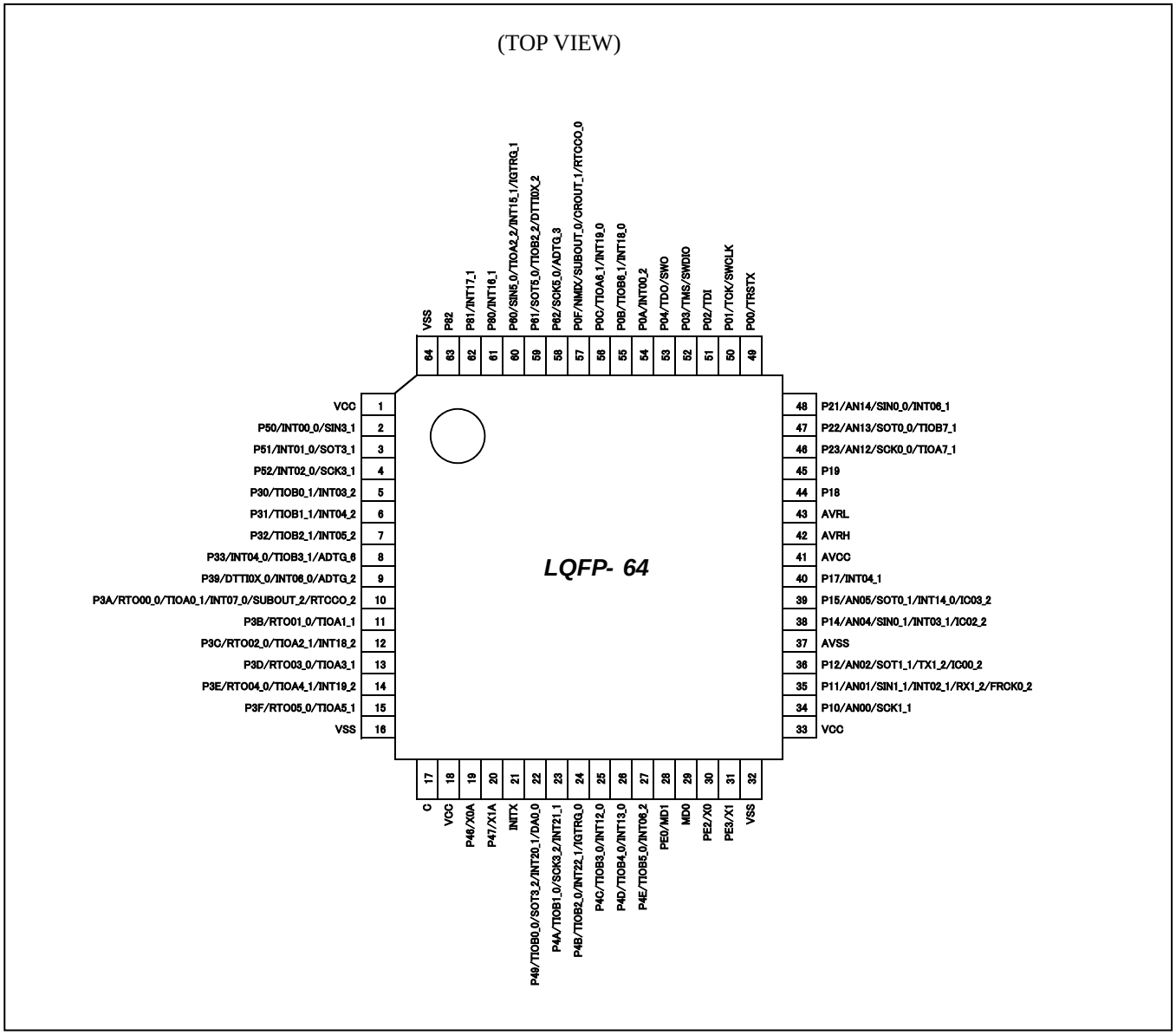
A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a Hardware watchdog and a Software watchdog.

The Hardware watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the Hardware watchdog is active in any low-power consumption modes except RTC, Stop modes.

3. Pin Assignment

LQD064/ LQG064



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

4. List of Pin Functions

List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No			Pin Name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-52	LQFP-48 QFN-48			
1	1	1	VCC	-	
2	2	2	P50 INT00_0 SIN3_1	H*1	K
3	3	3	P51 INT01_0 SOT3_1 (SDA3_1)	H*2	K
4	4	4	P52 INT02_0 SCK3_1 (SCL3_1)	H*2	K
5	-	-	P30 TIOB0_1 INT03_2	E	K
6	-	-	P31 TIOB1_1 INT04_2	E	K
7	-	-	P32 TIOB2_1 INT05_2	E	K
8	-	-	P33 INT04_0 TIOB3_1 ADTG_6	E	K
9	6	5	P39 DTTI0X_0 INT06_0 ADTG_2	E	K
10	7	6	P3A RTO00_0 (PPG00_0) TIOA0_1 INT07_0 SUBOUT_2 RTCCO_2	G	K
11	8	7	P3B RTO01_0 (PPG00_0) TIOA1_1	G	J

Pin No			Pin Name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-52	LQFP-48 QFN-48			
12	9	8	P3C RTO02_0 (PPG02_0) TIOA2_1 INT18_2	G	K
13	10	9	P3D RTO03_0 (PPG02_0) TIOA3_1	G	J
14	11	10	P3E RTO04_0 (PPG04_0) TIOA4_1 INT19_2	G	K
15	12	11	P3F RTO05_0 (PPG04_0) TIOA5_1	G	J
16	13	12	VSS	-	
17	14	13	C	-	
18	15	14	VCC	-	
19	16	15	P46 X0A	D	F
20	17	16	P47 X1A	D	G
21	18	17	INITX	B	C
22	19	18	P49 TIOB0_0 INT20_1 DA0_0	K	K
	-	-	SOT3_2 (SDA3_2)		
23	20	19	P4A TIOB1_0 INT21_1	E	K
	-	-	SCK3_2 (SCL3_2)		
24	-	-	P4B TIOB2_0 INT22_1 IGTRG_0	E	K
25	-	-	P4C TIOB3_0 INT12_0	E	K
26	-	-	P4D TIOB4_0 INT13_0	E	K

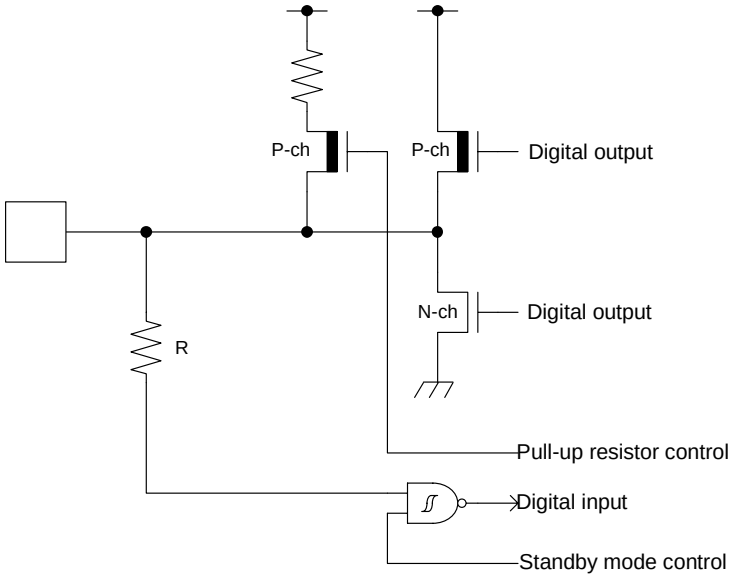
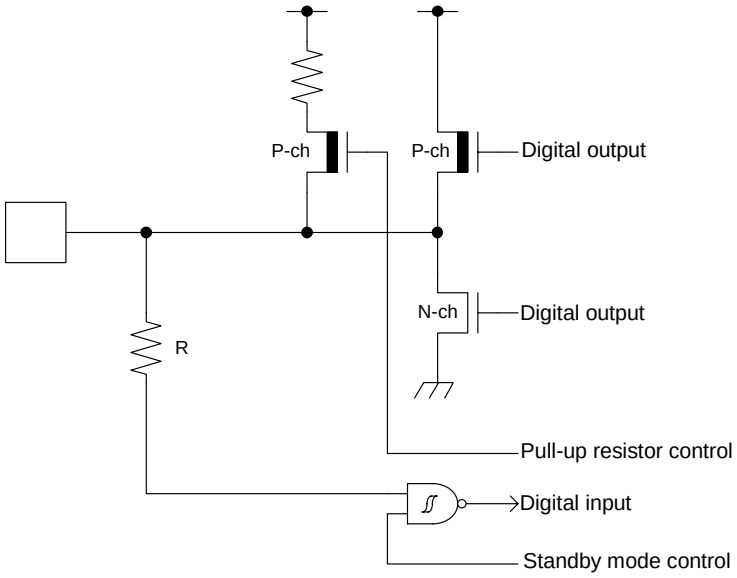
Pin No			Pin Name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-52	LQFP-48 QFN-48			
46	37	34	P23 AN12 SCK0_0 (SCL0_0) TIOA7_1	I*2	M
47	38	35	P22 AN13 SOT0_0 (SDA0_0) TIOB7_1	I*2	M
48	39	36	P21 AN14 SIN0_0 INT06_1	I*1	M
49	41	37	P00 TRSTX	E	I
50	42	38	P01 TCK SWCLK	E	I
51	43	39	P02 TDI	E	I
52	44	40	P03 TMS SWDIO	E	I
53	45	41	P04 TDO SWO	E	I
54	-	-	P0A INT00_2	E	K
55	-	-	P0B TIOB6_1 INT18_0	E	K
56	-	-	P0C TIOA6_1 INT19_0	E	K
57	46	42	P0F NMIX SUBOUT_0 CROUT_1 RTCCO_0	E	H
58	-	-	P62 SCK5_0 (SCL5_0) ADTG_3	E	J

Pin function	Pin name	Function description	Pin No		
			LQFP-64 QFN-64	LQFP-52	LQFP-48 QFN-48
Multi-function Serial 5	SIN5_0	Multi-function serial interface ch.5 input pin	60	48	44
	SOT5_0 (SDA5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I^2C (operation mode 4).	59	47	43
	SCK5_0 (SCL5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I^2C (operation mode 4).	58	-	-
Multi-function Timer 0	DTTI0X_0	Input signal of waveform generator to control outputs RTO00 to RTO05 of Multi-function timer 0.	9	6	5
	DTTI0X_2		59	47	43
	FRCK0_2	16-bit free-run timer ch.0 external clock input pin	35	28	26
	IC00_2	16-bit input capture input pin of Multi-function timer 0. ICxx describes channel number.	36	29	27
	IC02_2		38	31	29
	IC03_2		39	32	30
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	10	7	6
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	11	8	7
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	12	9	8
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	13	10	9
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	14	11	10
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	15	12	11
	IGTRG_0	PPG IGBT mode external trigger input pin	24	-	-
	IGTRG_1		60	48	44

Pin function	Pin name	Function description	Pin No		
			LQFP-64 QFN-64	LQFP-52	LQFP-48 QFN-48
CAN	TX1_2	CAN interface TX output pin	36	29	27
	RX1_2	CAN interface RX input pin	35	28	26
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	57	46	42
	RTCCO_2		10	7	6
	SUBOUT_0	Sub clock output pin	57	46	42
	SUBOUT_2		10	7	6
DAC	DA0_0	D/A converter ch.0 analog output pin	22	19	18
RESET	INITX	External Reset Input pin. A reset is valid when INITX="L".	21	18	17
Mode	MD0	Mode 0 pin. During normal operation, MD0="L" must be input. During serial programming to Flash memory, MD0="H" must be input.	29	23	21
	MD1	Mode 1 pin. During serial programming to Flash memory, MD1="L" must be input.	28	22	20
Power	VCC	Power supply Pin	1	1	1
			18	15	14
			33	-	-
GND	VSS	GND Pin	16	13	12
			32	26	24
			64	52	48
Clock	X0	Main clock (oscillation) input pin	30	24	22
	X0A	Sub clock (oscillation) input pin	19	16	15
	X1	Main clock (oscillation) I/O pin	31	25	23
	X1A	Sub clock (oscillation) I/O pin	20	17	16
	CROUT_1	Built-in high-speed CR-osc clock output port	57	46	42
Analog Power	AVCC	A/D converter and D/A converter analog power supply pin	41	33	31
	AVRH	A/D converter analog reference voltage input pin	42	34	32
Analog GND	AVSS	A/D converter and D/A converter GND pin	37	30	28
	AVRL	A/D converter analog reference voltage input pin	43	35	33
C pin	C	Power supply stabilization capacity pin	17	14	13

Note:

- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

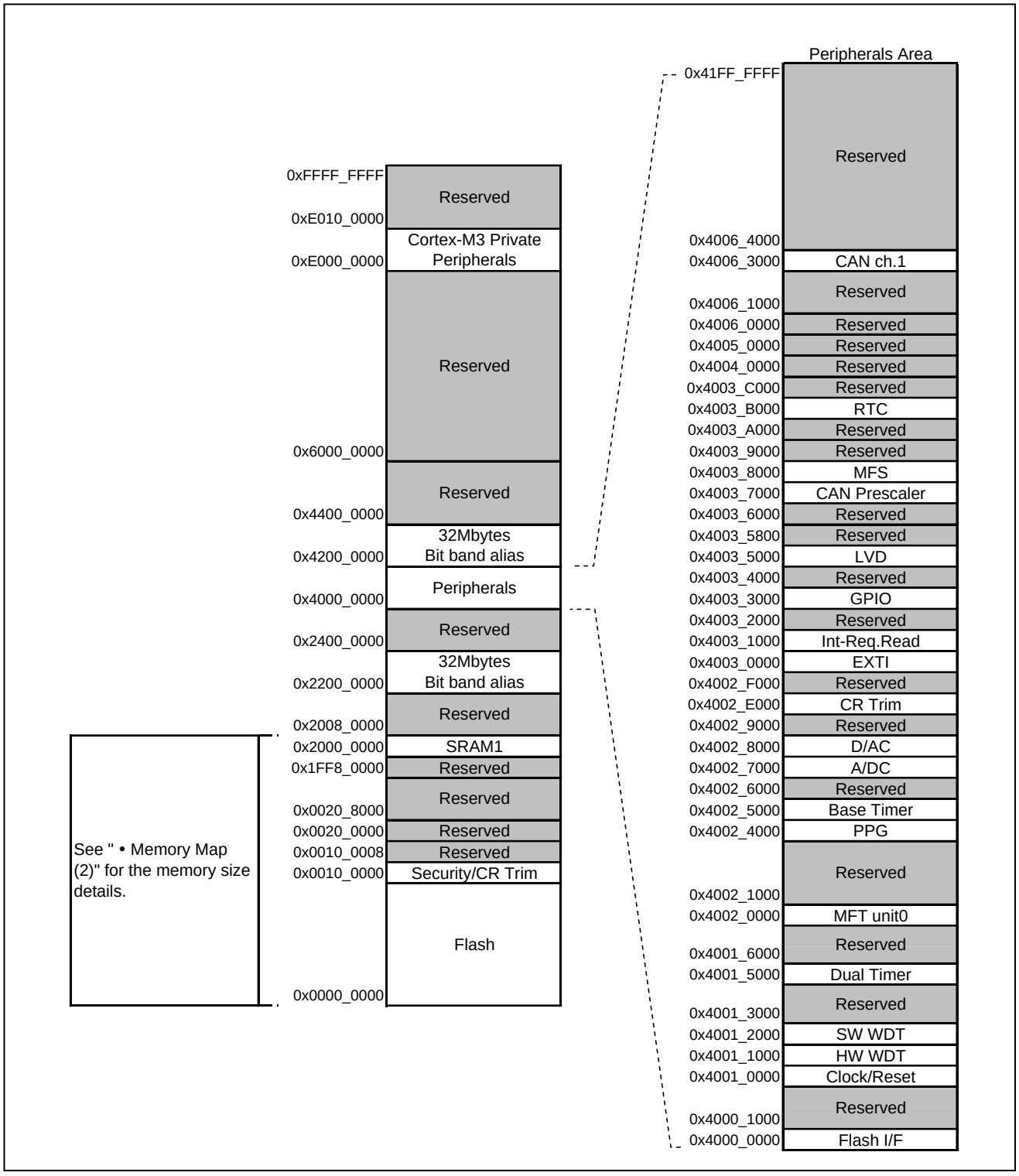
Type	Circuit	Remarks
G		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -12 mA, I_{OL}= 12 mA • +B input is available
H		• CMOS level output • CMOS level hysteresis input • 5 V tolerant • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA • Available to control PZR registers. Only P51, P52. • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

9. Memory Size

See Memory size in Product Lineup to confirm the memory size.

10. Memory Map

Memory Map (1)



11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

- INITX=0

  This is the period when the INITX pin is the L level.

- INITX=1

  This is the period when the INITX pin is the H level.

- SPL=0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

- SPL=1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at 0

  This is the status that the input function cannot be used. Internal input is fixed at L.

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage*1, *3	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage*1, *3	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage*1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage*1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage*1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
Clamp maximum current	I_{CLAMP}	-2	+2	mA	*7
Clamp total maximum current	$\Sigma [I_{CLAMP}]$		+20	mA	*7
L level maximum output current*4	I_{OL}	-	10	mA	4 mA type
			20	mA	12 mA type
L level average output current*5	I_{OLAV}	-	4	mA	4 mA type
			12	mA	12 mA type
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current*6	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current*4	I_{OH}	-	- 10	mA	4 mA type
			- 20	mA	12 mA type
H level average output current*5	I_{OHAV}	-	- 4	mA	4 mA type
			- 12	mA	12 mA type
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current*6	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	350	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0$ V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: Ensure that the voltage does not exceed V_{CC} + 0.5 V, for example, when the power is turned on.

*4: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*5: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.

*6: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100 ms.

12.4.9 CSIO/UART Timing

CSIO (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to clock synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function serial is connected to, see Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*

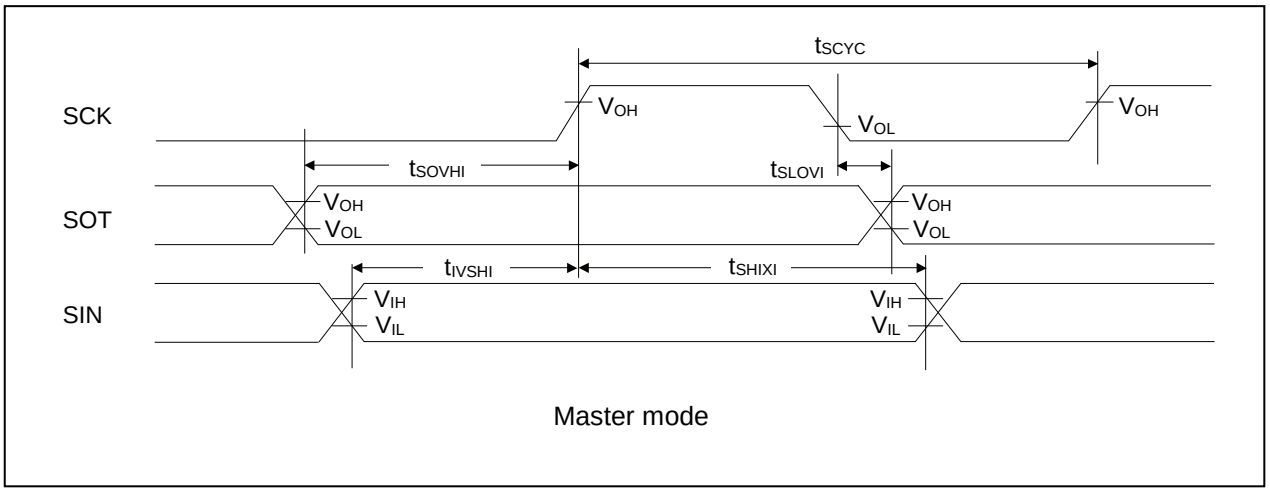
CSIO (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

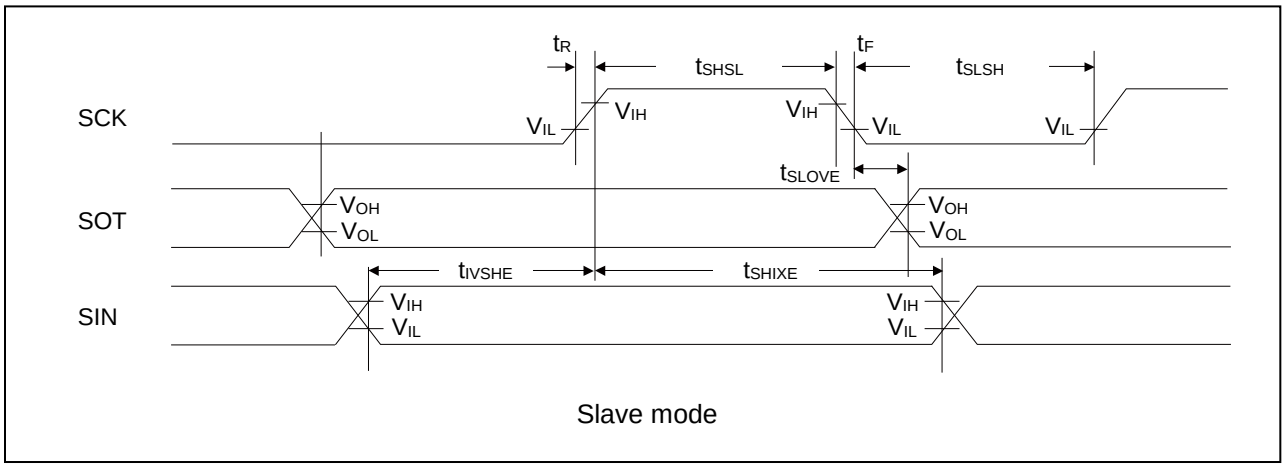
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to clock synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
- *About the APB bus number which Multi-function serial is connected to, see Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



Master mode

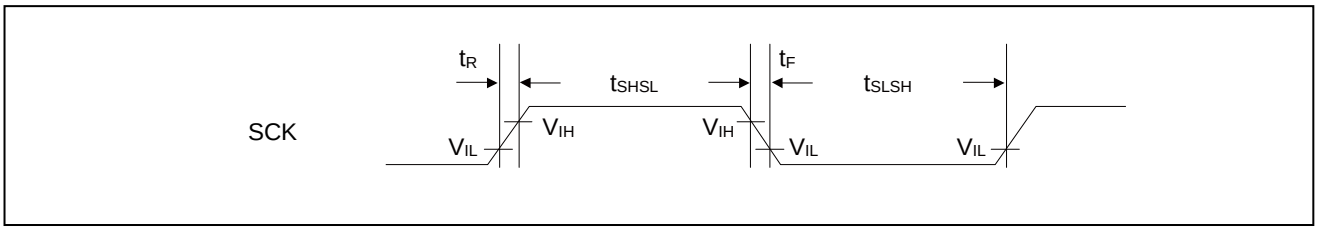


Slave mode

UART external clock input (EXT = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	t_F		-	5	ns	
SCK rising time	t_R		-	5	ns	



12.4.10 External Input Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

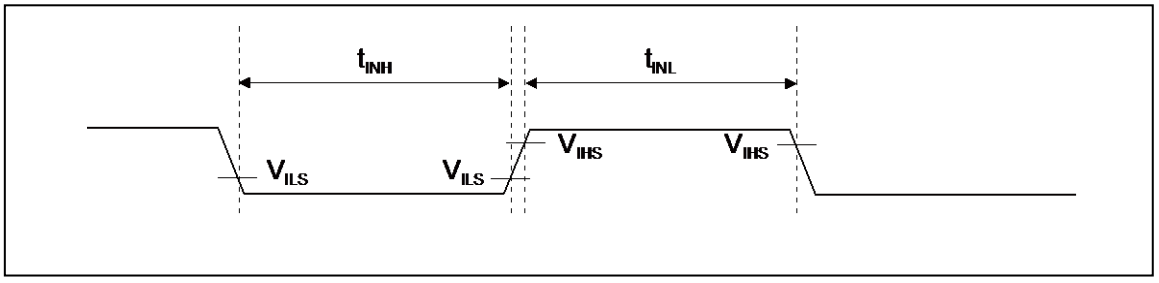
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		IGTRG	-	$2t_{CYCP}$*1	-	ns	PPG IGBT mode
		INTxx, NMIX	*2	$2t_{CYCP}$ + 100*1	-	ns	External interrupt, NMI
			*3	500	-	ns	

*1: t_{CYCP} indicates the APB bus clock cycle time.

About the APB bus number which the A/D converter, Multi-function Timer, External interrupt are connected to, see Block Diagram in this data sheet.

*2: When in Run mode, in Sleep mode.

*3: When in stop mode, in RTC mode, in timer mode.



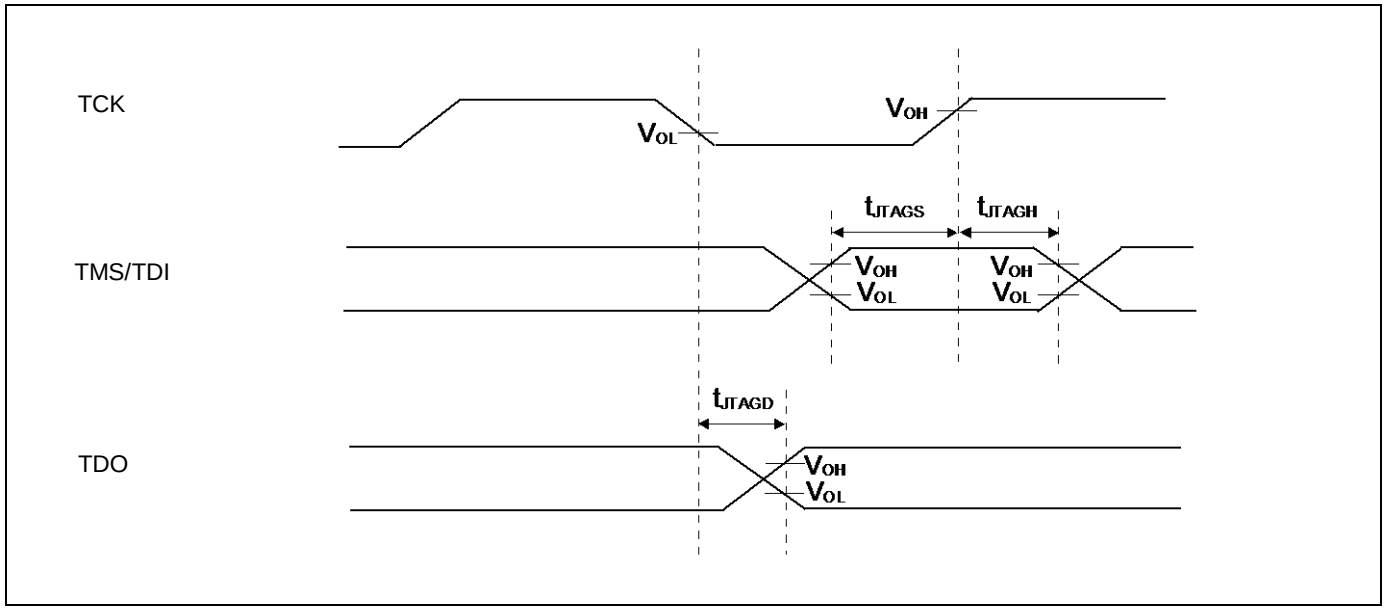
12.4.12 JTAG Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 4.5$ V	-	25	ns	
			$V_{CC} < 4.5$ V	-	45		

Note:

- *When the external load capacitance C_L = 30 pF.*



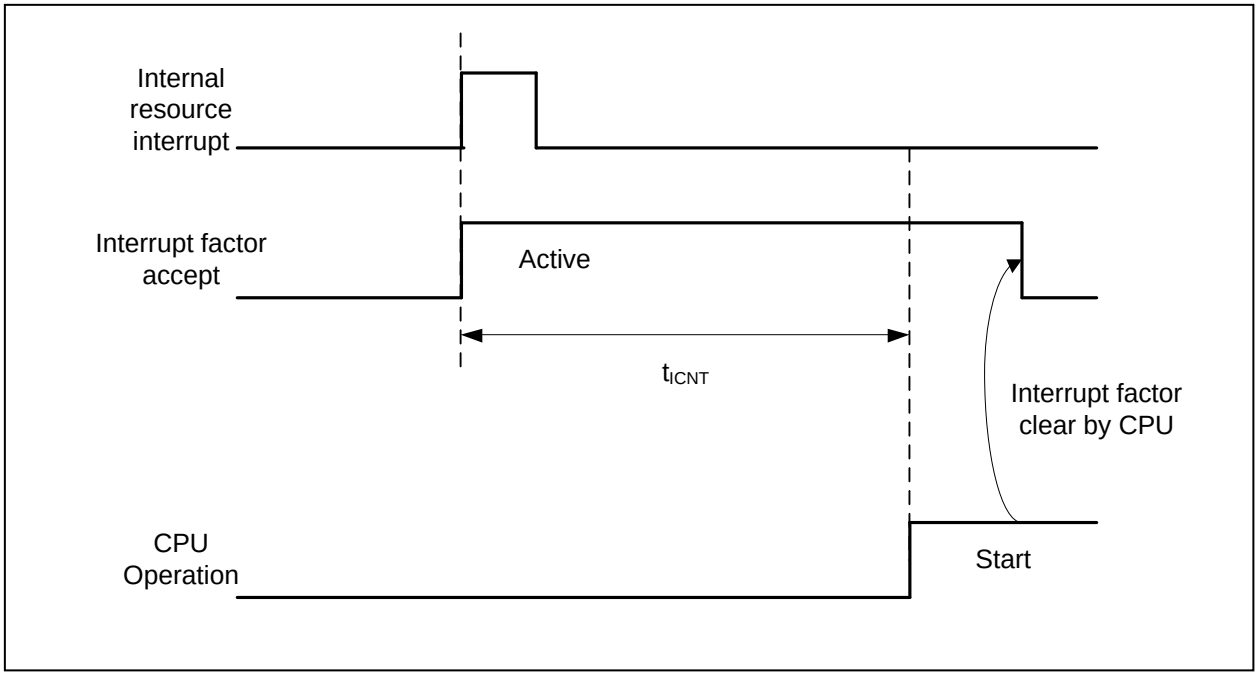
12.7.2 Interrupt of Low-Voltage Detection

(T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI = 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		3.04	3.30	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		3.40	3.70	4.00	V	When voltage rises
Detected voltage	VDL	SVHI = 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		3.50	3.80	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.10	4.43	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		3.86	4.20	4.54	V	When voltage rises
Detected voltage	VDL	SVHI = 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		3.96	4.30	4.64	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	8160 × t_{CYCP}*	µs	
LVD detection delay time	t_{LVDDL}	-	-	-	200	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

Operation example of return from Low-Power consumption mode (by internal resource interrupt*)



*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes. See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM3 Family Peripheral Manual.*
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in FM3 Family Peripheral Manual.*

12.9.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

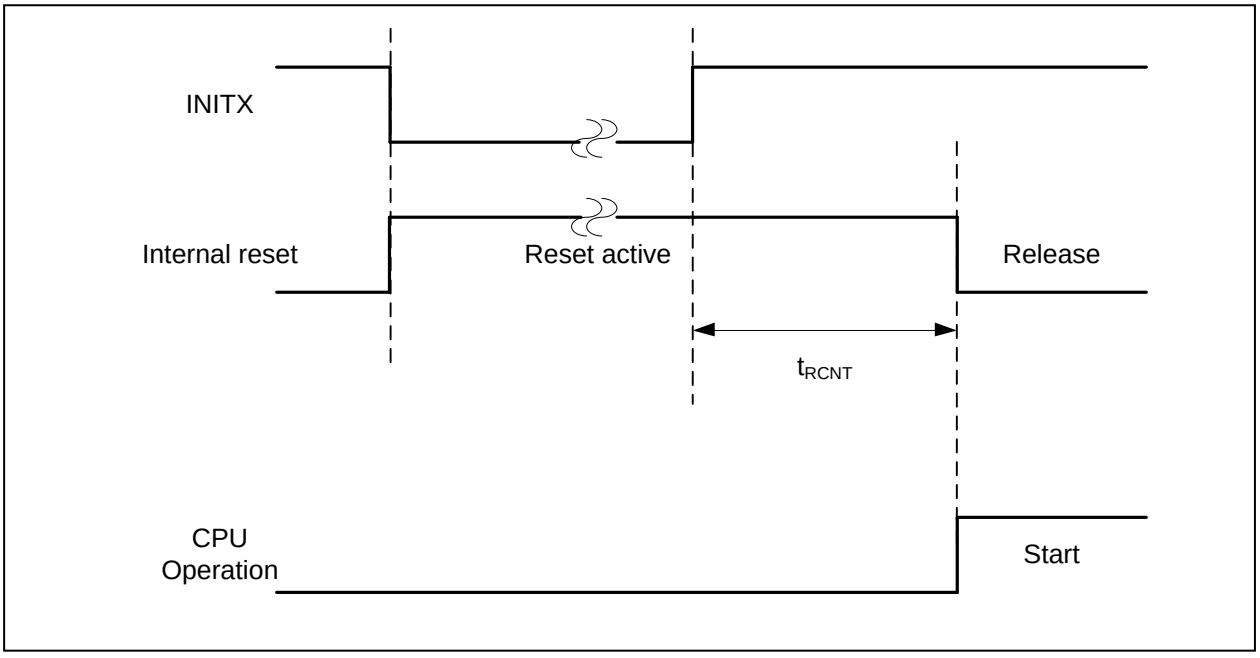
Return Count Time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

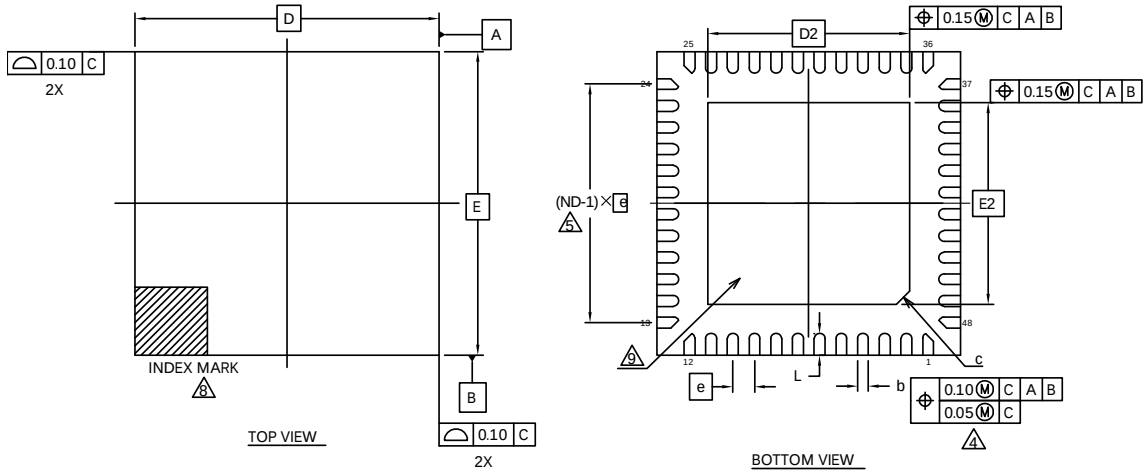
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	149	264	µs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		149	264	µs	
Low-speed CR Timer mode		318	603	µs	
Sub Timer mode		308	583	µs	
RTC/Stop mode		248	443	µs	

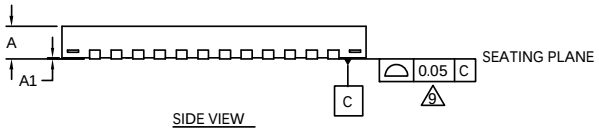
*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by INITX)



Package Type	Package Code
QFN 48	WNY048





SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.80
A1	0.00	—	0.05
D	7.00 BSC		
E	7.00 BSC		
b	0.18	0.25	0.30
D2	4.65 BSC		
E2	4.65 BSC		
e	0.50 BSC		
c	0.30 REF		
L	0.45	0.50	0.55

NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5-1994.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL. THE DIMENSION "b"SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSEDHEAT SINK SLUG AS WELL AS THE TERMINALS.
10. JEDEC SPECIFICATION NO. REF : N/A

PACKAGE OUTLINE, 48 LEAD QFN
7.00X7.00X0.80 MM WNY048 4.65X4.65 MM EPAD(SAWN) REV*I

002-16422 **