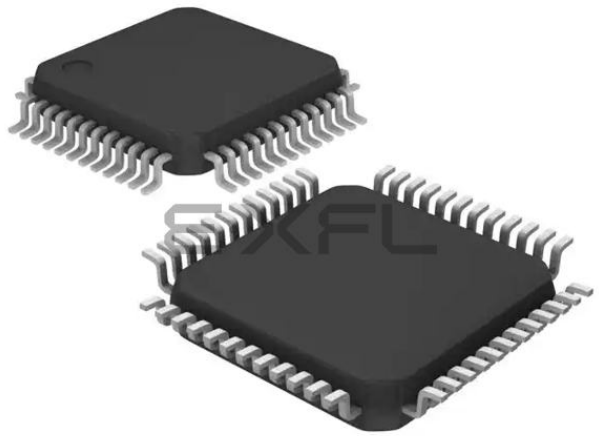
Analog Devices Inc./Maxim Integrated - MAXQ7667AACM+T Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	16-Bit
Speed	16MHz
Connectivity	LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	16
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 2.75V
Data Converters	A/D 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq7667aacm-t

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5V, V_{AVDD} = +3.3V; V_{DVDD} = +2.5V, system clock (f_{SYSCLK}) = 16MHz, burst frequency (f_{BURST}) = bandpass frequency (f_{BPF}) = 50kHz, C_{REFBG} = C_{REF} = 1µF in parallel with 0.01µF, f_{ADCCLK} = 2MHz (SAR data rate = 125ksps), T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BANDPASS FILTER						
Center Frequency	f_{BPF}		25		100	kHz
Passband Width		-3dB		0.14 x f_{BPF}		kHz
Minimum Stopband Rejection		One decade away from center frequency		-60		dB
Output Data Rate				10 x f_{BPF}		ksps
Output Data Resolution				16		Bits
LOWPASS FILTER						
Corner Frequency	f_{LPF}	-3dB		0.1 x f_{BPF}		kHz
Rolloff				40		dB/Decade
Output Data Rate				5 x f_{BPF}		ksps
Output Data Resolution				16		Bits
SAR ADC						
Resolution		Measurement	12			Bits
		No missing codes	11			
Integral Nonlinearity		Tested at 125ksps		±1	±2	LSB
Differential Nonlinearity		Tested at 125ksps	-2		+2	LSB
Offset Error				±1	±3	mV
Offset-Error Drift				±5		µV/°C
Gain Error					±1	%
Gain-Error Temperature Coefficient				±0.4		ppmFS/°C
Input-Referred Noise		At ADC inputs		400		$µV_{RMS}$
Differential Input Range		Unipolar	0		V_{REF}	V
		Bipolar	$-V_{REF}/2$		$+V_{REF}/2$	
Absolute Input Range			0		V_{AVDD}	V
Input Leakage Current				±0.1		µA
Conversion Time		13 ADCCLK cycles at 2MHz			6.5	µs
Input Capacitance				14		pF
Track-and-Hold Acquisition Time		Three ADCCLK cycles at 2MHz			1.5	µs
Turn-On Time		Eight ADCCLK cycles at 2MHz			4	µs
Conversion Clock	f_{ADCCLK}		0.5		4	MHz
Conversion Rate		f_{ADCCLK} = 4MHz (not production tested)			250	ksps

16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5V, V_{AVDD} = +3.3V; V_{DVDD} = +2.5V, system clock (f_{SYSCLK}) = 16MHz, burst frequency (f_{BURST}) = bandpass frequency (f_{BPF}) = 50kHz, C_{REFBG} = C_{REF} = 1µF in parallel with 0.01µF, f_{ADCCLK} = 2MHz (SAR data rate = 125ksps), T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE BUFFER						
Offset				5		mV
Minimum Load			2.5			kΩ
Output Bypass Capacitor				0.47		µF
EXTERNAL VOLTAGE REFERENCE (Reference Buffer Disabled)						
Reference Input Range		Applied at REF	1.0		V_{AVDD}	V
Reference Input Impedance		Measured at REF with the SAR and sigma-delta ADCs running at maximum frequency		50		kΩ
INTERNAL VOLTAGE REFERENCE (REFBG)						
Initial Accuracy			2.45	2.5	2.55	V
Maximum Temperature Coefficient				100		ppm/°C
Output Impedance				1.1		kΩ
Power-Supply Rejection Ratio		V_{AVDD} = 3.0V to 3.6V		60		dB
Output Noise				0.5		mV_{RMS}
PROGRAMMABLE BURST-FREQUENCY OSCILLATOR						
Burst-Frequency Range			0.025		1.335	MHz
Burst-Frequency Resolution				0.1		%
Burst-Frequency Locking Time		Change from 40kHz to 60kHz		5		ms
		Change from 50kHz to 50.5kHz		2		
CRYSTAL OSCILLATOR						
Frequency Range		Tested crystal frequency		16		MHz
		Minimum crystal frequency		4		
		External clock input	4		16	
Temperature Stability		Excluding crystal		25		ppm/°C
Startup Time		16MHz crystal		10		ms
XIN Input Low Voltage		When driven with external clock source			0.3 x V_{DVDD}	V
XIN Input High Voltage		When driven with external clock source	0.7 x V_{DVDD}			V
INTERNAL RC OSCILLATOR						
Frequency				13.5		MHz
Initial Accuracy				10.5		%
Temperature Drift		T_A = T_{MIN} to T_{MAX}		700		ppm
Supply Rejection		V_{DVDD} = 2.25V to 2.75V		-1.5		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5V, V_{AVDD} = +3.3V; V_{DVDD} = +2.5V, system clock (f_{SYSCLK}) = 16MHz, burst frequency (f_{BURST}) = bandpass frequency (f_{BPF}) = 50kHz, C_{REFBG} = C_{REF} = 1µF in parallel with 0.01µF, f_{ADCCLK} = 2MHz (SAR data rate = 125ksps), T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Adjustable Frequency Range		Using the RCTRM register	-40		+40	%
Frequency Adjustment Resolution				0.2		%
SUPPLY VOLTAGE SUPERVISORS						
DVDD Reset Threshold		Asserts $\overline{RESET}$ if V_{DVDD} falls below this threshold	2.10		2.25	V
DVDD Interrupt Threshold		Generates an interrupt if V_{DVDD} falls below this threshold	2.25		2.38	V
Minimum Reset and Interrupt Threshold Difference			150			mV
AVDD Interrupt Threshold		Generates an interrupt if V_{AVDD} falls below this threshold	2.95		3.15	V
DVDDIO Interrupt Threshold		Generates an interrupt if V_{DVDDIO} falls below this threshold	4.5		4.75	V
Supervisor Operating Range		At DVDD	1.5		2.75	V
Supervisor Hysteresis				1		%
$\overline{RESET}$ Release Delay		After V_{DVDD} rises above the reset threshold		35		µs
Power-Up Time		Time from $\overline{RESET}$ is released to the execution of the first instruction (serial bootloader off)		1		µs
+5V LINEAR REGULATOR (DVDDIO, GATE5, Requires External Pass Transistor, see the *Typical Application Circuit/Functional Diagram*)						
Regulator Output Voltage		At DVDDIO	4.75		5.25	V
GATE5 Output High Voltage		I_{SOURCE} = 0µA (no load)	V_{DVDDIO} - 0.1			V
GATE5 Output Low Voltage		I_{SINK} = 500µA			2	V
GATE5 Output Resistance		I_{SINK} = 0µA to 50µA		330		Ω
Gain Bandwidth		DVDDIO to GATE5		1.58		kHz
Gain		DVDDIO to GATE5		1700		V/V
GATE5 Slew Rate				4.3		V/ms
Maximum Load Capacitance		Maximum capacitance on DVDDIO when using an external pass transistor		1		µF
+3.3V LINEAR REGULATOR (REG3P3)						
REG3P3 Output Voltage			3.15		3.45	V
Load Current					50	mA
Output Short-Circuit Current		REG3P3 shorted to AGND		150		mA

16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5V, V_{AVDD} = +3.3V; V_{DVDD} = +2.5V, system clock (f_{SYSCLK}) = 16MHz, burst frequency (f_{BURST}) = bandpass frequency (f_{BPF}) = 50kHz, C_{REFBG} = C_{REF} = 1µF in parallel with 0.01µF, f_{ADCCLK} = 2MHz (SAR data rate = 125ksps), T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
+2.5V LINEAR REGULATOR (REG2P5)							
REG2P5 Output Voltage				2.38		2.62	V
Load Current						50	mA
Output Short-Circuit Current		REG2P5 shorted to DGND			100		mA
POWER REQUIREMENTS							
Supply Voltage Range		DVDD		2.25	2.5	2.75	V
		AVDD		3.00	3.3	3.6	
		DVDDIO		4.5	5.0	5.5	
AVDD Supply Current		All analog functions enabled			12	18	mA
		All analog functions disabled			3	10	µA
		Incremental AVDD supply current	LNA		2.4		mA
			Sigma-delta ADC		12		
			SAR ADC, 250ksps, f_{ADCCLK} = 4MHz		600		µA
			PLL		300		
			Supply voltage supervisors		3		
			Internal voltage reference		220		
			Reference buffer		300		
			Bias (any AVDD module enabled)		1.5		mA
DVDD Supply Current					11		mA
DVDDIO Supply Current					2.5		mA
DIGITAL INPUTS (GPIO, UART, JTAG, SPI™)							
Input High Voltage				V_{DVDDIO} - 1			V
Input Low Voltage						0.8	V
Input Hysteresis		V_{DVDDIO} = 5.0V			500		mV
Input Leakage Current		Digital input voltage = DGND or DVDDIO, pullup disabled			±0.01	±1	µA
Pullup/Pulldown Resistance		Pulled up to DVDDIO internally, pulled down to DGND internally			150		kΩ
Input Capacitance					15		pF

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5V, V_{AVDD} = +3.3V; V_{DVDD} = +2.5V, system clock (f_{SYSCLK}) = 16MHz, burst frequency (f_{BURST}) = bandpass frequency (f_{BPF}) = 50kHz, C_{REFBG} = C_{REF} = 1µF in parallel with 0.01µF, f_{ADCCLK} = 2MHz (SAR data rate = 125ksps), T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS (GPIO, UART, JTAG, SPI)						
Output Low Voltage		I_{SINK} = 0.5mA, drive strength = low			0.4	V
		I_{SINK} = 1.0mA, drive strength = high			0.4	
Output High Voltage		I_{SOURCE} = 0.5mA, drive strength = low	V_{DVDDIO} - 0.5			V
		I_{SOURCE} = 1.0mA, drive strength = high	V_{DVDDIO} - 0.5			
Maximum Output Impedance		Drive strength = low		880		Ω
		Drive strength = high		450		
Three-State Leakage				±0.01	±1	µA
Three-State Capacitance				15		pF
BURST OUTPUT						
Output Low Voltage		I_{SINK} = 8mA			0.4	V
Output High Voltage		I_{SOURCE} = 8mA	V_{DVDDIO} - 0.5			V
Maximum Output Impedance		Drive strength = low		90		Ω
		Drive strength = high		45		
Three-State Leakage				±0.01	±1	µA
Three-State Capacitance				15		pF
Short-Circuit Current		Burst drive set to high		50		mA
$\overline{\text{RESET}}$						
Internal Pullup Resistance		Pulled up to DVDDIO		120		kΩ
Output Low Voltage		I_{SINK} = 0.5mA			0.4	V
Output High Voltage		No external load	V_{DVDDIO} - 0.5			V
Input Low Voltage		When driven by external source			0.8	V
Input High Voltage		When driven by external source	V_{DVDDIO} - 1			V
UART/LIN INTERFACE (UTX, URX)						
UART Baud Rates		Asynchronous mode (system clock/32)			500	kbps
		Synchronous mode (system clock/8)			2000	
		LIN 2.0 compatibility (Note 3)	1		20	

16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

Pin Description

PIN	NAME	FUNCTION
1	P1.3/TCK	Port 1 Data 3/JTAG Serial Clock Input. P1.3 is a general-purpose digital I/O. TCK is the JTAG serial test clock input. Refer to the *MAXQ7667 User's Guide* Sections 5 and 11.
2	P1.4/MOSI	Port 1 Data 4/SPI Serial Data Output. P1.4 is a general-purpose digital I/O. MOSI is the master output, slave input for the SPI interface. Refer to the *MAXQ7667 User's Guide* Sections 5 and 9.
3	P1.5/MISO	Port 1 Data 5/SPI Serial Data Input. P1.5 is a general-purpose digital I/O. MISO is the master input, slave output for the SPI interface. Refer to the *MAXQ7667 User's Guide* Sections 5 and 9.
4	P1.6/SCLK	Port 1 Data 6/SPI Serial Clock Output. P1.6 is a general-purpose digital I/O. SCLK is the serial clock for the SPI interface. SCLK is an input when operating as a slave and an output when operating as a master. Refer to the *MAXQ7667 User's Guide* Sections 5 and 9.
5	P1.7/SYNC/SS	Port 1 Data 7/Schedule Timer Sync Input/SPI Slave Select. P1.7 is a general-purpose digital I/O. A rising edge on the SYNC input resets the schedule timer. In SPI slave mode, SS is the SPI slave-select input. In SPI master mode, use SS or a GPIO to manually select an external slave. Refer to the *MAXQ7667 User's Guide* Sections 5, 7, and 9.
6, 19, 42	DVDD	Digital Supply Voltage. Connect DVDD directly to a +2.5V external source or to REG2P5 output for single supply operation. Bypass DVDD to DGND with a 0.1µF capacitor as close as possible to the device. Connect all DVDD nodes together.
7, 18, 43	DGND	Digital Ground. Connect all DGND nodes together. Connect to AGND at a single point.
8, 17, 44	DVDDIO	Digital I/O Supply Voltage. DVDDIO powers all digital I/Os except for XIN and XOUT. Bypass DVDDIO to DGND with a 0.1µF capacitor as close as possible to the device. Connect all DVDDIO nodes together.
9	P0.0/URX	Port 0 Data 0/UART Receive Data Input. P0.0 is a general-purpose digital I/O. URX is a UART or LIN data receive input. Refer to the *MAXQ7667 User's Guide* Sections 5 and 8.
10	P0.1/UTX	Port 0 Data 1/UART Transmit Data Output. P0.1 is a general-purpose digital I/O. UTX is a UART or LIN data transmit output. Refer to the *MAXQ7667 User's Guide* Sections 5 and 8.
11	P0.2/$\overline{\text{TXEN}}$	Port 0 Data 2/UART Transmit Output. P0.2 is a general-purpose digital I/O. $\overline{\text{TXEN}}$ asserts low when the UART is transmitting. Use $\overline{\text{TXEN}}$ to enable an external LIN/UART transceiver. Refer to the *MAXQ7667 User's Guide* Sections 5 and 8.
12	P0.3/T0/ ADCCTL	Port 0 Data 3/Timer 0 I/O/ADC Control Input. P0.3 is a general-purpose digital I/O. T0 is the primary Type 2 timer/counter 0 output or input. ADCCTL is a sampling/conversion trigger input for the SAR ADC. Refer to the *MAXQ7667 User's Guide* Sections 5, 6, and 14.
13	P0.4/T0B	Port 0 Data 4/Timer 0B I/O/Comparator Output. P0.4 is a general-purpose digital I/O. T0B is the secondary Type 2 timer/counter 0 output or input. Refer to the *MAXQ7667 User's Guide* Sections 5 and 6.
14	P0.5/T1	Port 0 Data 5/Timer 1 I/O. P0.5 is a general-purpose digital I/O. T1 is the primary Type 2 timer/counter 1 output or input. Refer to the *MAXQ7667 User's Guide* Sections 5 and 6.
15	P0.6/T2	Port 0 Data 6/Timer 2 I/O. P0.6 is a general-purpose digital I/O. T2 is the primary Type 2 timer/counter 2 output or input. Refer to the *MAXQ7667 User's Guide* Sections 5 and 6.
16	P0.7/T2B	Port 0 Data 7/Timer 2B I/O. P0.7 is a general-purpose digital I/O. T2B is the secondary Type 2 timer/counter 2 output or input. Refer to the *MAXQ7667 User's Guide* Sections 5 and 6.
20	XIN	Crystal Oscillator Input. Connect an external crystal or resonator between XIN and XOUT. When using an external clock source drive XIN with 2.5V level clock while leaving XOUT unconnected. Connect XIN to DGND when an external clock source is not used.

Pin Description (continued)

PIN	NAME	FUNCTION
21	XOUT	Crystal Oscillator Output. Connect an external crystal or resonator between XIN and XOUT. Leave XOUT unconnected when driving XIN with a 2.5V level clock or when an external clock source is not used.
22	REG2P5	+2.5V Voltage Regulator Output
23	REG3P3	+3.3V Voltage Regulator Output
24	GATE5	+5V DVDDIO Voltage Regulator Control Output. GATE5 controls an external npn or nMOS transistor that passes power to DVDDIO.
25	$\overline{\text{RESET}}$	Reset Input/Output. $\overline{\text{RESET}}$ is open drain with an internal pullup resistor to DVDDIO. Internal circuitry pulls $\overline{\text{RESET}}$ low when V_{DVDDIO} falls below its brownout reset value or watchdog reset is enabled and the watchdog timeout period expires. Force $\overline{\text{RESET}}$ low externally for manual reset.
26	FILT	PLL VCO Control Input. Connect external filter components on FILT for the internal PLL circuit. See the *Typical Application Circuit/Functional Diagram*.
27, 32	AVDD	Analog Supply Voltage. Connect all AVDD inputs directly to a +3.3V source or to REG3P3 for self-powered operation. Bypass each AVDD to AGND with a 0.1µF capacitor as close as possible to the device.
28, 31, 33	AGND	Analog Ground. Connect all AGND nodes together. Connect to DGND at a single point.
29	ECHON	Negative Echo Input. AC-couple ECHON to an ultrasonic transducer.
30	ECHOP	Positive Echo Input. AC-couple ECHOP to an ultrasonic transducer.
34	REF	ADC Reference Input/Reference Buffer Output. When using the internal reference, the buffered bandgap reference voltage (V_{REF}) is provided for both SAR and sigma-delta ADCs. When using an external reference, apply an external voltage source ranging between 1V and V_{AVDD} at REF. Disable the reference buffer when applying an external reference at REF. Bypass REF to AGND with a 0.47µF capacitor.
35	REFBG	+2.5V Reference Output/Reference Buffer Input. Bypass to AGND with a 0.47µF capacitor.
36	AIN0	SAR ADC Input 0. AIN0 pairs with AIN1 in differential mode.
37	AIN1	SAR ADC Input 1. AIN1 pairs with AIN0 in differential mode.
38	AIN2	SAR ADC Input 2. AIN2 pairs with AIN3 in differential mode.
49	AIN3	SAR ADC Input 3. AIN3 pairs with AIN2 in differential mode.
40	AIN4	SAR ADC Input 4
41	N.C.	No Connection. Internally connected. Leave unconnected.
45	BURST	Burst Output. Burst is the ultrasonic transducer excitation pulse output. BURST remains in three-state mode on power-up.
46	P1.0/TDO	Port 1 Data 0/JTAG Output. P1.0 is a general-purpose digital I/O. TDO is the JTAG serial data output. Refer to the *MAXQ7667 User's Guide* Sections 5 and 11.
47	P1.1/TMS	Port 1 Data 1/JTAG Test Mode-Select Input. P1.1 is a general-purpose digital I/O. TMS is the JTAG mode-select input. Refer to the *MAXQ7667 User's Guide* Sections 5 and 11.
48	P1.2/TDI	Port 1 Data 2/JTAG Input. P1.2 is a general-purpose digital I/O. TDI is the JTAG serial data input. Refer to the *MAXQ7667 User's Guide* Sections 5 and 11.

16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

Detailed Features

- Smart Analog Peripherals
  - Dedicated Ultrasonic Burst Generator
  - Echo Receiving Path
    - Low-Noise Amplifier
    - Time Variable Gain Amplifier
    - 16-Bit Sigma-Delta ADC
    - Digital Bandpass Filter
    - Full-Wave Rectifier and Digital Lowpass Filter
    - 8-Deep, 16-Bit Wide FIFO Simplifies Real-Time Processing
    - Magnitude Comparator
  - 5-Channel, 12-Bit SAR ADC with 250ksps Sampling Rate
  - Internal Bandgap Voltage Reference for the ADCs (Also Accepts External Voltage Reference)
- Timer/Digital I/O Peripherals
  - SPI Interface
  - Three 16-Bit (or Six 8-Bit) Programmable Type 2 Timers/Counters
  - 16-Bit Schedule Timer
  - Programmable Watchdog Timer
  - 16 General-Purpose Digital I/Os with Multipurpose Capability
- High-Performance, Low-Power, 16-Bit RISC Core
  - 1MHz–16MHz Operation, Approaching 1MIPS per 1MHz
  - Low Power (< 2.5mA/MIPS, DVDD = +2.5V)
  - 16-Bit Instruction Word, 16-Bit Data Bus
  - 33 Instructions (Most Require Only One Clock Cycle)
  - 16-Level Hardware Stack
  - Three Independent Data Pointers with Automatic Increment/Decrement
- Program and Data Memory
  - Internal 32KB Program Flash
  - Internal 4KB Data RAM
  - Internal 8KB Utility ROM
- Crystal/Clock Module
  - 1MHz–16MHz External Crystal Oscillator
  - 13.5MHz Internal RC Oscillator
  - External Clock Source Operation
- 16 x 16 Hardware Multiplier with 48-Bit Accumulator, Single Clock Cycle Operation
- Power-Management Module
  - Power-On Reset (POR)
  - Power-Supply Supervisor/Brownout Detection for All Supplies
  - On-Chip +5V, +3.3V, and +2.5V Regulators for Single Supply Operation
- JTAG Interface
  - Extensive Debug and Emulation Support
  - In-System Test Capability
  - Flash-Memory-Program Download
- UART
  - Synchronous and Asynchronous Transfers
  - Independent Baud-Rate Generator
  - 2-Wire Interface
  - Transmit and Receive FIFOs
- LIN
  - Supports LIN 1.3, LIN 2.0, and SAE J2602
  - Automatic Baud-Rate Detection and LIN Frame Synchronization
  - Up to 64 Bytes Frame Length
  - Automatic Calculation of Standard (LIN 1.3) and Enhanced (LIN 2.0) Checksums
- 7mm x 7mm, 48-Pin LQFP Package
- -40°C to +125°C Operating Temperature Range

16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

Detailed Description

The ultrasonic distance-measurement peripherals in the MAXQ7667 include a burst signal generator for acoustic transmission and mixed signal circuits for amplifying and digitizing echo signals ranging between 25kHz and 100kHz. The burst signal is a square wave with adjustable duty cycle and pulse count. The burst is derived either directly from the system clock or from a programmable PLL locked to the system clock. The MAXQ7667 effectively digitizes the echo signals received at the ECHOP and ECHON inputs using an LNA, sigma-delta ADC with variable analog gain amplifier, noise-limiting digital bandpass filter, digital full-wave rectifier, and a digital lowpass filter (see the *Typical Application Circuit/Functional Diagram*). The device detects echo signals at the burst frequency with amplitudes ranging from 10µV$_{P-P}$ to 100mV$_{P-P}$. Echoes greater than 100mV$_{P-P}$ and less than 2V$_{P-P}$ are internally clipped but do not saturate the receiver. To optimize echo reception, the clock used for processing the echo locks to the burst frequency. The MAXQ7667's burst generator can generate higher frequencies, but the maximum usable frequency for the echo receive path is 100kHz . For applications requiring transducer frequencies above 100kHz, implement an external echo receive path. The SAR ADC can then digitize the filtered echo envelope.

An integrated 16-bit RISC µC (MAXQ20) provides timing control, signal processing, and data I/O. The 16-bit Harvard architecture RISC core executes most instructions in a single clock cycle from instruction fetch to cycle completion. The MAXQ20 provides optimal performance for noise-sensitive analog applications.

The MAXQ7667 includes a 13.5MHz RC oscillator, external crystal oscillator, watchdog timer, schedule timer, three general-purpose Type 2 timers/counters, two 8-bit GPIO ports, SPI interface, JTAG interface, LIN capable UART interface, 12-bit SAR ADC with five multiplexed input channels, supply-voltage monitors, and a voltage reference for communication, diagnostics, and miscellaneous support.

Burst Controller

The MAXQ7667 provides a square-wave burst signal at the BURST output. Use the burst control to transmit an ultrasonic signal. Typical applications use the burst signal to switch an external transistor that drives a high-voltage transformer, which excites the transducer (see the *Typical Application Circuit/Functional Diagram*). Use software to configure the duty cycle, frequency, number of pulses, and drive current of the burst. See Section 17 of the *MAXQ7667 User's Guide*.

Derive the burst signal either directly from the system clock or from a programmable oscillator phase locked to the system clock (Figure 1). Using the system clock limits the burst frequency to one of 16 choices. Integer division of the system clock generates these 16 frequencies. The PLL allows a fractional division of the system clock. Any frequency within the PLL range is selectable to a resolution of 0.13% or better.

When using the internal PLL, connect external filter components (C1, R1, and C2) to FILT as shown in Figure 1. These components filter the analog voltage that controls the VCO in the PLL. The filter component values shown in the figure are suitable for the entire PLL frequency range.

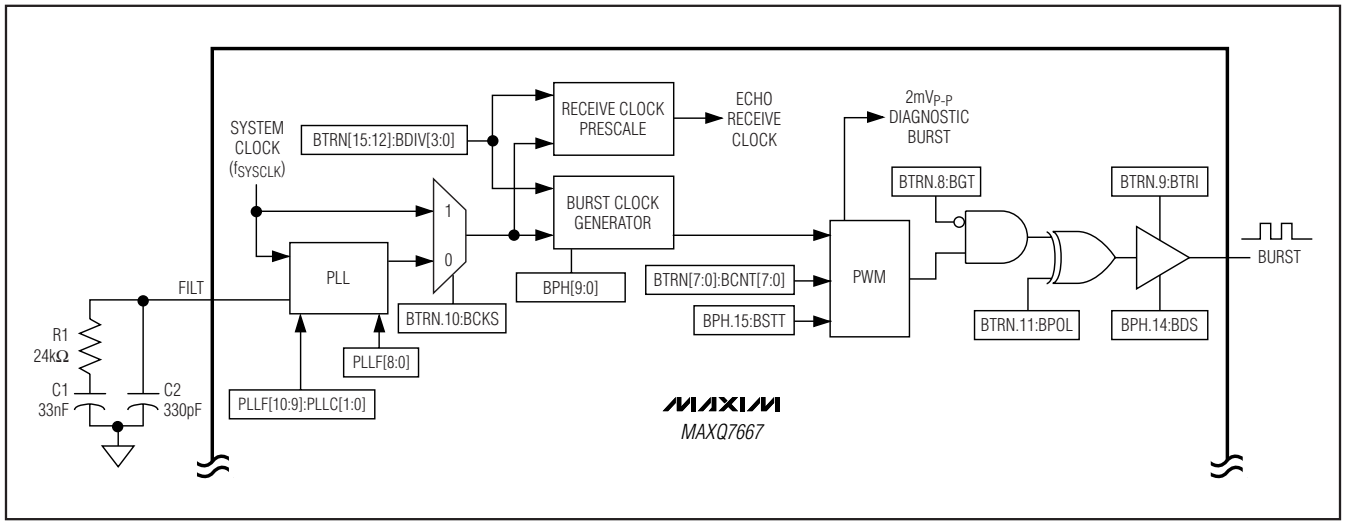

Figure 1. Burst Transmission Stage

Echo Receive Path

Low-Noise Amplifier (LNA)

The LNA provides a 40V/V fixed gain to the input signal. The differential inputs of the LNA are ECHOP and ECHON. For proper biasing of the LNA, AC-couple the transducer or any external circuitry to ECHOP and ECHON. For a single-ended input signal, AC-couple the signal to ECHOP with a 0.01µF capacitor and connect ECHON to AGND through a 0.01µF capacitor placed as close as possible to the signal source. The outputs of the LNA connect to the inputs of a 16-bit sigma-delta ADC and can connect internally to the AIN0 and AIN1 inputs of the SAR ADC for external monitoring (Figure 2).

Diagnostic Signals

An analog multiplexer located at the input of the LNA selects one of three possible signals for processing by the echo receive path; the normal echo signal AC-coupled to the ECHOP and ECHON inputs, 0V signal, or a $2mV_{P-P}$ internally generated signal (Figure 2). The $2mV_{P-P}$ square-wave signal, with frequency and duty cycle matching the burst signal, allows the echo receive chain to process a simulated echo.

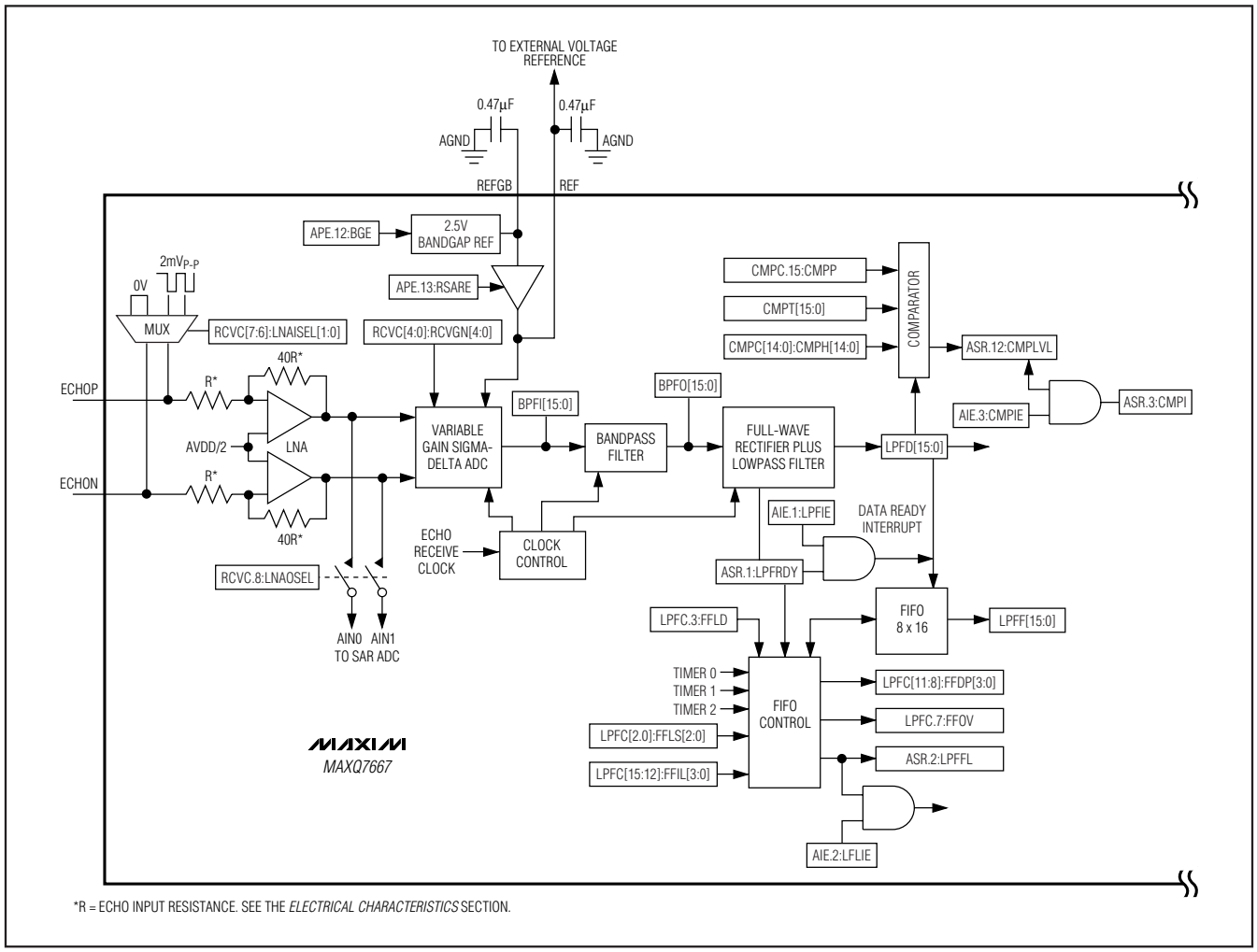

Figure 2. Echo Receive Path

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Sigma-Delta ADC

The MAXQ7667 features a 16-bit sigma-delta ADC with an analog gain adjustable from 38dB to 60dB (including the fixed LNA gain) with a maximum gain step of 12.5% (typical). Gain changes settle within one ADC conversion. Use software to create a virtual time variable gain amplifier. A digital bandpass and lowpass filters remove switching glitches and DC offset at the output of the ADC.

In a typical application, the software sets the gain to a low value when the burst is first sent and increases the gain as the time from when the burst was sent increases. As a result, strong echoes from nearby objects are processed without clipping while small signals from distant objects are processed with the maximum gain. The ADC samples the amplified echo signal from the LNA at 80 times the burst output frequency. The ADC provides conversion results at a data rate equal to 10 times the burst output frequency. The ADC conversion results also load to an 8-deep first-in-first-out (FIFO) at the native data rate or a separate time base without loading the CPU.

Digital Bandpass Filter

The digital bandpass filter has a center frequency that tracks the burst output frequency. The bandpass width is 14% of the center frequency. The bandpass filter provides the 16-bit output data at a data rate equal to 10 times the burst output frequency.

Full-Wave Rectifier

The full-wave rectifier detects the envelope of the digital bandwidth filter output to generate a DC output proportional to the peak-to-peak amplitude of the input signal. Full-wave rectification allows the digital lowpass filter to respond faster without excessive ripple.

Digital Lowpass Filter

The lowpass filter removes the ripple from the full-wave detector output. The output of the lowpass filter is available at a data rate equal to five times the burst output frequency. The corner frequency is 1/5 the burst frequency with approximately 40dB per decade rolloff. The 16-bit output data of the lowpass filter is stored in a FIFO register with a depth of eight samples. The MAXQ7667 allows data transfer from the lowpass filter

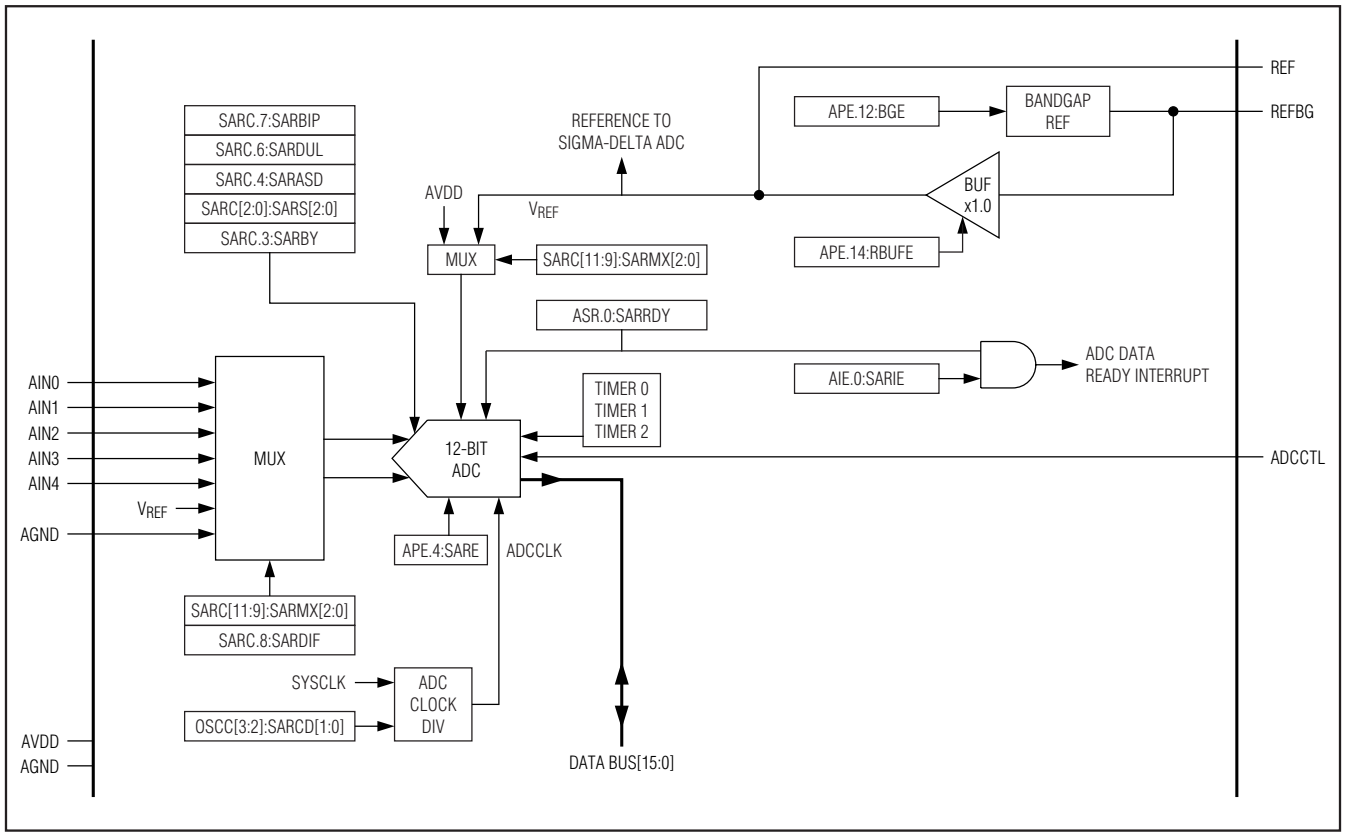

Figure 3. SAR ADC Block Diagram

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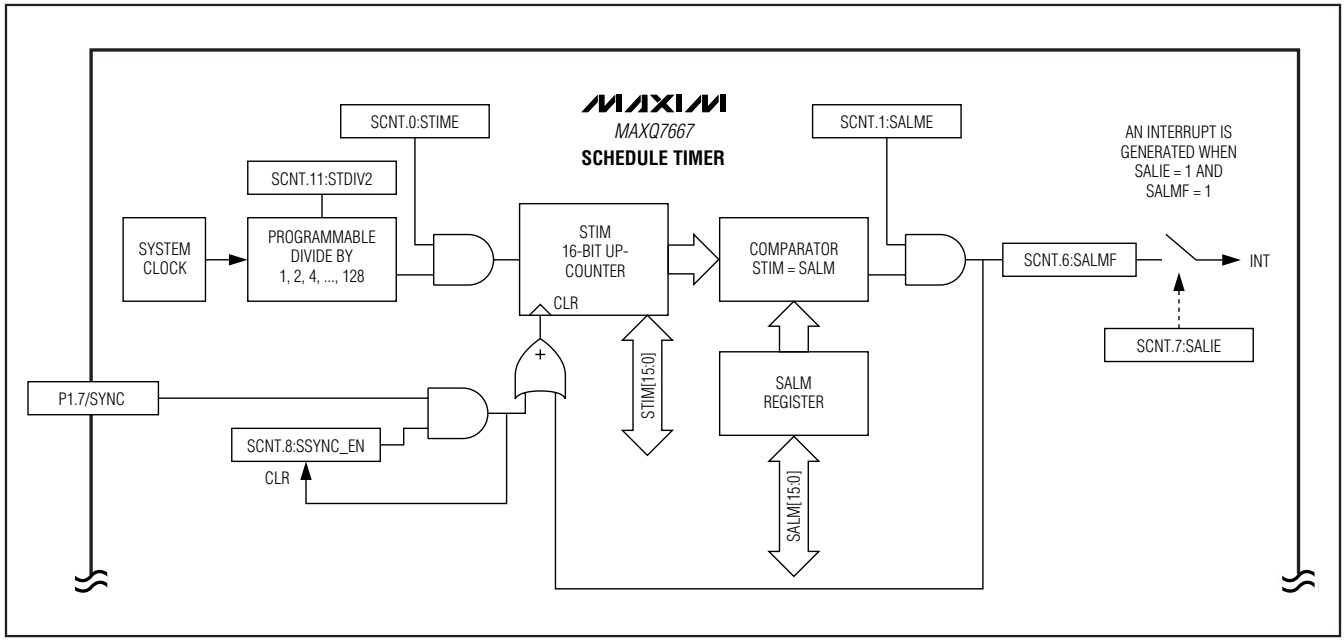

Figure 8. Schedule-Timer Module Block Diagram

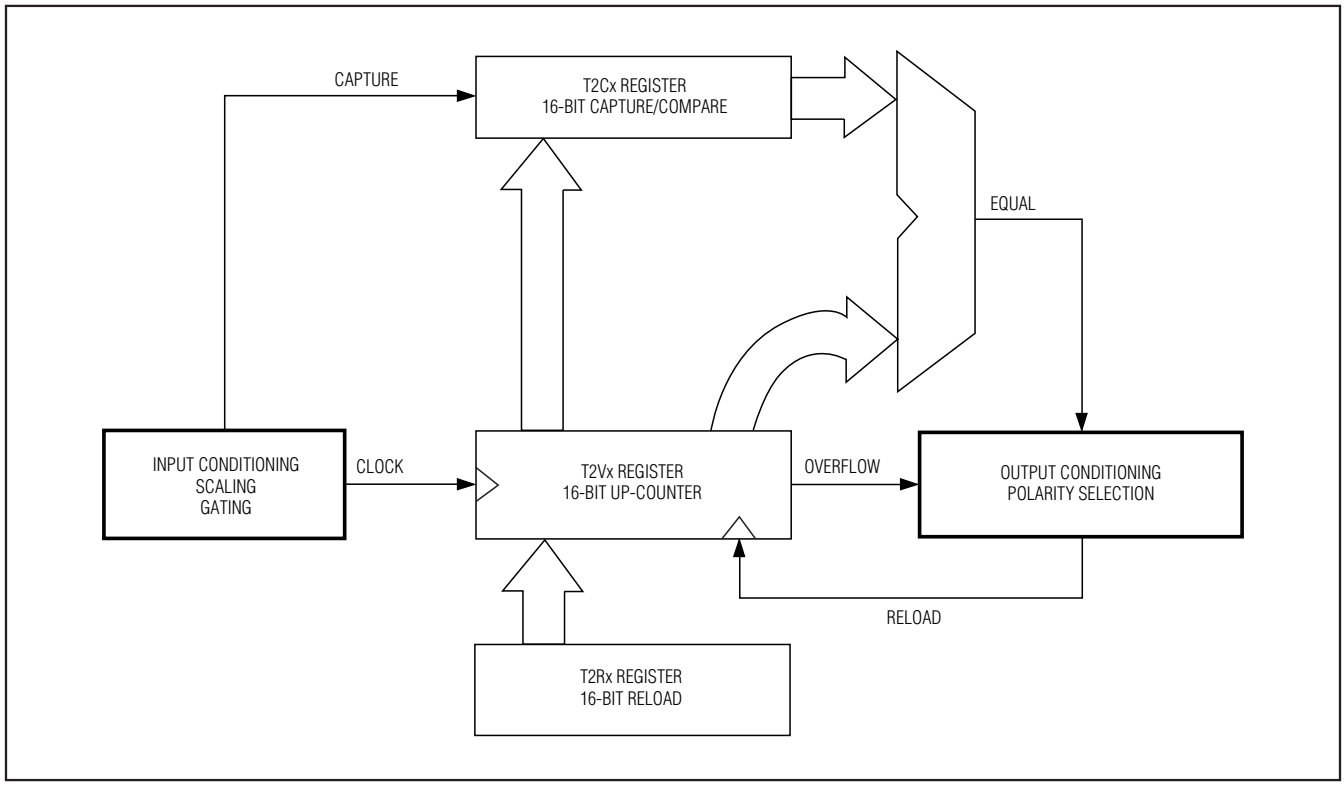

Figure 9. Type 2 Timer/Counter in 16-Bit Mode

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The following four digital I/Os form the TAP interface:

- TDO—Serial output signal for test instruction and data. Data transitions on the falling edge of TCK. TDO idles high when inactive. TDO serially transfers internal data to the external host. Data transfers lease significant bit first.
- TDI—Serial input signal for test instruction and data. Transition data on the rising edge of TCK. TDO pulls high when unconnected. TDI serially transfers data from the external host to the internal TAP module shift registers. Data transfers least significant bit first.
- TCK—Serial clock for the test logic. When TCK stops at 0, storage elements in the test logic must retain their data indefinitely. Force TCK high when inactive.
- TMS—Test mode selection. The rising edge of TCK samples the test signals at TMS. The TAP controller decodes the test signals at TMS to control the test operation. Force TMS high when inactive.

UART/LIN Interface

The MAXQ7667 includes a UART/LIN transceiver combination that supports communication speeds up 2MBd. The LIN standard for example limits communication speed to 20kBd or less. Connect a LIN transceiver or other UART connections such as RS-232 and RS-485 directly to the MAXQ7667's 2-wire interface: URX and UTX. The MAXQ7667 operates as a LIN slave or LIN master device. The UART provides the programmable baud-rate generators to communicate effectively to or from the LIN transceiver. The device holds up to 8 bytes of data in each of the transmit and receive FIFOs. The following characteristics apply to the MAXQ7667 UART/LIN interface:

- Full-duplex operation for asynchronous data transfers up to 500kBd (system clock/32)
- Half-duplex operation for synchronous data transfers up to 2MBd (system clock/8)
- 8-deep receive and transmit FIFO with programmable interrupt for receive and transmit
- Independent baud-rate generator
- Programmable 9th data bit (commonly used for parity or address/data selection)—UART mode only
- Hardware support for LIN including break detection, autobaud, address identity filtering, checksum calculation, and block length checking
- Supports common RS-232 and LIN baud rates: 1000, 1200, 2400, 4800, 9600, 19,200, 20,000, 38,400, 57,600, and 115,200 with system clock = 16MHz.

SPI Interface

The MAXQ7667 supports 4-wire SPI interface communication with 8-bit or 16-bit data streams operating in either master mode or slave mode. The SPI interface allows synchronous half-duplex or full-duplex serial data transfers to a wide variety of external serial devices using MISO, MOSI, SS, and SCLK signals. Collision detection is provided when two or more masters attempt a data transfer at the same time. See Section 9 of the *MAXQ7667 User's Guide*.

General-Purpose Digital I/O Ports

Two 8-bit digital I/O ports (P0._ and P1._), with dedicated one or more alternative functions, are available as general-purpose I/Os (GPIOs) under the control of the integrated MAXQ20. Set each I/O within each port individually as an input or output. The GPIOs incorporate a Schmitt trigger receiver and a full CMOS output driver (Figure 13). Each GPIO configures as an input with pullup to DVDDIO at power-up. When programmed as an input, each I/O is configurable for high-impedance, weak pullup to DVDDIO or pulldown to DGND. When programmed as an output, writing to the port output register (PO) controls the output logic state. The outputs source or sink at least 1.6mA. Configure the drive strength for each I/O within each port to high or low using the pad drive strength register for optimum EMI performance. All the I/O ports have interrupt capability that wake up the device while in stop mode and have protection circuitry to DVDDIO and DGND.

Supply-Voltage Regulators

The MAXQ7667 requires three different power-supply voltages. DVDDIO, nominally +5V, allows interfacing to standard 5V logic on all the digital I/Os including the LIN/UART, JTAG, and SPI ports. DVDD, nominally +2.5V, powers all the high-speed digital circuits. AVDD, nominally 3.3V, powers the analog circuits.

External power supplies or internal voltage regulators provide each of the supply voltages. The internal voltage regulators provide 3.3V and 2.5V supplies from the 5V DVDDIO input. Obtain the 5V supply from a higher external voltage supply by using a few external components. The MAXQ7667 includes an internal error amplifier used to regulate the voltage on DVDDIO by driving the gate or base of an external pass transistor. Refer to the *MAXQ7667 User's Guide* for more details on the external components needed for 5V regulation.

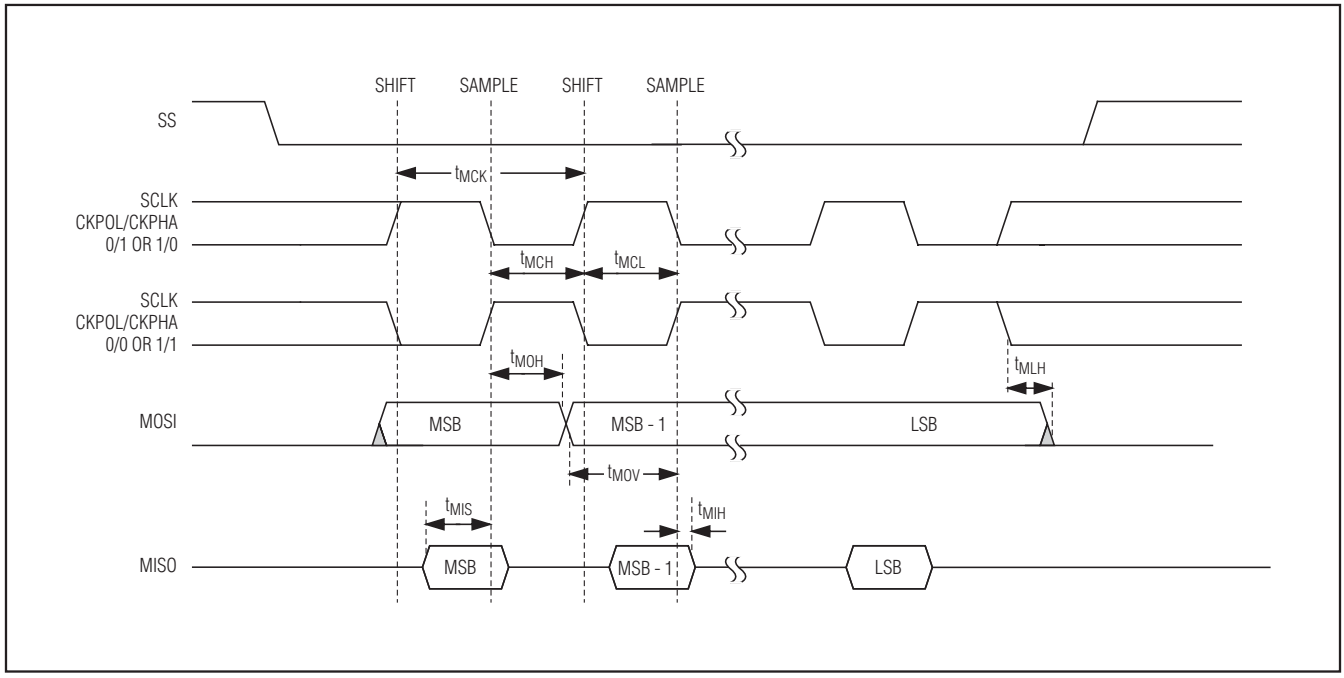

Figure 11. SPI Timing Diagram in Master Mode

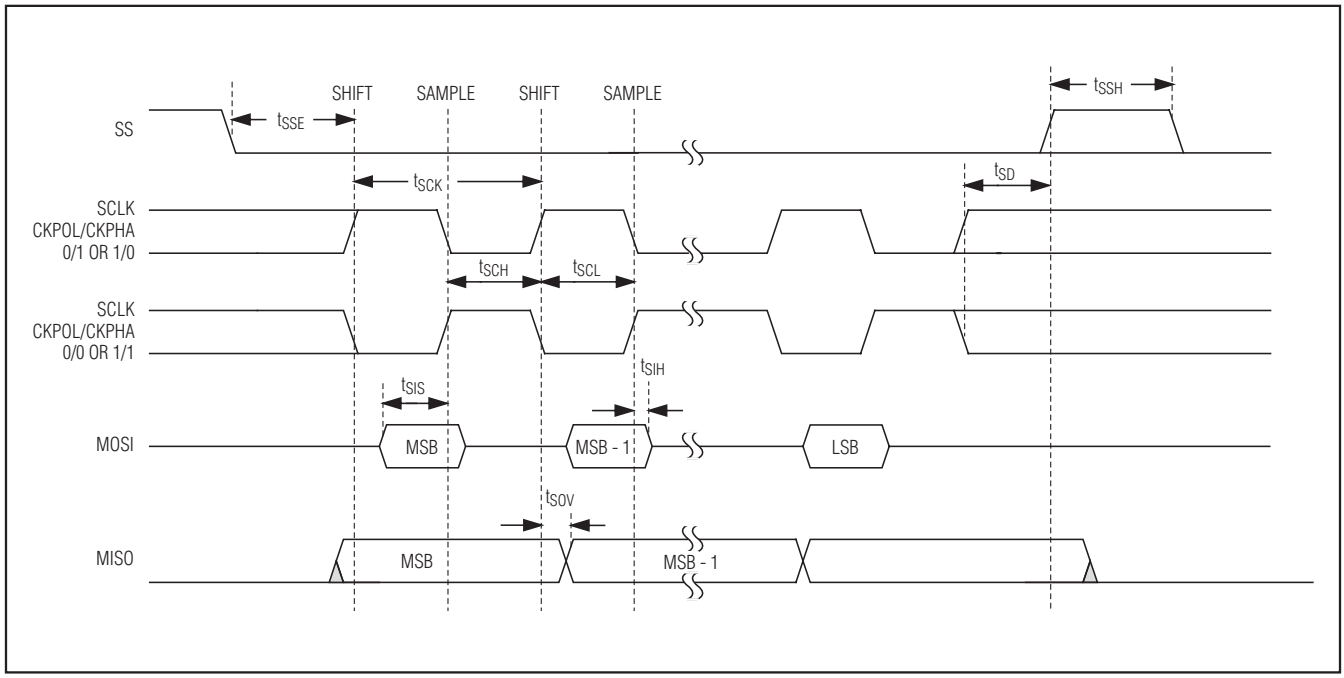

Figure 12. SPI Timing Diagram in Slave Mode

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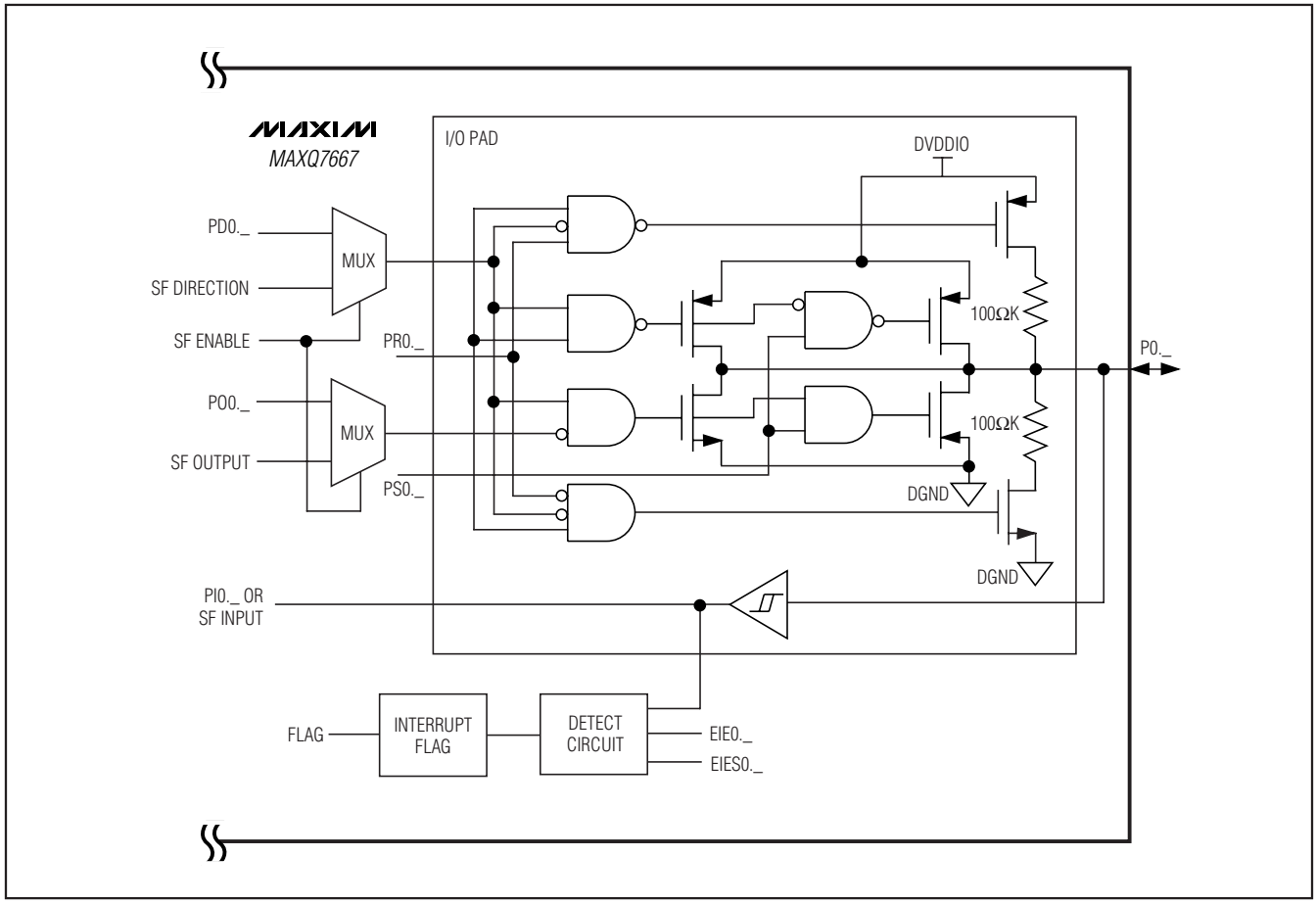

Figure 13. Port 0 Digital I/O Basic Circuitry. Port 1 Circuitry is the Same as Port 2.

Connect bypass capacitors at each power-supply input as close as possible to the device. Use a bypass capacitor less than 0.47µF on DVDDIO. For most applications, 0.1µF bypass capacitors are adequate.

Supply Brownout Monitor

Power supplies DVDD, AVDD, and DVDDIO each include a brownout monitor/supervisor that alerts the µC when their corresponding supply voltages drop below the interrupt threshold. Activate each brownout monitor independently using the corresponding brownout enable bits: VDBE, VIBE, and VABE.

Reset

In reset mode, no instruction execution occurs and all inputs/outputs return to their default states. Code execution resumes at address 8000h (in the utility ROM) once the reset condition is removed.

Four different sources reset the MAXQ7667: POR, watchdog timer reset, external reset, and internal system reset.

During normal operation, force $\overline{\text{RESET}}$ low for at least four system clock cycles for an external reset. Set the ROD bit in the SC register, while the SPE bit in the ICDF register is set, for an internal system reset. See Section 16 of the *MAXQ7667 User's Guide*.

Power-On Reset (POR)

The MAXQ7667 includes a DVDD voltage supervisor to control the µC POR. On power-up, internal circuitry pulls $\overline{\text{RESET}}$ low and resets all the internal registers. $\overline{\text{RESET}}$ is held low for the duration of the power-on delay after V_{DVDD} rises above the DVDD reset threshold. The internal RC oscillator starts up and software execution begins at the reset vector location 8000h immediately after the device exits POR while $\overline{\text{RESET}}$ is

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memory. Access physical memory segments (other than the stack and register memories) as either program memory or data memory, but not both at once.

By default, the memory is arranged in a Harvard architecture, with separate address spaces for program and data memory. The configuration of program and data space depends on the current execution location.

- When executing code from flash memory, access the SRAM and utility ROM in data space.
- When executing code from SRAM, access the flash memory and utility ROM in data space.
- When executing code from the utility ROM, access the flash memory and SRAM in data space.

Utility ROM (see Section 18 of the MAXQ7667 User's Guide)

The utility ROM is a 4K x 16 block of internal ROM memory that defaults to a starting address of 8000h. The utility ROM consists of subroutines called from application software. The subroutines include:

- In-system programming (bootloader) over the JTAG or UART interface
- In-circuit debug routines
- Test routines (internal memory tests, memory loader, etc.)
- User-callable routines for in-application flash programming and code space table lookup

Following any reset, execution begins in the utility ROM. The ROM software determines whether the program execution immediately jumps to the start of the user-application code (located at address 0000h) or to one of the special routines mentioned above. Call the routines within the utility ROM using the application software. Refer to the *MAXQ7667 User's Guide* for more information on the utility ROM contents.

Password protect in-system programming, in-application programming, and in-circuit debugging functions using a password-lock (PWL) bit. The PWL bit is implemented in the SC register. When the PWL bit is set to one (POR default), the password is required to access the utility ROM, including in-circuit debug and in-system programming routines that allow reading or writing of internal memory. When the PWL bit is cleared to zero, these utilities are fully accessible without the password. The password is automatically set to all ones following a mass erase.

Data Memory

The 2K x 16 internal data SRAM maps into either program or data space. The contents of the SRAM are maintained during stop mode and across non-POR resets, as long as DVDD remains within the operating voltage range.

A data memory cycle requires only one system clock period to support fast internal execution. This allows a complete read or write operation on SRAM in one clock cycle. The MMU handles data memory mapping and access control. Read or write to the data memory with word or byte-wide commands.

Stack Memory

The MAXQ7667 provides a 16 x 16 hardware stack to support subroutine calls and system interrupts. A 16-bit wide internal hardware stack provides storage for program return addresses and general-purpose use. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and interrupts serviced.

Register Set

Sets of registers control most functions. These registers provide a working space for memory operations as well as configuring and addressing peripheral registers on the device. Registers are divided into two major types; system registers and peripheral registers. The register set common to most MAXQ-based devices, also known as the system registers, includes the ALU, accumulator registers, data pointers, interrupt vectors and control, and stack pointer. The peripheral registers define additional functionality. Tables 1 and 3 show the MAXQ7667 register set.

Programming

Two different methods program the flash memory: in-system programming and in-application programming. Both methods afford great flexibility in system design as well as reduce the life-cycle cost of the embedded system. The MAXQ7667 password protects these features to prevent unauthorized access to code memory.

In-System Programming

An internal bootstrap loader reloads the device over a simple JTAG or UART interface allowing cost savings in system software upgrade. During power-up, the MAXQ7667 first checks for activity on the JTAG port. If no activity is present, the device checks if a password-protected program is present. If the password is set,

Table 1. System Register Map

REGISTER INDEX	MODULE NAME (BASE SPECIFIER)						
	AP (8h)	A (9h)	PFX (Bh)	IP (Ch)	SP (Dh)	DPC (Eh)	DP (Fh)
0h	AP	**A[0]**	**PFX[0]**	**IP**	—	—	—
1h	APC	**A[1]**	**PFX[1]**	—	**SP**	—	—
2h	—	**A[2]**	**PFX[2]**	—	**IV**	—	—
3h	—	**A[3]**	**PFX[3]**	—	—	OFFS	**DP[0]**
4h	PSF	**A[4]**	**PFX[4]**	—	—	**DPC**	—
5h	IC	**A[5]**	**PFX[5]**	—	—	**GR**	—
6h	IMR	**A[6]**	**PFX[6]**	—	**LC[0]**	GRL	—
7h	—	**A[7]**	**PFX[7]**	—	**LC[1]**	**BP**	**DP[1]**
8h	SC	**A[8]**		—	—	***GRS***	—
9h	—	**A[9]**	—	—	—	GRH	—
Ah	—	**A[10]**	—	—	—	***GRXL***	—
Bh	*IIR*	**A[11]**	—	—	—	***FP***	—
Ch	—	**A[12]**	—	—	—	—	—
Dh	—	**A[13]**	—	—	—	—	—
Eh	CKCN	**A[14]**	—	—	—	—	—
Fh	WDCN	**A[15]**	—	—	—	—	—

Note: *Registers in italics are read-only. Registers in bold are 16-bit wide.*

Table 3. Peripheral Register Map

REGISTER INDEX	MODULE NAME (BASE SPECIFIER)					
	M0 (0h)	M1 (1h)	M2 (2h)	M3 (3h)	M4 (4h)	M5 (5h)
0h	PO0	MCNT	T2CNA0	T2CNA2	—	BPH
1h	PO1	MA	T2H0	T2H2	—	BTRN
2h	—	MB	T2RH0	T2RH2	—	SARC
3h	EIF0	MC2	T2CH0	T2CH2	—	RCVC
4h	EIF1	MC1	T2CNA1	—	—	PLLF
5h	—	MC0	T2H1	CNT1	—	AIE
6h	—	SPIB	T2RH1	SCON	—	CMPC
7h	—	SPICN	T2CH1	SBUF	—	CMPT
8h	PI0	SPICF	T2CNB0	T2CNB2	—	ASR
9h	PI1	SPICK	T2V0	T2V2	—	SARD
Ah	—	—	T2R0	T2R2	—	LPFC
Bh	EIE0	—	T2C0	T2C2	—	OSCC
Ch	EIE1	MC1R	T2CNB1	FSTAT	—	BPFI
Dh	—	MC0R	T2V1	ERRR	—	BPFO
Eh	—	SCNT	T2R1	CHKSUM	—	LPFD
Fh	—	STIM	T2C1	ISVEC	—	LPFF
10h	PD0	SALM	T2CFG0	T2CFG2	—	APE
11h	PD1	FPCTL	T2CFG1	STA0	—	—
12h	—	—	—	SMD	—	FGAIN
13h	EIES0	—	—	FCON	—	B1COEF
14h	EIES1	—	—	CNT0	—	B2COEF
15h	—	—	—	CNT2	—	B3COEF
16h	—	—	—	IDFB	—	A2A
17h	—	RCTRM	—	SADDR	—	A2B
18h	PS0	—	ICDT0	SADEN	—	—
19h	PS1	—	ICDT1	BT	—	A2D
1Ah	—	—	ICDC	TMR	—	—
1Bh	PR0	—	ICDF	—	—	A3A
1Ch	PR1	ID0	ICDB	—	—	A3B
1Dh	—	ID1	ICDA	—	—	—
1Eh	—	—	ICDD	—	—	A3D
1Fh	—	—	—	—	—	—

Table 4. Peripheral Register Bit Functions and Reset Values (continued)

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BT	BT15	BT14	BT13	BT12	BT11	BT10	BT9	BT8	BT7	BT6	BT5	BT4	BT3	BT2	BT1	BT0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TMR	TMR15	TMR14	TMR13	TMR12	TMR11	TMR10	TMR9	TMR8	TMR7	TMR6	TMR5	TMR4	TMR3	TMR2	TMR1	TMR0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BPH	BSTT	BDS	—	—	—	—	BPH9	BPH8	BPH7	BPH6	BPH5	BPH4	BPH3	BPH2	BPH1	BPH0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BTRN	BDIV3	BDIV2	BDIV1	BDIV0	BPOL	BCKS	BTRI	BGT	BCTN7	BCTN6	BCTN5	BCTN4	BCTN3	BCTN2	BCTN1	BCTN0
	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
SARC	—	—	—	—	SARMX2	SARMX1	SARMX0	SARDIF	SARBIP	SARDUL	SARRSEL	SARASD	SARBY	SARC2	SARC1	SARC0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RCVC	—	—	—	—	—	—	—	LNAOSEL	LNAISEL1	LNAISEL0	—	RCVGN4	RCVGN3	RCVGN2	RCVGN1	RCVGN0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PLLF	—	—	—	—	—	PLLC1	PLLC0	PLLF8	PLLF7	PLLF6	PLLF5	PLLF4	PLLF3	PLLF2	PLLF1	PLLF0
	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
AIE	—	—	—	—	—	—	—	—	XTIE	VIBIE	VDBIE	VABIE	CMPIE	LFLIE	LPFIE	SARIE
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CMPC	CMPP	CMPH14	CMPH13	CMPH12	CMPH11	CMPH10	CMPH9	CMPH8	CMPH7	CMPH6	CMPH5	CMPH4	CMPH3	CMPH2	CMPH1	CMPH0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CMPT	CMPT15	CMPT14	CMPT13	CMPT12	CMPT11	CMPT10	CMPT9	CMPT8	CMPT7	CMPT6	CMPT5	CMPT4	CMPT3	CMPT2	CMPT1	CMPT0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ASR	VIOLVL	DVLVL	AVLVL	CMPLVL	—	—	—	XTRDY	XTI	VIBI	VDBI	VABI	CMPI	LPFFL	LPFRDY	SARRDY
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SARD	—	—	—	—	SARD11	SARD10	SARD9	SARD8	SARD7	SARD6	SARD5	SARD4	SARD3	SARD2	SARD1	SARD0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LPFC	FFIL3	FFIL2	FFIL1	FFIL0	FFDP3	FFDP2	FFDP1	FFDP0	FFOV	—	—	—	FFLD	FFLS2	FFLS1	FFLS0
	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
OSCC	—	—	—	—	—	—	—	—	—	—	—	—	SARCD1	SARCD0	XTE	RCE
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BPFI	BPFI15	BPFI14	BPFI13	BPFI12	BPFI11	BPFI10	BPFI9	BPFI8	BPFI7	BPFI6	BPFI5	BPFI4	BPFI3	BPFI2	BPFI1	BPFI0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BPFO	BPFO15	BPFO14	BPFO13	BPFO12	BPFO11	BPFO10	BPFO9	BPFO8	BPFO7	BPFO6	BPFO5	BPFO4	BPFO3	BPFO2	BPFO1	BPFO0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LPFD	LPFD15	LPFD14	LPFD13	LPFD12	LPFD11	LPFD10	LPFD9	LPFD8	LPFD7	LPFD6	LPFD5	LPFD4	LPFD3	LPFD2	LPFD1	LPFD0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LPFF	LPFF15	LPFF14	LPFF13	LPFF12	LPFF11	LPFF10	LPFF9	LPFF8	LPFF7	LPFF6	LPFF5	LPFF4	LPFF3	LPFF2	LPFF1	LPFF0
	NOT INITIALIZED															
APE	—	RBUFE	RSARE	BGE	LRIOPD	LRDPD	LRAPD	VIBE	VDPE	VDBE	VABE	SARE	PLLE	MDE	LNAE	BIASE
	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

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Applications Information

Development and Technical Support

A variety of highly versatile, affordably priced development tools for this µC are available from Maxim and third-party suppliers, including:

– Compilers

– Evaluation kit

– Integrated development environments (IDEs)

– JTAG-to-serial converters for programming and debugging

A partial list of development tool vendors can be found at **www.maxim-ic.com/MAXQ_tools**.

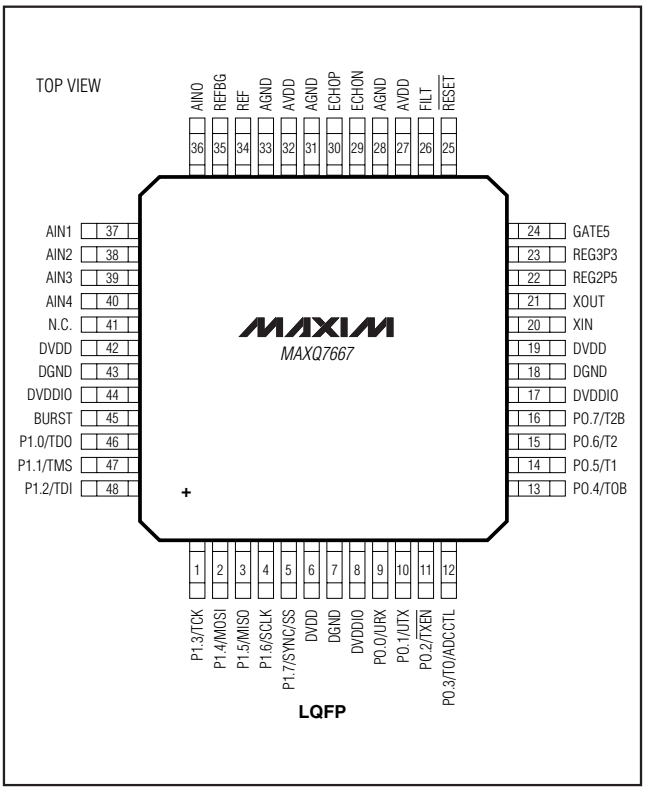
Technical support is available at **https://support.maxim-ic.com/micro**.

Additional Documentation

Designers must have the following documents to fully use all the features of this device. This data sheet contains pin descriptions, feature overviews, and electrical specifications. Errata sheets contain deviations from published specifications. The user's guides offer detailed information about device features and operation. The following documents can be downloaded from **www.maxim-ic.com/microcontrollers**.

- This MAXQ7667 data sheet, which contains electrical/timing specifications and pin descriptions.
- The MAXQ7667 revision-specific errata sheet (**www.maxim-ic.com/errata**).
- The *MAXQ7667 Family User's Guide*, which contains detailed information on core features and operation, including programming.

Pin Configuration



Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 LQFP	C48+2	**21-0054**