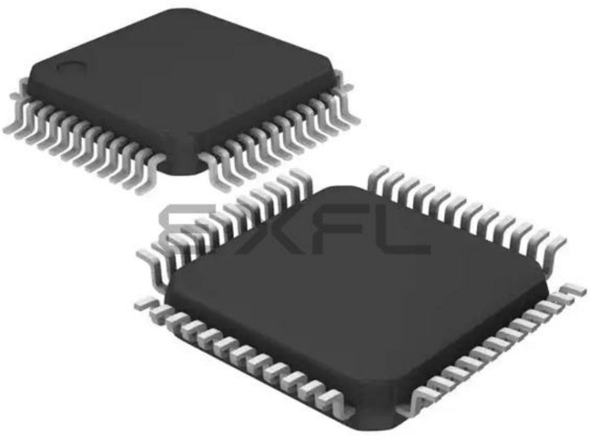
Analog Devices Inc./Maxim Integrated - MAXQ7667AACM/V+GB Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	-
Core Size	16-Bit
Speed	16MHz
Connectivity	LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	16
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 2.75V
Data Converters	A/D 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq7667aacm-v-gb

16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

ABSOLUTE MAXIMUM RATINGS

DVDDIO, GATE5, REG3P3, REG2P5 to
DGND ....-0.3V to +6.0V
AVDD to AGND ....-0.3V to +4.0V
DVDD to DGND ....-0.3V to +3.0V
DVDDIO to DVDD ....-0.3V to +6.0V
AVDD to DVDD ....-0.3V to +4.0V
AGND to DGND..-0.3V to +0.3V
Digital Inputs/Outputs to DGND..........-0.3V to (V_{DVDDIO} + 0.3V)
Analog Inputs/Outputs to AGND ....-0.3V to (V_{AVDD} + 0.3V)
XIN, XOUT to DGND ....-0.3V to (V_{DVDD} + 0.3V)
Maximum Current into Any Pin...50mA
Continuous Power Dissipation (T_A = +70°C)
48-Pin LQFP (derate 21.7mW/°C above +70°C).....1739.1mW
Operating Temperature Range ....-40°C to +125°C
Storage Temperature Range ....-60°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DVDDIO} = +5V, V_{AVDD} = +3.3V; V_{DVDD} = +2.5V, system clock (f_{SYSCLK}) = 16MHz, burst frequency (f_{BURST}) = bandpass frequency (f_{BPF}) = 50kHz, C_{REFBG} = C_{REF} = 1µF in parallel with 0.01µF, f_{ADCCLK} = 2MHz (SAR data rate = 125ksps), T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ECHO INPUT (Low-Noise Amplifier and Sigma-Delta ADC)						
Input-Referred Noise (Note 1)		VGA gain adjust = 1.55µV_{P-P}/LSB		5.6		µV_{RMS}
		VGA gain adjust = 0.1µV_{P-P}/LSB		0.7		
Minimum Detectable Signal		VGA gain adjust = 1.55µV_{P-P}/LSB		80		µV_{P-P}
		VGA gain adjust = 0.1µV_{P-P}/LSB		10		
Operating Input Range		VGA gain adjust = 1.55µV_{P-P}/LSB, unclipped		100		mV_{P-P}
		VGA gain adjust = 0.1µV_{P-P}/LSB, unclipped		6.7		
Programmable Gain		From echo input to bandpass filter in reply to input: VGA gain adjust = 1.55µV_{P-P}/LSB		1.55		µV_{P-P}/LSB
		From echo input to bandpass filter in reply to input: VGA gain adjust = 0.1µV_{P-P}/LSB		0.1		
Programmable-Gain Adjust Resolution		(Note 2)		10		%
LNA Bandwidth				150		kHz
ADC Sampling Rate				80 x f_{BPF}		kHz
ADC Output Data Rate				10 x f_{BPF}		kHz
ADC Output Data Resolution				16		Bits
Echo-Input Resistance	R_{IN}	For each echo input		14		kΩ
Echo-Input Capacitance				14		pF
Echo-Input DC Bias Voltage				V_{AVDD}/2		V
Maximum Overvoltage Recovery Time		Recover from 2V_{P-P} input		10		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5V, V_{AVDD} = +3.3V; V_{DVDD} = +2.5V, system clock (f_{SYSCLK}) = 16MHz, burst frequency (f_{BURST}) = bandpass frequency (f_{BPF}) = 50kHz, C_{REFBG} = C_{REF} = 1µF in parallel with 0.01µF, f_{ADCCLK} = 2MHz (SAR data rate = 125ksps), T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE BUFFER						
Offset				5		mV
Minimum Load			2.5			kΩ
Output Bypass Capacitor				0.47		µF
EXTERNAL VOLTAGE REFERENCE (Reference Buffer Disabled)						
Reference Input Range		Applied at REF	1.0		V_{AVDD}	V
Reference Input Impedance		Measured at REF with the SAR and sigma-delta ADCs running at maximum frequency		50		kΩ
INTERNAL VOLTAGE REFERENCE (REFBG)						
Initial Accuracy			2.45	2.5	2.55	V
Maximum Temperature Coefficient				100		ppm/°C
Output Impedance				1.1		kΩ
Power-Supply Rejection Ratio		V_{AVDD} = 3.0V to 3.6V		60		dB
Output Noise				0.5		mV_{RMS}
PROGRAMMABLE BURST-FREQUENCY OSCILLATOR						
Burst-Frequency Range			0.025		1.335	MHz
Burst-Frequency Resolution				0.1		%
Burst-Frequency Locking Time		Change from 40kHz to 60kHz		5		ms
		Change from 50kHz to 50.5kHz		2		
CRYSTAL OSCILLATOR						
Frequency Range		Tested crystal frequency		16		MHz
		Minimum crystal frequency		4		
		External clock input	4		16	
Temperature Stability		Excluding crystal		25		ppm/°C
Startup Time		16MHz crystal		10		ms
XIN Input Low Voltage		When driven with external clock source			0.3 x V_{DVDD}	V
XIN Input High Voltage		When driven with external clock source	0.7 x V_{DVDD}			V
INTERNAL RC OSCILLATOR						
Frequency				13.5		MHz
Initial Accuracy				10.5		%
Temperature Drift		T_A = T_{MIN} to T_{MAX}		700		ppm
Supply Rejection		V_{DVDD} = 2.25V to 2.75V		-1.5		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5V, V_{AVDD} = +3.3V; V_{DVDD} = +2.5V, system clock (f_{SYSCLK}) = 16MHz, burst frequency (f_{BURST}) = bandpass frequency (f_{BPF}) = 50kHz, C_{REFBG} = C_{REF} = 1µF in parallel with 0.01µF, f_{ADCCLK} = 2MHz (SAR data rate = 125ksps), T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Adjustable Frequency Range		Using the RCTRM register	-40		+40	%
Frequency Adjustment Resolution				0.2		%
SUPPLY VOLTAGE SUPERVISORS						
DVDD Reset Threshold		Asserts $\overline{RESET}$ if V_{DVDD} falls below this threshold	2.10		2.25	V
DVDD Interrupt Threshold		Generates an interrupt if V_{DVDD} falls below this threshold	2.25		2.38	V
Minimum Reset and Interrupt Threshold Difference			150			mV
AVDD Interrupt Threshold		Generates an interrupt if V_{AVDD} falls below this threshold	2.95		3.15	V
DVDDIO Interrupt Threshold		Generates an interrupt if V_{DVDDIO} falls below this threshold	4.5		4.75	V
Supervisor Operating Range		At DVDD	1.5		2.75	V
Supervisor Hysteresis				1		%
$\overline{RESET}$ Release Delay		After V_{DVDD} rises above the reset threshold		35		µs
Power-Up Time		Time from $\overline{RESET}$ is released to the execution of the first instruction (serial bootloader off)		1		µs
+5V LINEAR REGULATOR (DVDDIO, GATE5, Requires External Pass Transistor, see the *Typical Application Circuit/Functional Diagram*)						
Regulator Output Voltage		At DVDDIO	4.75		5.25	V
GATE5 Output High Voltage		I_{SOURCE} = 0µA (no load)	V_{DVDDIO} - 0.1			V
GATE5 Output Low Voltage		I_{SINK} = 500µA			2	V
GATE5 Output Resistance		I_{SINK} = 0µA to 50µA		330		Ω
Gain Bandwidth		DVDDIO to GATE5		1.58		kHz
Gain		DVDDIO to GATE5		1700		V/V
GATE5 Slew Rate				4.3		V/ms
Maximum Load Capacitance		Maximum capacitance on DVDDIO when using an external pass transistor		1		µF
+3.3V LINEAR REGULATOR (REG3P3)						
REG3P3 Output Voltage			3.15		3.45	V
Load Current					50	mA
Output Short-Circuit Current		REG3P3 shorted to AGND		150		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5V, V_{AVDD} = +3.3V; V_{DVDD} = +2.5V, system clock (f_{SYSCLK}) = 16MHz, burst frequency (f_{BURST}) = bandpass frequency (f_{BPF}) = 50kHz, C_{REFBG} = C_{REF} = 1µF in parallel with 0.01µF, f_{ADCCLK} = 2MHz (SAR data rate = 125ksps), T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

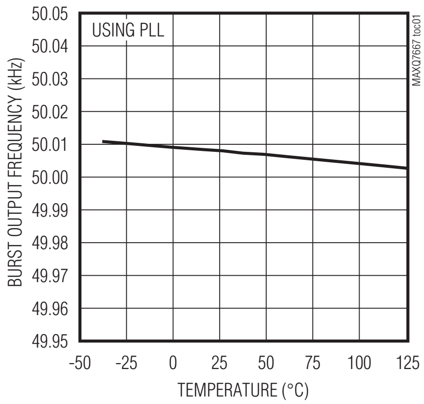
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
+2.5V LINEAR REGULATOR (REG2P5)						
REG2P5 Output Voltage			2.38		2.62	V
Load Current					50	mA
Output Short-Circuit Current		REG2P5 shorted to DGND		100		mA
POWER REQUIREMENTS						
Supply Voltage Range		DVDD	2.25	2.5	2.75	V
		AVDD	3.00	3.3	3.6	V
		DVDDIO	4.5	5.0	5.5	V
AVDD Supply Current		All analog functions enabled		12	18	mA
		All analog functions disabled		3	10	µA
		Incremental AVDD supply current: LNA		2.4		mA
		Incremental AVDD supply current: Sigma-delta ADC		12		mA
		Incremental AVDD supply current: SAR ADC, 250ksps, f_{ADCCLK} = 4MHz		600		µA
		Incremental AVDD supply current: PLL		300		µA
		Incremental AVDD supply current: Supply voltage supervisors		3		µA
		Incremental AVDD supply current: Internal voltage reference		220		µA
		Incremental AVDD supply current: Reference buffer		300		µA
		Incremental AVDD supply current: Bias (any AVDD module enabled)		1.5		mA
DVDD Supply Current				11		mA
DVDDIO Supply Current				2.5		mA
DIGITAL INPUTS (GPIO, UART, JTAG, SPI™)						
Input High Voltage			V_{DVDDIO} - 1			V
Input Low Voltage					0.8	V
Input Hysteresis		V_{DVDDIO} = 5.0V		500		mV
Input Leakage Current		Digital input voltage = DGND or DVDDIO, pullup disabled		±0.01	±1	µA
Pullup/Pulldown Resistance		Pulled up to DVDDIO internally, pulled down to DGND internally		150		kΩ
Input Capacitance				15		pF

SPI is a trademark of Motorola, Inc.

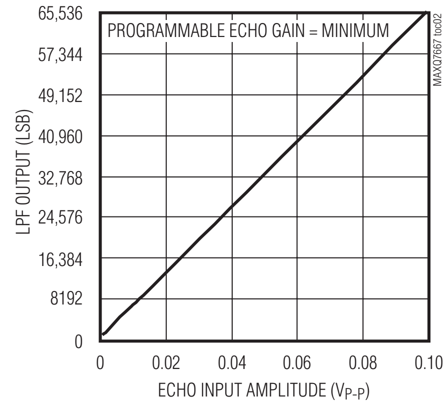
Typical Operating Characteristics

(V_{DVDDIO} = +5V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, f_{SYSCLK} = 16MHz, burst frequency = bandpass frequency = 50kHz, T_A = +25°C, unless otherwise noted.)

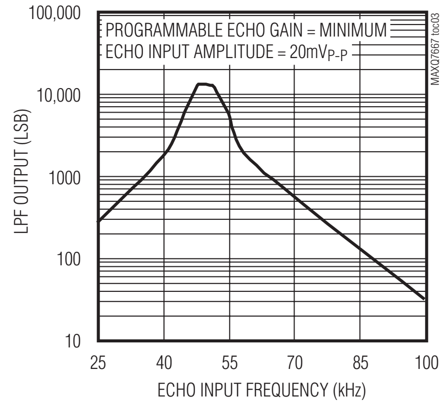
BURST OUTPUT FREQUENCY vs. TEMPERATURE



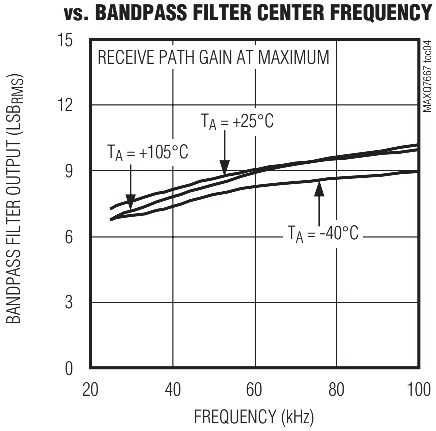
LOWPASS FILTER OUTPUT vs. ECHO INPUT AMPLITUDE



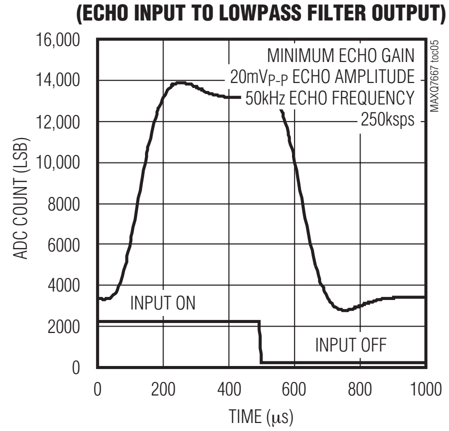
LOWPASS FILTER OUTPUT vs. ECHO INPUT FREQUENCY



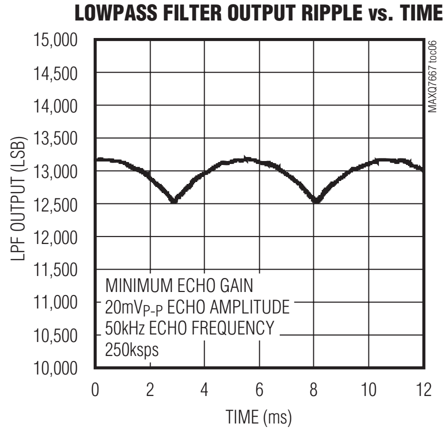
BANDPASS FILTER OUTPUT NOISE FLOOR vs. BANDPASS FILTER CENTER FREQUENCY



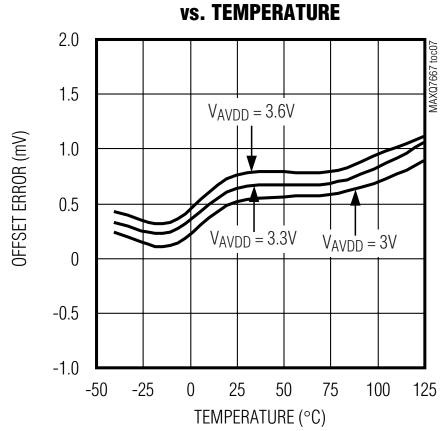
RECEIVE PATH RESPONSE TIME (ECHO INPUT TO LOWPASS FILTER OUTPUT)



LOWPASS FILTER OUTPUT RIPPLE vs. TIME



SAR ADC OFFSET ERROR vs. TEMPERATURE

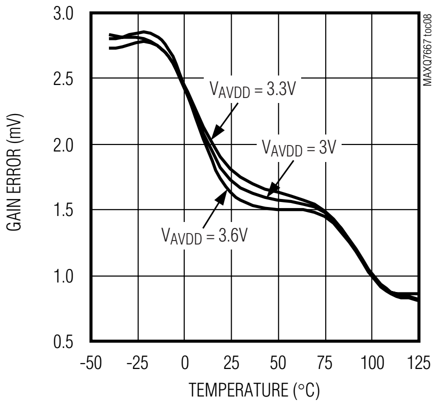


16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

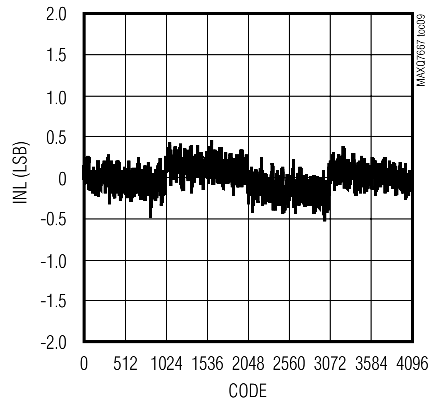
Typical Operating Characteristics (continued)

(V_{DVDDIO} = +5V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, f_{SYSCLK} = 16MHz, burst frequency = bandpass frequency = 50kHz, T_A = +25°C, unless otherwise noted.)

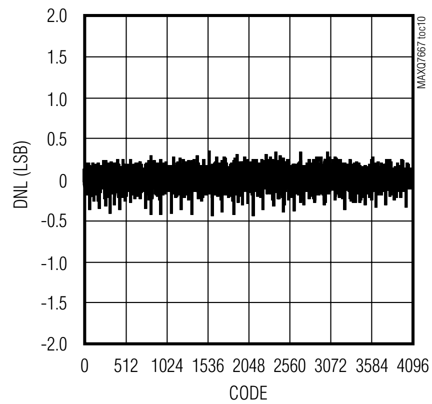
SAR ADC GAIN ERROR vs. TEMPERATURE



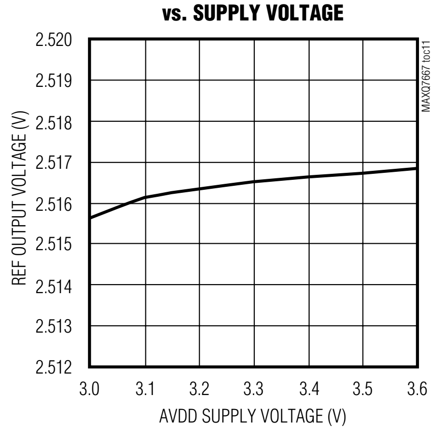
SAR ADC INL vs. CODE



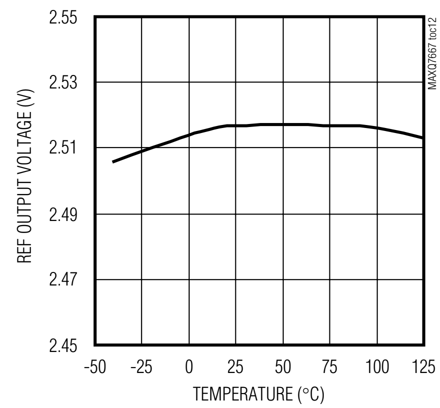
SAR ADC DNL vs. CODE



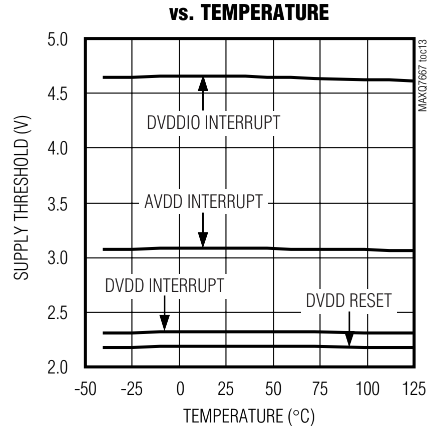
REFERENCE OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



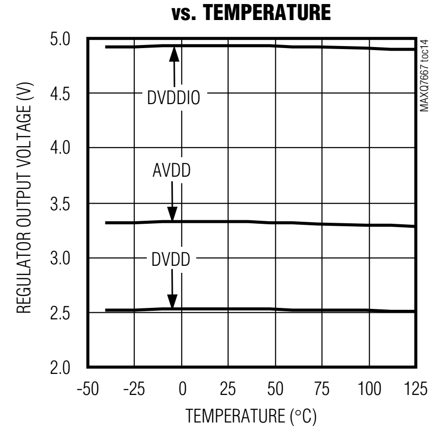
REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE



SUPPLY BROWNOUT THRESHOLDS vs. TEMPERATURE



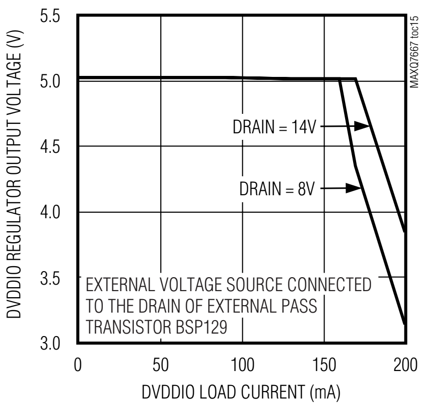
REGULATOR OUTPUT VOLTAGE vs. TEMPERATURE



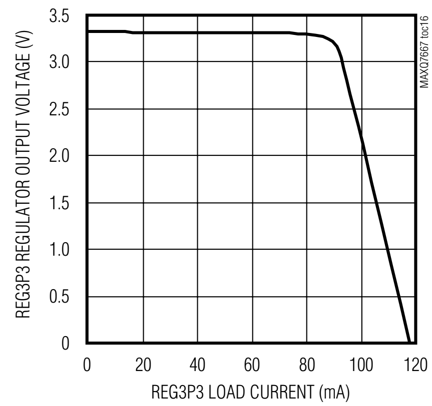
Typical Operating Characteristics (continued)

(V_{DVDDIO} = +5V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, f_{SYSCLK} = 16MHz, burst frequency = bandpass frequency = 50kHz, T_A = +25°C, unless otherwise noted.)

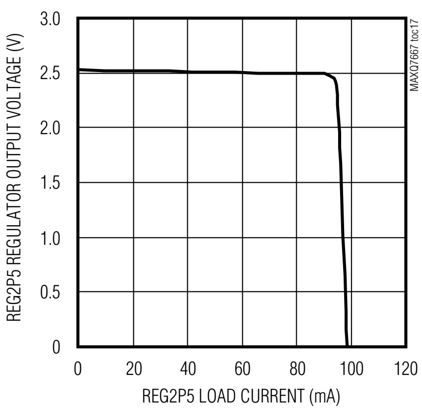
DVDDIO REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT



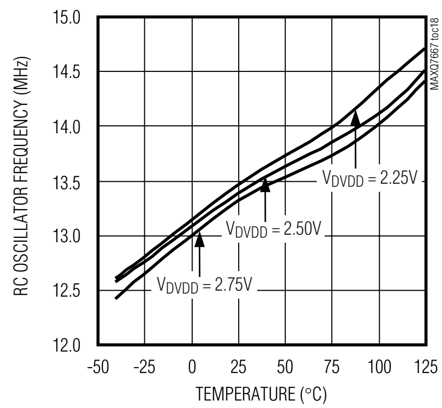
REG3P3 REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT



REG2P5 REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT



RC OSCILLATOR FREQUENCY vs. TEMPERATURE



16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

Pin Description

PIN	NAME	FUNCTION
1	P1.3/TCK	Port 1 Data 3/JTAG Serial Clock Input. P1.3 is a general-purpose digital I/O. TCK is the JTAG serial test clock input. Refer to the *MAXQ7667 User's Guide* Sections 5 and 11.
2	P1.4/MOSI	Port 1 Data 4/SPI Serial Data Output. P1.4 is a general-purpose digital I/O. MOSI is the master output, slave input for the SPI interface. Refer to the *MAXQ7667 User's Guide* Sections 5 and 9.
3	P1.5/MISO	Port 1 Data 5/SPI Serial Data Input. P1.5 is a general-purpose digital I/O. MISO is the master input, slave output for the SPI interface. Refer to the *MAXQ7667 User's Guide* Sections 5 and 9.
4	P1.6/SCLK	Port 1 Data 6/SPI Serial Clock Output. P1.6 is a general-purpose digital I/O. SCLK is the serial clock for the SPI interface. SCLK is an input when operating as a slave and an output when operating as a master. Refer to the *MAXQ7667 User's Guide* Sections 5 and 9.
5	P1.7/SYNC/SS	Port 1 Data 7/Schedule Timer Sync Input/SPI Slave Select. P1.7 is a general-purpose digital I/O. A rising edge on the SYNC input resets the schedule timer. In SPI slave mode, SS is the SPI slave-select input. In SPI master mode, use SS or a GPIO to manually select an external slave. Refer to the *MAXQ7667 User's Guide* Sections 5, 7, and 9.
6, 19, 42	DVDD	Digital Supply Voltage. Connect DVDD directly to a +2.5V external source or to REG2P5 output for single supply operation. Bypass DVDD to DGND with a 0.1µF capacitor as close as possible to the device. Connect all DVDD nodes together.
7, 18, 43	DGND	Digital Ground. Connect all DGND nodes together. Connect to AGND at a single point.
8, 17, 44	DVDDIO	Digital I/O Supply Voltage. DVDDIO powers all digital I/Os except for XIN and XOUT. Bypass DVDDIO to DGND with a 0.1µF capacitor as close as possible to the device. Connect all DVDDIO nodes together.
9	P0.0/URX	Port 0 Data 0/UART Receive Data Input. P0.0 is a general-purpose digital I/O. URX is a UART or LIN data receive input. Refer to the *MAXQ7667 User's Guide* Sections 5 and 8.
10	P0.1/UTX	Port 0 Data 1/UART Transmit Data Output. P0.1 is a general-purpose digital I/O. UTX is a UART or LIN data transmit output. Refer to the *MAXQ7667 User's Guide* Sections 5 and 8.
11	P0.2/$\overline{\text{TXEN}}$	Port 0 Data 2/UART Transmit Output. P0.2 is a general-purpose digital I/O. $\overline{\text{TXEN}}$ asserts low when the UART is transmitting. Use $\overline{\text{TXEN}}$ to enable an external LIN/UART transceiver. Refer to the *MAXQ7667 User's Guide* Sections 5 and 8.
12	P0.3/T0/ ADCCTL	Port 0 Data 3/Timer 0 I/O/ADC Control Input. P0.3 is a general-purpose digital I/O. T0 is the primary Type 2 timer/counter 0 output or input. ADCCTL is a sampling/conversion trigger input for the SAR ADC. Refer to the *MAXQ7667 User's Guide* Sections 5, 6, and 14.
13	P0.4/T0B	Port 0 Data 4/Timer 0B I/O/Comparator Output. P0.4 is a general-purpose digital I/O. T0B is the secondary Type 2 timer/counter 0 output or input. Refer to the *MAXQ7667 User's Guide* Sections 5 and 6.
14	P0.5/T1	Port 0 Data 5/Timer 1 I/O. P0.5 is a general-purpose digital I/O. T1 is the primary Type 2 timer/counter 1 output or input. Refer to the *MAXQ7667 User's Guide* Sections 5 and 6.
15	P0.6/T2	Port 0 Data 6/Timer 2 I/O. P0.6 is a general-purpose digital I/O. T2 is the primary Type 2 timer/counter 2 output or input. Refer to the *MAXQ7667 User's Guide* Sections 5 and 6.
16	P0.7/T2B	Port 0 Data 7/Timer 2B I/O. P0.7 is a general-purpose digital I/O. T2B is the secondary Type 2 timer/counter 2 output or input. Refer to the *MAXQ7667 User's Guide* Sections 5 and 6.
20	XIN	Crystal Oscillator Input. Connect an external crystal or resonator between XIN and XOUT. When using an external clock source drive XIN with 2.5V level clock while leaving XOUT unconnected. Connect XIN to DGND when an external clock source is not used.

Detailed Description

The ultrasonic distance-measurement peripherals in the MAXQ7667 include a burst signal generator for acoustic transmission and mixed signal circuits for amplifying and digitizing echo signals ranging between 25kHz and 100kHz. The burst signal is a square wave with adjustable duty cycle and pulse count. The burst is derived either directly from the system clock or from a programmable PLL locked to the system clock. The MAXQ7667 effectively digitizes the echo signals received at the ECHOP and ECHON inputs using an LNA, sigma-delta ADC with variable analog gain amplifier, noise-limiting digital bandpass filter, digital full-wave rectifier, and a digital lowpass filter (see the *Typical Application Circuit/Functional Diagram*). The device detects echo signals at the burst frequency with amplitudes ranging from 10µV_{P-P} to 100mV_{P-P}. Echoes greater than 100mV_{P-P} and less than 2V_{P-P} are internally clipped but do not saturate the receiver. To optimize echo reception, the clock used for processing the echo locks to the burst frequency. The MAXQ7667's burst generator can generate higher frequencies, but the maximum usable frequency for the echo receive path is 100kHz . For applications requiring transducer frequencies above 100kHz, implement an external echo receive path. The SAR ADC can then digitize the filtered echo envelope.

An integrated 16-bit RISC µC (MAXQ20) provides timing control, signal processing, and data I/O. The 16-bit Harvard architecture RISC core executes most instructions in a single clock cycle from instruction fetch to cycle completion. The MAXQ20 provides optimal performance for noise-sensitive analog applications.

The MAXQ7667 includes a 13.5MHz RC oscillator, external crystal oscillator, watchdog timer, schedule timer, three general-purpose Type 2 timers/counters, two 8-bit GPIO ports, SPI interface, JTAG interface, LIN capable UART interface, 12-bit SAR ADC with five multiplexed input channels, supply-voltage monitors, and a voltage reference for communication, diagnostics, and miscellaneous support.

Burst Controller

The MAXQ7667 provides a square-wave burst signal at the BURST output. Use the burst control to transmit an ultrasonic signal. Typical applications use the burst signal to switch an external transistor that drives a high-voltage transformer, which excites the transducer (see the *Typical Application Circuit/Functional Diagram*). Use software to configure the duty cycle, frequency, number of pulses, and drive current of the burst. See Section 17 of the *MAXQ7667 User's Guide*.

Derive the burst signal either directly from the system clock or from a programmable oscillator phase locked to the system clock (Figure 1). Using the system clock limits the burst frequency to one of 16 choices. Integer division of the system clock generates these 16 frequencies. The PLL allows a fractional division of the system clock. Any frequency within the PLL range is selectable to a resolution of 0.13% or better.

When using the internal PLL, connect external filter components (C1, R1, and C2) to FILT as shown in Figure 1. These components filter the analog voltage that controls the VCO in the PLL. The filter component values shown in the figure are suitable for the entire PLL frequency range.

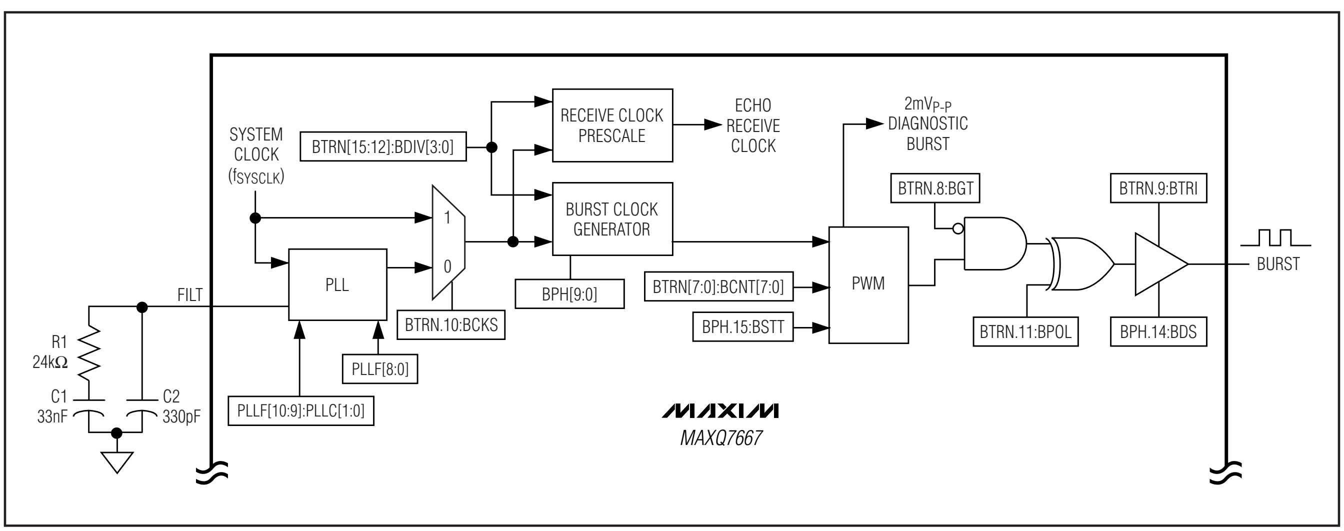


Figure 1. Burst Transmission Stage

Echo Receive Path

Low-Noise Amplifier (LNA)

The LNA provides a 40V/V fixed gain to the input signal. The differential inputs of the LNA are ECHOP and ECHON. For proper biasing of the LNA, AC-couple the transducer or any external circuitry to ECHOP and ECHON. For a single-ended input signal, AC-couple the signal to ECHOP with a 0.01µF capacitor and connect ECHON to AGND through a 0.01µF capacitor placed as close as possible to the signal source. The outputs of the LNA connect to the inputs of a 16-bit sigma-delta ADC and can connect internally to the AIN0 and AIN1 inputs of the SAR ADC for external monitoring (Figure 2).

Diagnostic Signals

An analog multiplexer located at the input of the LNA selects one of three possible signals for processing by the echo receive path; the normal echo signal AC-coupled to the ECHOP and ECHON inputs, 0V signal, or a $2mV_{P-P}$ internally generated signal (Figure 2). The $2mV_{P-P}$ square-wave signal, with frequency and duty cycle matching the burst signal, allows the echo receive chain to process a simulated echo.

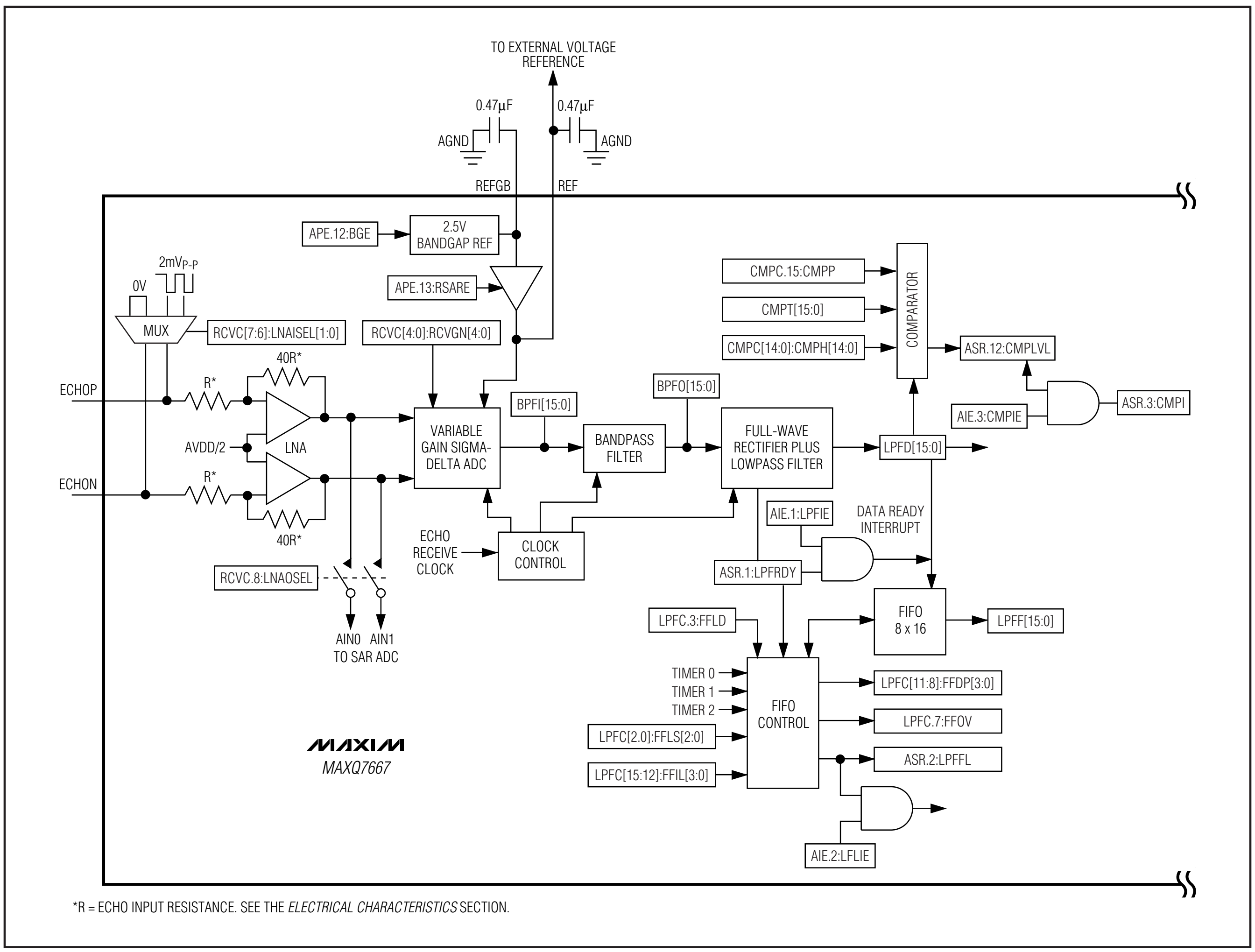


Figure 2. Echo Receive Path

16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

Sigma-Delta ADC

The MAXQ7667 features a 16-bit sigma-delta ADC with an analog gain adjustable from 38dB to 60dB (including the fixed LNA gain) with a maximum gain step of 12.5% (typical). Gain changes settle within one ADC conversion. Use software to create a virtual time variable gain amplifier. A digital bandpass and lowpass filters remove switching glitches and DC offset at the output of the ADC.

In a typical application, the software sets the gain to a low value when the burst is first sent and increases the gain as the time from when the burst was sent increases. As a result, strong echoes from nearby objects are processed without clipping while small signals from distant objects are processed with the maximum gain. The ADC samples the amplified echo signal from the LNA at 80 times the burst output frequency. The ADC provides conversion results at a data rate equal to 10 times the burst output frequency. The ADC conversion results also load to an 8-deep first-in-first-out (FIFO) at the native data rate or a separate time base without loading the CPU.

Digital Bandpass Filter

The digital bandpass filter has a center frequency that tracks the burst output frequency. The bandpass width is 14% of the center frequency. The bandpass filter provides the 16-bit output data at a data rate equal to 10 times the burst output frequency.

Full-Wave Rectifier

The full-wave rectifier detects the envelope of the digital bandwidth filter output to generate a DC output proportional to the peak-to-peak amplitude of the input signal. Full-wave rectification allows the digital lowpass filter to respond faster without excessive ripple.

Digital Lowpass Filter

The lowpass filter removes the ripple from the full-wave detector output. The output of the lowpass filter is available at a data rate equal to five times the burst output frequency. The corner frequency is 1/5 the burst frequency with approximately 40dB per decade rolloff. The 16-bit output data of the lowpass filter is stored in a FIFO register with a depth of eight samples. The MAXQ7667 allows data transfer from the lowpass filter

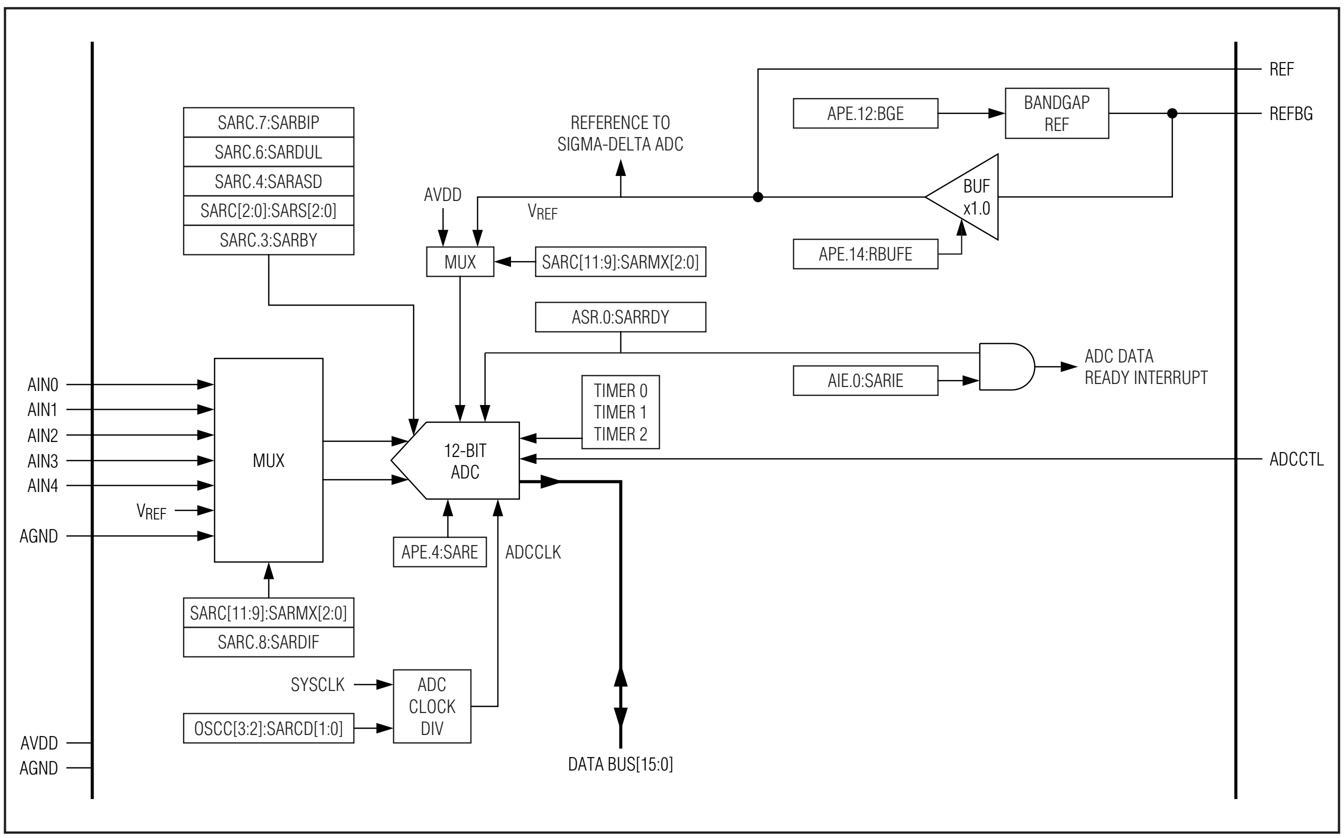


Figure 3. SAR ADC Block Diagram

output to the FIFO automatically each time the lowpass filter output updates, through the control of one of the timer outputs, or through software. The device includes a FIFO depth counter with programmable interrupt levels and generates an interrupt if a FIFO overflow condition occurs. The output of the digital lowpass filter connects to a digital comparator that can generate an interrupt for a specified echo signal level.

Digital Comparator and Threshold Adjust

The digital comparator output asserts when the echo amplitude at the output of the digital lowpass filter crosses a given threshold. The comparator's threshold level, hysteresis, and interrupt polarity are programmable.

SAR ADC

The MAXQ7667 incorporates a 12-bit unbuffered SAR ADC with sample-and-hold and conversion rate up to 250ksps. The ADC allows measurements of temperature, battery voltage, or other parameters using five single-ended or two fully differential analog inputs (AIN0–AIN4). All of the analog inputs have a range of 0 to V_{REF} in unipolar mode and $\pm V_{REF}/2$ in bipolar mode.

The SAR ADC supports three different conversion start sources: timers, ADC control input (ADCCTL), and software write. The conversion start source triggers the ADC acquisition and conversion. The system clock provides the ADC clock frequency programmable to 1/2, 1/4, 1/8, or 1/16 of the system clock. Use internal bandgap reference, external reference, or AVDD for voltage reference of the SAR ADC. Figure 3 shows a simplified block diagram of the SAR ADC.

The output of the SAR ADC is straight binary in unipolar mode and two's complement in bipolar mode. Figures 4 and 5 show the ADC transfer functions in unipolar mode and bipolar mode.

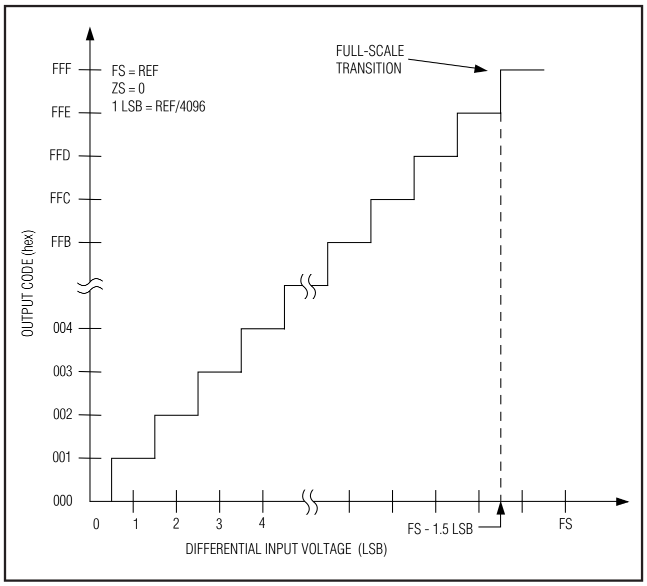


Figure 4. Unipolar Transfer Function

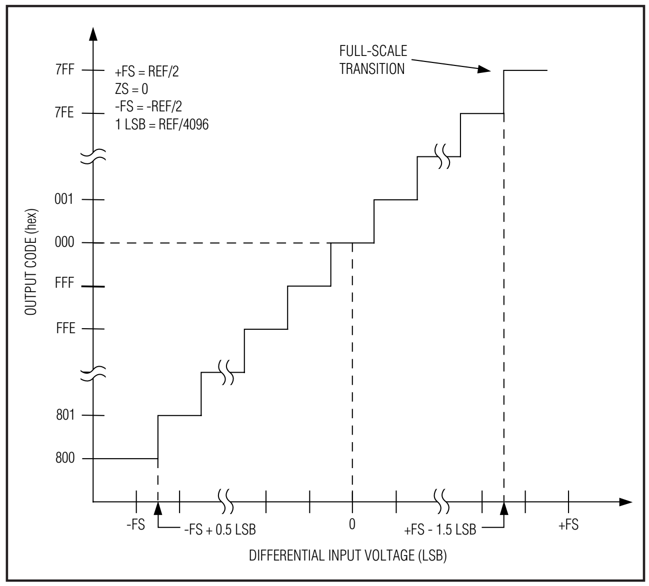


Figure 5. Bipolar Transfer Function

SAR ADC Analog Input Track-and-Hold (T/H)

Figures 6 and 7 show the equivalent input circuit of the MAXQ7667 analog input architecture. During acquisition (track), a sampling capacitor charges to the positive input voltage at AIN0–AIN4 in single-ended mode or AIN0 and AIN2 in differential mode while a second sampling capacitor connects to AGND in single-ended mode or AIN1 and AIN3 in differential mode. The ADC conversion start source and the ADC dual mode selection bits control the T/H timing.

Voltage Reference

The MAXQ7667 supports three possible voltage reference sources for ADC conversion; 2.5V internal buffered bandgap reference, external source, and AVDD. The internal 2.5V bandgap reference has high initial accuracy and temperature coefficient of typically less than 100ppm/°C. When operating in internal reference mode, either the buffered output of the internal reference or AVDD connects to the SAR ADC while the buffered output of the internal reference connects to the sigma-delta ADC. When operating in external reference mode, an external source ranging between 1V and V_{AVDD} applied at either the REF or REFBG inputs provides the reference to the SAR ADC and sigma-delta ADC. Bypass REFBG and REF to AGND with a 0.47µF capacitor for optimum performance. See Section 14 of the *MAXQ7667 User's Guide*.

Schedule Timer

The MAXQ7667's schedule timer provides general timekeeping and software synchronization to an external I/O. The schedule timer features include the following:

- 16-bit autoreload up-counter for the timer
- Programmable 16-bit alarm register
- Alarm interrupts
- Schedule timer incremented by a programmable system clock prescaler (1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128)
- Schedule timer up-counter resettable through an external I/O pin, which allows synchronization of a schedule timer to an external event
- Wake-up alarm to pull the system clock from stop-mode to normal operation

Figure 8 shows a simplified block diagram of the schedule timer.

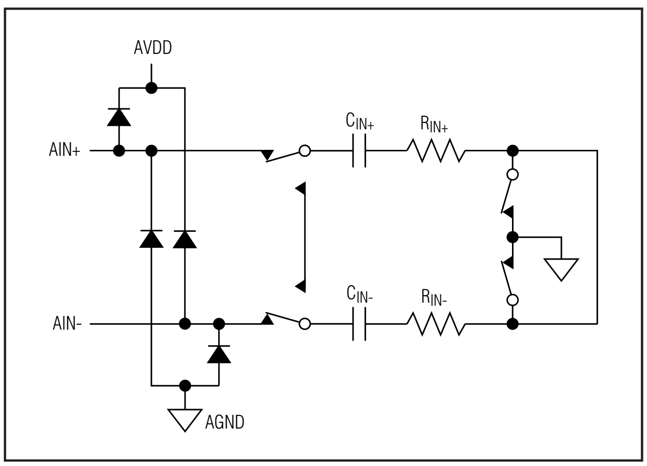


Figure 6. Equivalent Input Circuit (Track/Acquisition Mode)

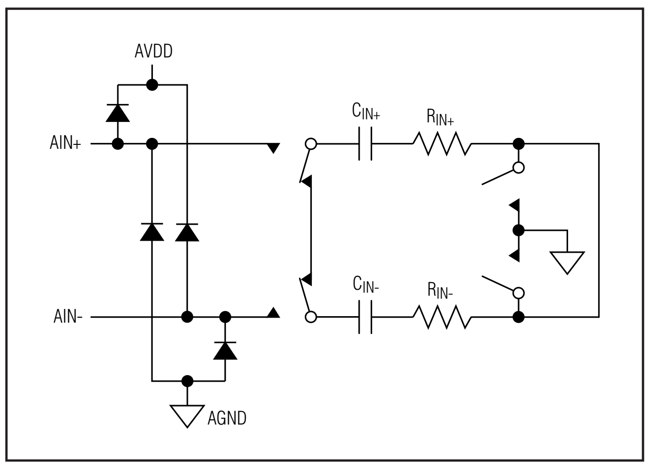


Figure 7. Equivalent Input Circuit (Hold/Conversion Mode)

Type 2 Timers/Counters

The MAXQ7667 includes three 16-bit timers/counters with programmable I/O (Figure 9). Each timer is a Type 2 timer implemented in the MAXQ® family. The Type 2 timer is an autoreload 16-bit timer/counter offering the following functions:

- 8-bit/16-bit timer/counter
- Up/down autoreload
- Counter function of external pulse
- Capture
- Compare

Clock Sources

The MAXQ7667 oscillator module supplies the system clock for the µC core and all of the peripheral modules. The high-frequency oscillator operates with a 1MHz to 16MHz crystal. Use the internal RC oscillator as the system clock for applications that do not require precise timing. See Section 15 of the *MAXQ7667 User's Guide*.

The MAXQ7667 supports the following master clock sources:

- Internal high-frequency oscillator drives an external 1MHz–16MHz crystal or ceramic resonator
- Internal, fast-starting, 13.5MHz RC oscillator (default oscillator at startup and in the event the external crystal fails)
- External 4MHz–16MHz clock input

Crystal Selection

The MAXQ7667 requires a crystal with the following specifications:

Frequency: 1MHz–16MHz

C_{LOAD}: 6pF (min)

Drive level: 5µW

Series resonance resistance: 30Ω (max)

Note: Quartz crystal vendors often specify series resonance resistance (R1). Series resonance resistance is the resistance observed when the resonator is in the series resonant condition. When a resonator is used in the parallel resonant mode with an external load capacitance, as is the case with the MAXQ7667 oscillator circuit, the effective resistance at the loaded frequency of oscillation is:

$$R1 \times (1 + (CO/C_{LOAD}))^2$$

For typical shunt capacitance (CO) and load capacitance (C_{LOAD}) values, the effective resistance potentially exceeds R1 by a factor of 2.

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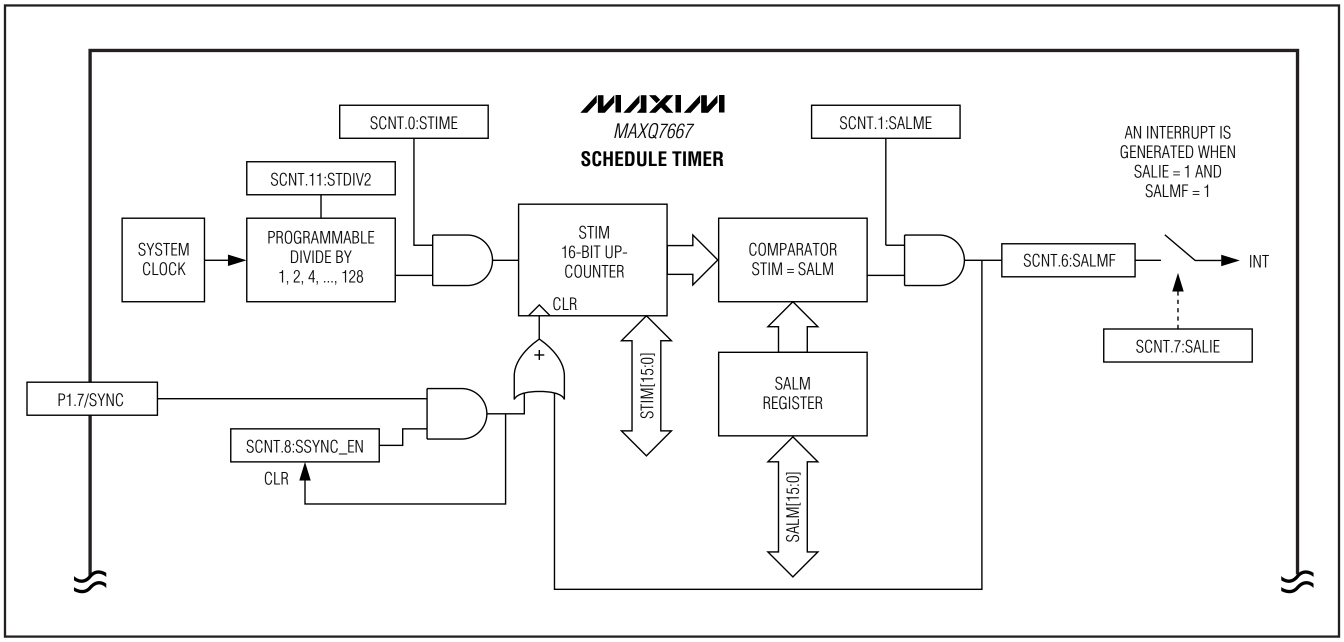

Figure 8. Schedule-Timer Module Block Diagram

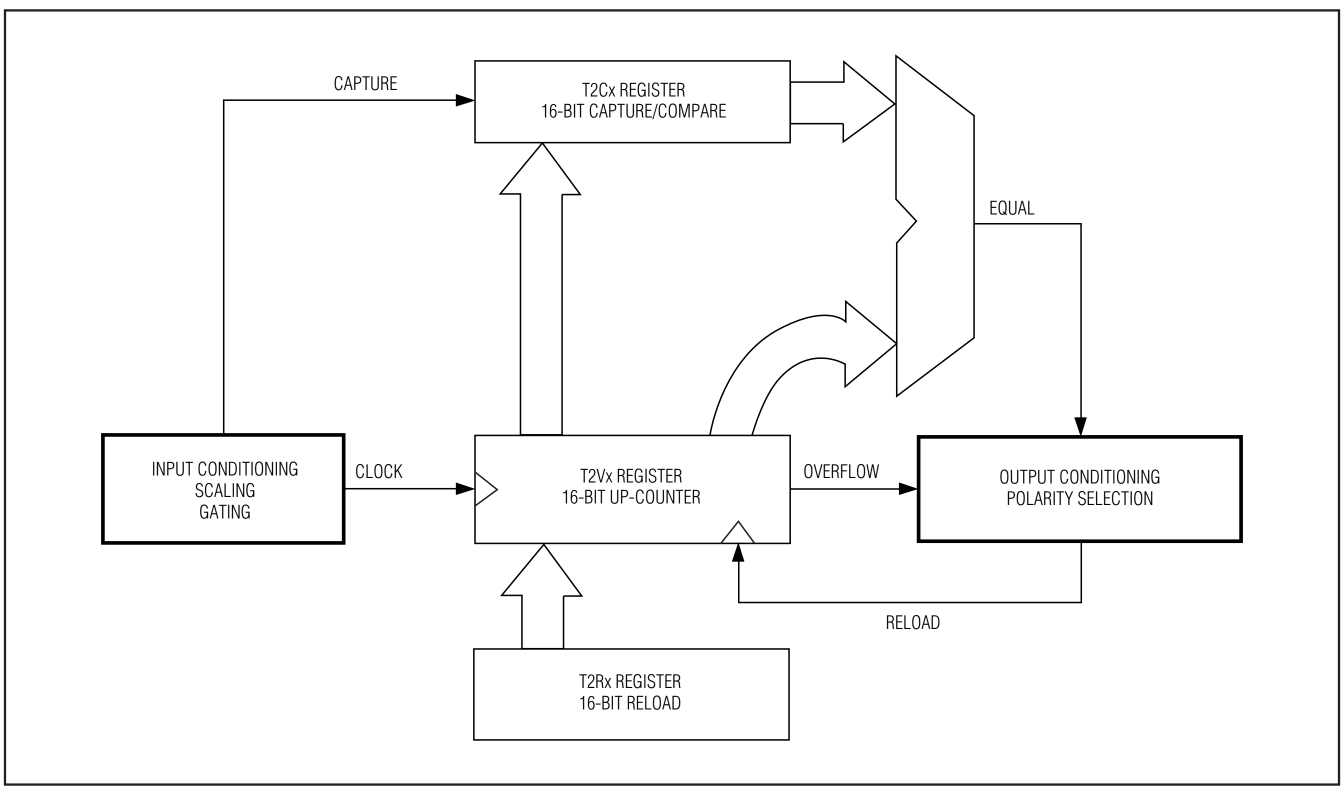

Figure 9. Type 2 Timer/Counter in 16-Bit Mode

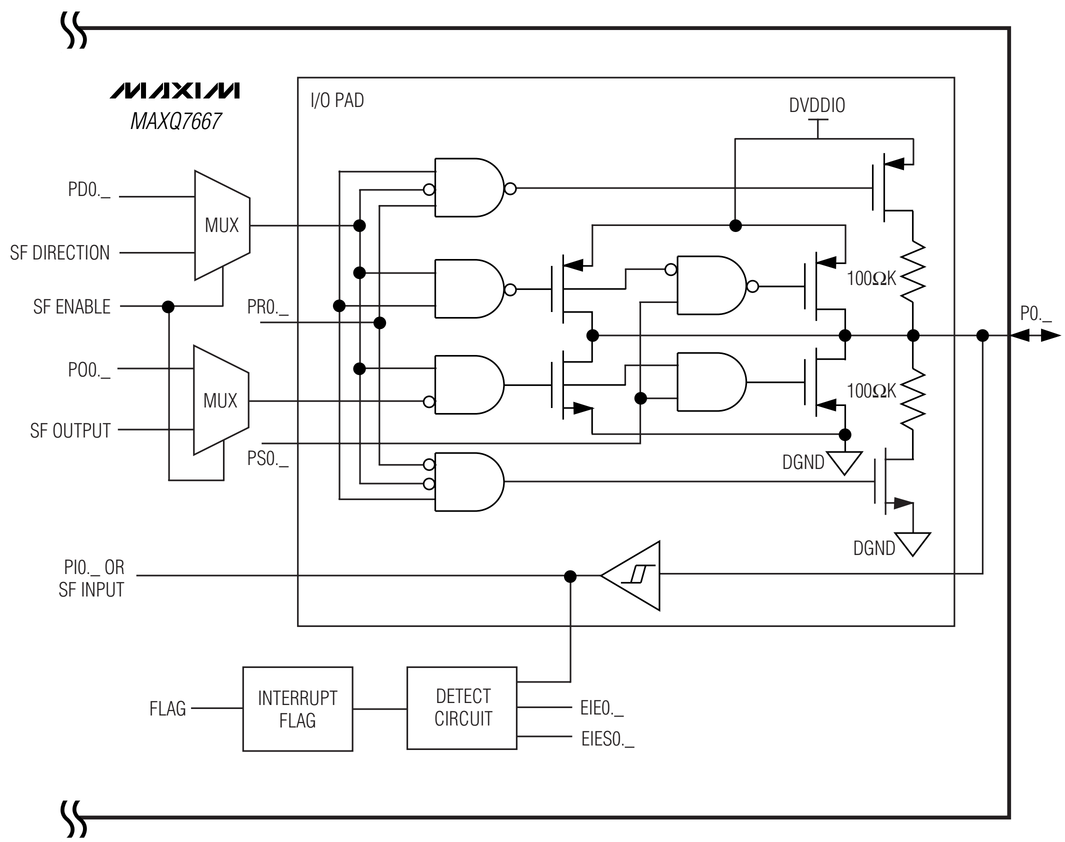

Figure 13. Port 0 Digital I/O Basic Circuitry. Port 1 Circuitry is the Same as Port 2.

Connect bypass capacitors at each power-supply input as close as possible to the device. Use a bypass capacitor less than 0.47µF on DVDDIO. For most applications, 0.1µF bypass capacitors are adequate.

Supply Brownout Monitor

Power supplies DVDD, AVDD, and DVDDIO each include a brownout monitor/supervisor that alerts the µC when their corresponding supply voltages drop below the interrupt threshold. Activate each brownout monitor independently using the corresponding brownout enable bits: VDBE, VIBE, and VABE.

Reset

In reset mode, no instruction execution occurs and all inputs/outputs return to their default states. Code execution resumes at address 8000h (in the utility ROM) once the reset condition is removed.

Four different sources reset the MAXQ7667: POR, watchdog timer reset, external reset, and internal system reset.

During normal operation, force $\overline{\text{RESET}}$ low for at least four system clock cycles for an external reset. Set the ROD bit in the SC register, while the SPE bit in the ICDF register is set, for an internal system reset. See Section 16 of the *MAXQ7667 User's Guide*.

Power-On Reset (POR)

The MAXQ7667 includes a DVDD voltage supervisor to control the µC POR. On power-up, internal circuitry pulls $\overline{\text{RESET}}$ low and resets all the internal registers. $\overline{\text{RESET}}$ is held low for the duration of the power-on delay after V_{DVDD} rises above the DVDD reset threshold. The internal RC oscillator starts up and software execution begins at the reset vector location 8000h immediately after the device exits POR while $\overline{\text{RESET}}$ is

Table 3. Peripheral Register Map

REGISTER INDEX	MODULE NAME (BASE SPECIFIER)					
	M0 (0h)	M1 (1h)	M2 (2h)	M3 (3h)	M4 (4h)	M5 (5h)
0h	PO0	MCNT	T2CNA0	T2CNA2	—	BPH
1h	PO1	MA	T2H0	T2H2	—	BTRN
2h	—	MB	T2RH0	T2RH2	—	SARC
3h	EIF0	MC2	T2CH0	T2CH2	—	RCVC
4h	EIF1	MC1	T2CNA1	—	—	PLLF
5h	—	MC0	T2H1	CNT1	—	AIE
6h	—	SPIB	T2RH1	SCON	—	CMPC
7h	—	SPICN	T2CH1	SBUF	—	CMPT
8h	PI0	SPICF	T2CNB0	T2CNB2	—	ASR
9h	PI1	SPICK	T2V0	T2V2	—	SARD
Ah	—	—	T2R0	T2R2	—	LPFC
Bh	EIE0	—	T2C0	T2C2	—	OSCC
Ch	EIE1	MC1R	T2CNB1	FSTAT	—	BPFI
Dh	—	MC0R	T2V1	ERRR	—	BPFO
Eh	—	SCNT	T2R1	CHKSUM	—	LPFD
Fh	—	STIM	T2C1	ISVEC	—	LPFF
10h	PD0	SALM	T2CFG0	T2CFG2	—	APE
11h	PD1	FPCTL	T2CFG1	STA0	—	—
12h	—	—	—	SMD	—	FGAIN
13h	EIES0	—	—	FCON	—	B1COEF
14h	EIES1	—	—	CNT0	—	B2COEF
15h	—	—	—	CNT2	—	B3COEF
16h	—	—	—	IDFB	—	A2A
17h	—	RCTRM	—	SADDR	—	A2B
18h	PS0	—	ICDT0	SADEN	—	—
19h	PS1	—	ICDT1	BT	—	A2D
1Ah	—	—	ICDC	TMR	—	—
1Bh	PR0	—	ICDF	—	—	A3A
1Ch	PR1	ID0	ICDB	—	—	A3B
1Dh	—	ID1	ICDA	—	—	—
1Eh	—	—	ICDD	—	—	A3D
1Fh	—	—	—	—	—	—

Table 4. Peripheral Register Bit Functions and Reset Values (continued)

REGISTER	REGISTER BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCNT	—	—	—	—	STDIV2	STDIV1	STDIV0	SSYNC_EN	SALIE	SALMF	—	—	—	—	SALME	STIME
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
STIM	STIM15	STIM14	STIM13	STIM12	STIM11	STIM10	STIM9	STIM8	STIM7	STIM6	STIM5	STIM4	STIM3	STIM2	STIM1	STIM0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SALM	SALM15	SALM14	SALM13	SALM12	SALM11	SALM10	SALM9	SALM8	SALM7	SALM6	SALM5	SALM4	SALM3	SALM2	SALM1	SALM0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FPCNTL	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DPMG
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RCTRM	—	—	—	—	—	—	—	RCTRM8	RCTRM7	RCTRM6	RCTRM5	RCTRM4	RCTRM3	RCTRM2	RCTRM1	RCTRM0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID0	ID015	ID014	ID013	ID012	ID011	ID010	ID09	ID08	ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ID1	ID115	ID114	ID113	ID112	ID111	ID110	ID19	ID18	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNA0	—	—	—	—	—	—	—	—	ET2	T2OE0	T2POL0	TR2L	TR2	CPRL2	SS2	G2EN
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2H0	—	—	—	—	—	—	—	—	T2H07	T2H06	T2H05	T2H04	T2H03	T2H02	T2H01	T2H00
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2RH0	—	—	—	—	—	—	—	—	T2RH07	T2RH06	T2RH05	T2RH04	T2RH03	T2RH02	T2RH01	T2RH00
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CH0	—	—	—	—	—	—	—	—	T2CH07	T2CH06	T2CH05	T2CH04	T2CH03	T2CH02	T2CH01	T2CH00
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNA1	—	—	—	—	—	—	—	—	ET2	T2OE0	T2POL0	TR2L	TR2	CPRL2	SS2	G2EN
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2H1	—	—	—	—	—	—	—	—	T2H17	T2H16	T2H15	T2H14	T2H13	T2H12	T2H.1	T2H10
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2RH1	—	—	—	—	—	—	—	—	T2RH17	T2RH16	T2RH15	T2RH14	T2RH13	T2RH12	T2RH11	T2RH10
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CH1	—	—	—	—	—	—	—	—	T2CH17	T2CH16	T2CH15	T2CH14	T2CH13	T2CH12	T2CH11	T2CH10
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNB0	—	—	—	—	—	—	—	—	ET2L	T2OE1	T2POL1	—	TF2	TF2L	TCC2	TC2L
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2V0	T2V015	T2V014	T2V013	T2V012	T2V011	T2V010	T2V09	T2V08	T2V07	T2V06	T2V05	T2V04	T2V03	T2V02	T2V01	T2V00
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2R0	T2R015	T2R014	T2R013	T2R012	T2R011	T2R010	T2R09	T2R08	T2R07	T2R06	T2R05	T2R04	T2R03	T2R02	T2R01	T2R00
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2C0	T2C015	T2C014	T2C013	T2C012	T2C011	T2C010	T2C09	T2C08	T2C07	T2C06	T2C05	T2C04	T2C03	T2C02	T2C01	T2C00
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNB1	—	—	—	—	—	—	—	—	ET2L	T2OE1	T2POL1	—	TF2	TF2L	TCC2	TC2L
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2V1	T2V115	T2V114	T2V113	T2V112	T2V111	T2V110	T2V19	T2V18	T2V17	T2V16	T2V15	T2V14	T2V13	T2V12	T2V11	T2V10
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2R1	T2R115	T2R114	T2R113	T2R112	T2R111	T2R110	T2R19	T2R18	T2R17	T2R16	T2R15	T2R14	T2R13	T2R12	T2R11	T2R10
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2C1	T2C115	T2C114	T2C113	T2C112	T2C111	T2C110	T2C19	T2C18	T2C17	T2C16	T2C15	T2C14	T2C13	T2C12	T2C11	T2C10
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CFG0	—	—	—	—	—	—	—	—	T2C1	T2DIV2	T2DIV1	T2DIV0	T2MD	CCF1	CCF0	C/T2
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CFG1	—	—	—	—	—	—	—	—	T2C1	T2DIV2	T2DIV1	T2DIV0	T2MD	CCF1	CCF0	C/T2
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDT0	ICDT015	ICDT014	ICDT013	ICDT012	ICDT011	ICDT010	ICDT09	ICDT08	ICDT07	ICDT06	ICDT05	ICDT04	ICDT03	ICDT02	ICDT01	ICDT00
	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB
ICDT1	ICDT115	ICDT114	ICDT113	ICDT112	ICDT111	ICDT110	ICDT19	ICDT18	ICDT17	ICDT16	ICDT15	ICDT14	ICDT13	ICDT12	ICDT11	ICDT10
	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB
ICDC	—	—	—	—	—	—	—	—	DME	—	REGE	—	CMD3	CMD2	CMD1	CMD0
	0	0	0	0	0	0	0	0	DW	0	DW	0	DW	DW	DW	DW

Table 4. Peripheral Register Bit Functions and Reset Values (continued)

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICDF	—	—	—	—	—	—	—	—	—	—	—	—	PSS1	PSS0	SPE	TXC
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDB	—	—	—	—	—	—	—	—	ICDB.7	ICDB.6	ICDB.5	ICDB.4	ICDB.3	ICDB.2	ICDB.1	ICDB.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDA	ICDA15	ICDA14	ICDA13	ICDA12	ICDA11	ICDA10	ICDA9	ICDA8	ICDA7	ICDA6	ICDA5	ICDA4	ICDA3	ICDA2	ICDA1	ICDA0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDD	ICDD15	ICDD14	ICDD13	ICDD12	ICDD11	ICDD10	ICDD9	ICDD8	ICDD7	ICDD6	ICDD5	ICDD4	ICDD3	ICDD2	ICDD1	ICDD0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNA2	—	—	—	—	—	—	—	—	ET2	T2OE0	T2POL0	TR2L	TR2	CPRL2	SS2	G2EN
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2H2	—	—	—	—	—	—	—	—	T2H27	T2H26	T2H25	T2H24	T2H23	T2H22	T2H21	T2H20
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2RH2	—	—	—	—	—	—	—	—	T2RH27	T2RH26	T2RH25	T2RH24	T2RH23	T2RH22	T2RH21	T2RH20
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CH2	—	—	—	—	—	—	—	—	T2CH27	T2CH26	T2CH25	T2CH24	T2CH23	T2CH22	T2CH21	T2CH20
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CNT1	—	—	—	—	—	—	—	—	RTN	CK	FL5	FL4	FL3	FL2	FL1	FL0
	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
SCON	—	—	—	—	—	—	—	—	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SBUF	—	—	—	—	—	—	—	—	SBUF7	SBUF6	SBUF5	SBUF4	SBUF3	SBUF2	SBUF1	SBUF0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNB2	—	—	—	—	—	—	—	—	ET2L	T2OE1	T2POL1	—	TF2	TF2L	TCC2	TC2L
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2V2	T2V215	T2V214	T2V213	T2V212	T2V211	T2V210	T2V29	T2V28	T2V27	T2V26	T2V25	T2V24	T2V23	T2V22	T2V21	T2V20
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2R2	T2R215	T2R214	T2R213	T2R212	T2R211	T2R210	T2R29	T2R28	T2R27	T2R26	T2R25	T2R24	T2R23	T2R22	T2R21	T2R20
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2C2	T2C215	T2C214	T2C213	T2C212	T2C211	T2C210	T2C29	T2C28	T2C27	T2C26	T2C25	T2C24	T2C23	T2C22	T2C21	T2C20
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FSTAT	—	—	—	—	—	—	—	—	—	—	TFF	TFAE	TFE	RFF	RFAF	RFE
	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
ERRR	—	—	—	—	—	—	—	—	—	OTE	DME	CKE	P1	PIE	P0	POE
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CHKSUM	CHKSUM15	CHKSUM14	CHKSUM13	CHKSUM12	CHKSUM11	CHKSUM10	CHKSUM9	CHKSUM8	CHKSUM7	CHKSUM6	CHKSUM5	CHKSUM4	CHKSUM3	CHKSUM2	CHKSUM1	CHKSUM0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ISVEC	—	—	—	—	—	—	—	—	—	—	—	—	ISVEC3	ISVEC2	ISVEC1	ISVEC0
	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
T2CFG2	—	—	—	—	—	—	—	—	T2C1	T2DIV2	T2DIV1	T2DIV0	T2MD	CCF1	CCF0	C/T2
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
STA0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INP	BUSY
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SMD	—	—	—	—	—	—	—	—	EIR	OFS	—	—	—	IE	SMOD	FEDE
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FCON	—	—	—	—	—	—	—	—	FTF	FRF	TXFT1	TXFT0	RXFT1	RXFT0	OE	FEN
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CNT0	—	—	—	—	—	—	—	—	WU	FP1	FP0	INE	AUT	INIT	LUN1	LUN0
	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0
CNT2	—	—	—	—	—	—	—	—	—	—	—	DMIS	PM	HDO	FBS	BTH
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IDFB	—	—	IDFBH5	IDFBH4	IDFBH3	IDFBH2	IDFBH1	IDFBH0	—	—	IDFBL5	IDFBL4	IDFBL3	IDFBL2	IDFBL1	IDFBL0
	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
SADDR	—	—	—	—	—	—	—	—	SADDR7	SADDR6	SADDR5	SADDR4	SADDR3	SADDR2	SADDR1	SADDR0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SADEN	—	—	—	—	—	—	—	—	SADEN7	SADEN6	SADEN5	SADEN4	SADEN3	SADEN2	SADEN1	SADEN0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/09	Initial release	—
1	7/09	Updated *Ordering Information* to indicate automotive qualified part	1