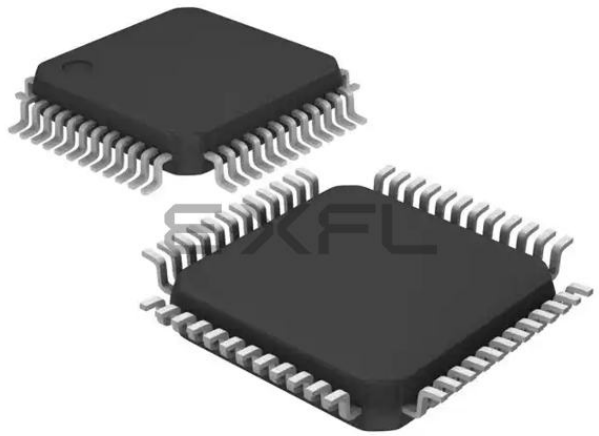
Analog Devices Inc./Maxim Integrated - MAXQ7667AACM/V+ Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	-
Core Size	16-Bit
Speed	16MHz
Connectivity	LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	16
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 2.75V
Data Converters	A/D 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq7667aacm-v

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5V, V_{AVDD} = +3.3V; V_{DVDD} = +2.5V, system clock (f_{SYSCLK}) = 16MHz, burst frequency (f_{BURST}) = bandpass frequency (f_{BPF}) = 50kHz, C_{REFBG} = C_{REF} = 1µF in parallel with 0.01µF, f_{ADCCLK} = 2MHz (SAR data rate = 125ksps), T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BANDPASS FILTER						
Center Frequency	f_{BPF}		25		100	kHz
Passband Width		-3dB		0.14 x f_{BPF}		kHz
Minimum Stopband Rejection		One decade away from center frequency		-60		dB
Output Data Rate				10 x f_{BPF}		ksps
Output Data Resolution				16		Bits
LOWPASS FILTER						
Corner Frequency	f_{LPF}	-3dB		0.1 x f_{BPF}		kHz
Rolloff				40		dB/Decade
Output Data Rate				5 x f_{BPF}		ksps
Output Data Resolution				16		Bits
SAR ADC						
Resolution		Measurement	12			Bits
		No missing codes	11			
Integral Nonlinearity		Tested at 125ksps		±1	±2	LSB
Differential Nonlinearity		Tested at 125ksps	-2		+2	LSB
Offset Error				±1	±3	mV
Offset-Error Drift				±5		µV/°C
Gain Error					±1	%
Gain-Error Temperature Coefficient				±0.4		ppmFS/°C
Input-Referred Noise		At ADC inputs		400		$µV_{RMS}$
Differential Input Range		Unipolar	0		V_{REF}	V
		Bipolar	$-V_{REF}/2$		$+V_{REF}/2$	
Absolute Input Range			0		V_{AVDD}	V
Input Leakage Current				±0.1		µA
Conversion Time		13 ADCCLK cycles at 2MHz			6.5	µs
Input Capacitance				14		pF
Track-and-Hold Acquisition Time		Three ADCCLK cycles at 2MHz			1.5	µs
Turn-On Time		Eight ADCCLK cycles at 2MHz			4	µs
Conversion Clock	f_{ADCCLK}		0.5		4	MHz
Conversion Rate		f_{ADCCLK} = 4MHz (not production tested)			250	ksps

16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5V, V_{AVDD} = +3.3V; V_{DVDD} = +2.5V, system clock (f_{SYSCLK}) = 16MHz, burst frequency (f_{BURST}) = bandpass frequency (f_{BPF}) = 50kHz, C_{REFBG} = C_{REF} = 1µF in parallel with 0.01µF, f_{ADCCLK} = 2MHz (SAR data rate = 125ksps), T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE BUFFER						
Offset				5		mV
Minimum Load			2.5			kΩ
Output Bypass Capacitor				0.47		µF
EXTERNAL VOLTAGE REFERENCE (Reference Buffer Disabled)						
Reference Input Range		Applied at REF	1.0		V_{AVDD}	V
Reference Input Impedance		Measured at REF with the SAR and sigma-delta ADCs running at maximum frequency		50		kΩ
INTERNAL VOLTAGE REFERENCE (REFBG)						
Initial Accuracy			2.45	2.5	2.55	V
Maximum Temperature Coefficient				100		ppm/°C
Output Impedance				1.1		kΩ
Power-Supply Rejection Ratio		V_{AVDD} = 3.0V to 3.6V		60		dB
Output Noise				0.5		mV_{RMS}
PROGRAMMABLE BURST-FREQUENCY OSCILLATOR						
Burst-Frequency Range			0.025		1.335	MHz
Burst-Frequency Resolution				0.1		%
Burst-Frequency Locking Time		Change from 40kHz to 60kHz		5		ms
		Change from 50kHz to 50.5kHz		2		
CRYSTAL OSCILLATOR						
Frequency Range		Tested crystal frequency		16		MHz
		Minimum crystal frequency		4		
		External clock input	4		16	
Temperature Stability		Excluding crystal		25		ppm/°C
Startup Time		16MHz crystal		10		ms
XIN Input Low Voltage		When driven with external clock source			0.3 x V_{DVDD}	V
XIN Input High Voltage		When driven with external clock source	0.7 x V_{DVDD}			V
INTERNAL RC OSCILLATOR						
Frequency				13.5		MHz
Initial Accuracy				10.5		%
Temperature Drift		T_A = T_{MIN} to T_{MAX}		700		ppm
Supply Rejection		V_{DVDD} = 2.25V to 2.75V		-1.5		%

16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5V, V_{AVDD} = +3.3V; V_{DVDD} = +2.5V, system clock (f_{SYSCLK}) = 16MHz, burst frequency (f_{BURST}) = bandpass frequency (f_{BPF}) = 50kHz, C_{REFBG} = C_{REF} = 1µF in parallel with 0.01µF, f_{ADCCLK} = 2MHz (SAR data rate = 125ksps), T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
+2.5V LINEAR REGULATOR (REG2P5)							
REG2P5 Output Voltage				2.38		2.62	V
Load Current						50	mA
Output Short-Circuit Current		REG2P5 shorted to DGND			100		mA
POWER REQUIREMENTS							
Supply Voltage Range		DVDD		2.25	2.5	2.75	V
		AVDD		3.00	3.3	3.6	
		DVDDIO		4.5	5.0	5.5	
AVDD Supply Current		All analog functions enabled			12	18	mA
		All analog functions disabled			3	10	µA
		Incremental AVDD supply current	LNA		2.4		mA
			Sigma-delta ADC		12		
			SAR ADC, 250ksps, f_{ADCCLK} = 4MHz		600		µA
			PLL		300		
			Supply voltage supervisors		3		
			Internal voltage reference		220		
			Reference buffer		300		
			Bias (any AVDD module enabled)		1.5		mA
DVDD Supply Current					11		mA
DVDDIO Supply Current					2.5		mA
DIGITAL INPUTS (GPIO, UART, JTAG, SPI™)							
Input High Voltage				V_{DVDDIO} - 1			V
Input Low Voltage						0.8	V
Input Hysteresis		V_{DVDDIO} = 5.0V			500		mV
Input Leakage Current		Digital input voltage = DGND or DVDDIO, pullup disabled			±0.01	±1	µA
Pullup/Pulldown Resistance		Pulled up to DVDDIO internally, pulled down to DGND internally			150		kΩ
Input Capacitance					15		pF

SPI is a trademark of Motorola, Inc.

16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDDIO} = +5V, V_{AVDD} = +3.3V; V_{DVDD} = +2.5V, system clock (f_{SYSCLK}) = 16MHz, burst frequency (f_{BURST}) = bandpass frequency (f_{BPF}) = 50kHz, C_{REFBG} = C_{REF} = 1µF in parallel with 0.01µF, f_{ADCCLK} = 2MHz (SAR data rate = 125ksps), T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI INTERFACE TIMING (Figures 11 and 12)						
SPI Master Operating Frequency	$1/t_{MCK}$	0.5 x f_{SYSCLK}			8	MHz
SPI Slave Operating Frequency	$1/t_{SCK}$	0.25 x f_{SYSCLK}			4	MHz
SCLK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$ - 25			ns
MOSI Output Hold Time After SCLK Sample Edge	t_{MOH}		$t_{MCK}/2$ - 25			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$ - 25			ns
MISO Input Valid to SCLK Sample Edge	t_{MIS}		25			ns
MISO Input Hold Time After SCLK Sample Edge	t_{MIH}		0			ns
SCLK Inactive to MOSI Inactive	t_{MLH}		0			ns
SCLK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		ns
SS Active to First Shift Edge	t_{SSE}		$4t_{SYSCLK}$			ns
MOSI Input Setup Time to SCLK Sample Edge	t_{SIS}		25			ns
MOSI Input Hold Time After SCLK Sample Edge	t_{SIH}		25			ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}				50	ns
SS Inactive Duration	t_{SSH}		t_{SYSCLK} + 25			ns
SCLK Inactive to SS Rising Edge	t_{SD}		t_{SYSCLK} + 25			ns
FLASH PROGRAMMING						
Flash Erase Time		Mass erase	200			ms
		Page erase (512 bytes per page)	20			
Flash Programming Time		20µs per word	657			ms
Write/Erase Cycles			10,000			Cycles
Data Retention		Average temperature = +85°C	15			Years

Note 1: Noise measured at bandpass filter output with ECHO+ and ECHO- shorted divided by the gain with f_{BPF} = 50kHz.

Note 2: Gain adjust resolution typically ranges between 6.25% and 12.5%.

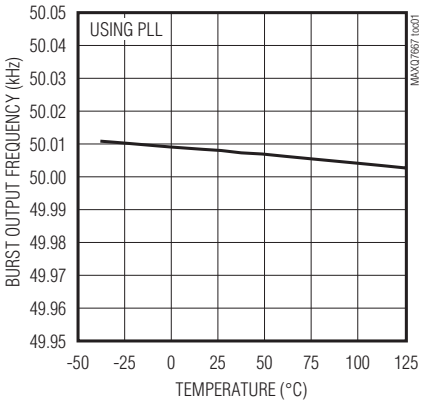
Note 3: LIN 2.0 specifies a maximim data rate of 20kbps. Higher data rates could be possible with compatible devices and suitable line conditions.

16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

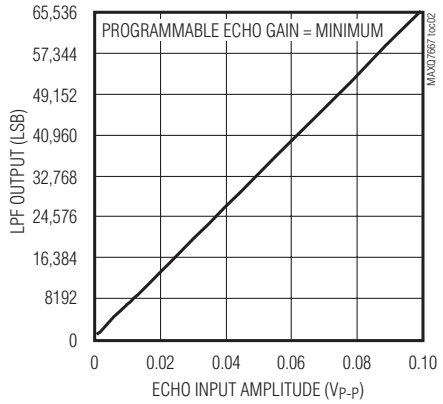
Typical Operating Characteristics

(V_{DVDDIO} = +5V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, f_{SYSCLK} = 16MHz, burst frequency = bandpass frequency = 50kHz, T_A = +25°C, unless otherwise noted.)

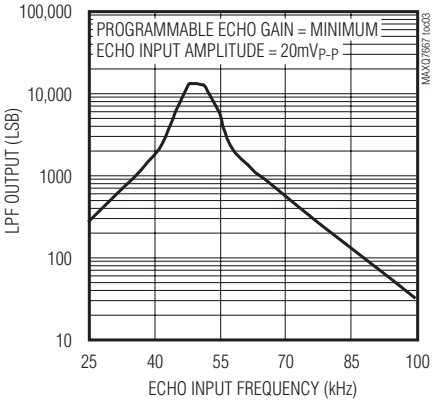
BURST OUTPUT FREQUENCY vs. TEMPERATURE



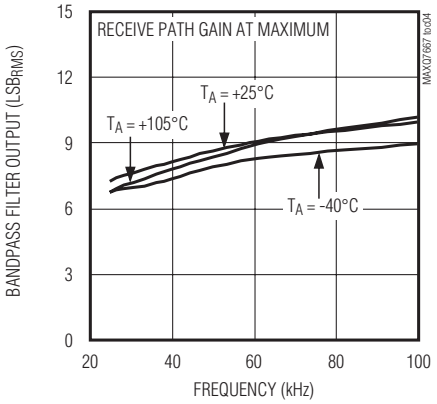
LOWPASS FILTER OUTPUT vs. ECHO INPUT AMPLITUDE



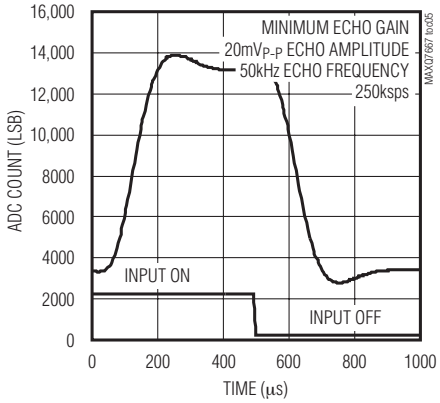
LOWPASS FILTER OUTPUT vs. ECHO INPUT FREQUENCY



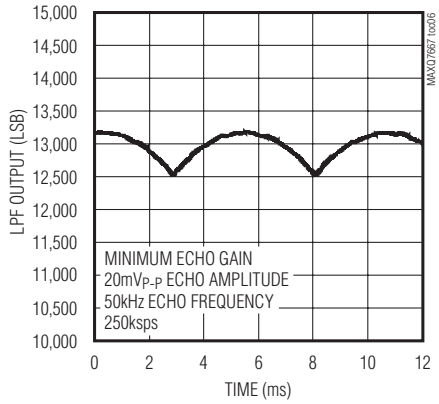
BANDPASS FILTER OUTPUT NOISE FLOOR vs. BANDPASS FILTER CENTER FREQUENCY



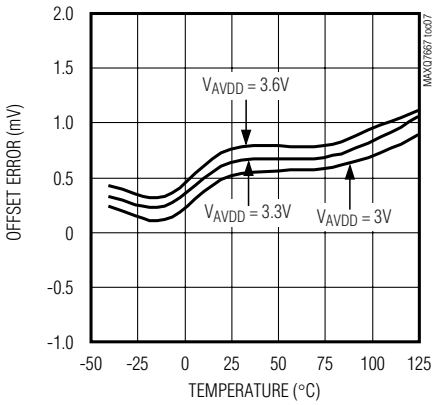
RECEIVE PATH RESPONSE TIME (ECHO INPUT TO LOWPASS FILTER OUTPUT)



LOWPASS FILTER OUTPUT RIPPLE vs. TIME



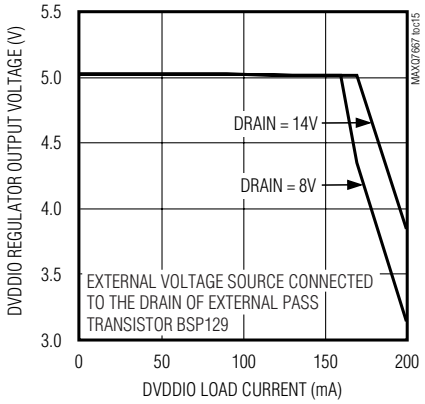
SAR ADC OFFSET ERROR vs. TEMPERATURE



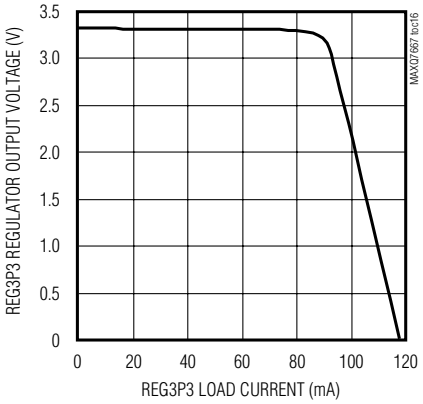
Typical Operating Characteristics (continued)

(V_{DVDDIO} = +5V, V_{AVDD} = +3.3V, V_{DVDD} = +2.5V, f_{SYSCLK} = 16MHz, burst frequency = bandpass frequency = 50kHz, T_A = +25°C, unless otherwise noted.)

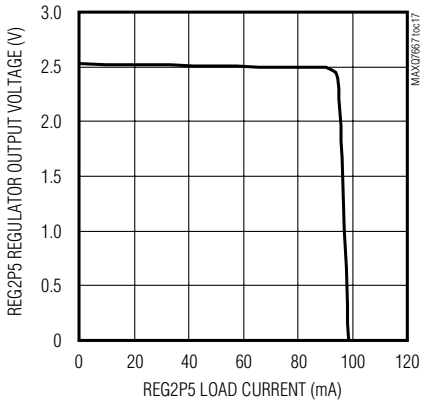
DVDDIO REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT



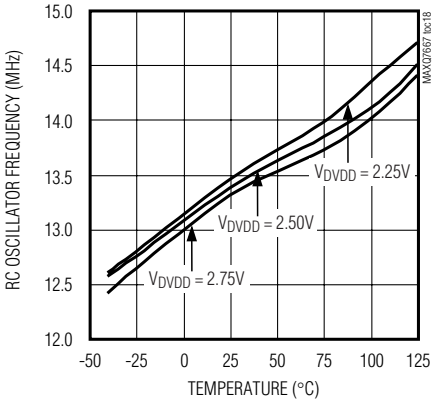
REG3P3 REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT



REG2P5 REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT



RC OSCILLATOR FREQUENCY vs. TEMPERATURE



16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

Detailed Description

The ultrasonic distance-measurement peripherals in the MAXQ7667 include a burst signal generator for acoustic transmission and mixed signal circuits for amplifying and digitizing echo signals ranging between 25kHz and 100kHz. The burst signal is a square wave with adjustable duty cycle and pulse count. The burst is derived either directly from the system clock or from a programmable PLL locked to the system clock. The MAXQ7667 effectively digitizes the echo signals received at the ECHOP and ECHON inputs using an LNA, sigma-delta ADC with variable analog gain amplifier, noise-limiting digital bandpass filter, digital full-wave rectifier, and a digital lowpass filter (see the *Typical Application Circuit/Functional Diagram*). The device detects echo signals at the burst frequency with amplitudes ranging from 10µV$_{P-P}$ to 100mV$_{P-P}$. Echoes greater than 100mV$_{P-P}$ and less than 2V$_{P-P}$ are internally clipped but do not saturate the receiver. To optimize echo reception, the clock used for processing the echo locks to the burst frequency. The MAXQ7667's burst generator can generate higher frequencies, but the maximum usable frequency for the echo receive path is 100kHz . For applications requiring transducer frequencies above 100kHz, implement an external echo receive path. The SAR ADC can then digitize the filtered echo envelope.

An integrated 16-bit RISC µC (MAXQ20) provides timing control, signal processing, and data I/O. The 16-bit Harvard architecture RISC core executes most instructions in a single clock cycle from instruction fetch to cycle completion. The MAXQ20 provides optimal performance for noise-sensitive analog applications.

The MAXQ7667 includes a 13.5MHz RC oscillator, external crystal oscillator, watchdog timer, schedule timer, three general-purpose Type 2 timers/counters, two 8-bit GPIO ports, SPI interface, JTAG interface, LIN capable UART interface, 12-bit SAR ADC with five multiplexed input channels, supply-voltage monitors, and a voltage reference for communication, diagnostics, and miscellaneous support.

Burst Controller

The MAXQ7667 provides a square-wave burst signal at the BURST output. Use the burst control to transmit an ultrasonic signal. Typical applications use the burst signal to switch an external transistor that drives a high-voltage transformer, which excites the transducer (see the *Typical Application Circuit/Functional Diagram*). Use software to configure the duty cycle, frequency, number of pulses, and drive current of the burst. See Section 17 of the *MAXQ7667 User's Guide*.

Derive the burst signal either directly from the system clock or from a programmable oscillator phase locked to the system clock (Figure 1). Using the system clock limits the burst frequency to one of 16 choices. Integer division of the system clock generates these 16 frequencies. The PLL allows a fractional division of the system clock. Any frequency within the PLL range is selectable to a resolution of 0.13% or better.

When using the internal PLL, connect external filter components (C1, R1, and C2) to FILT as shown in Figure 1. These components filter the analog voltage that controls the VCO in the PLL. The filter component values shown in the figure are suitable for the entire PLL frequency range.

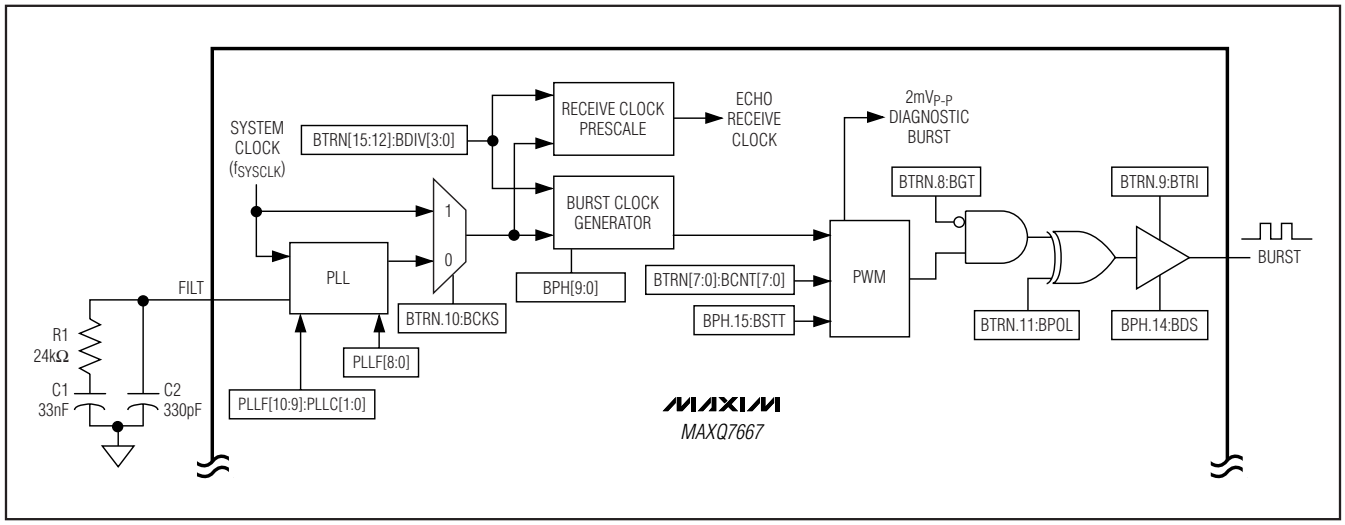


Figure 1. Burst Transmission Stage

16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

SAR ADC Analog Input Track-and-Hold (T/H)

Figures 6 and 7 show the equivalent input circuit of the MAXQ7667 analog input architecture. During acquisition (track), a sampling capacitor charges to the positive input voltage at AIN0–AIN4 in single-ended mode or AIN0 and AIN2 in differential mode while a second sampling capacitor connects to AGND in single-ended mode or AIN1 and AIN3 in differential mode. The ADC conversion start source and the ADC dual mode selection bits control the T/H timing.

Voltage Reference

The MAXQ7667 supports three possible voltage reference sources for ADC conversion; 2.5V internal buffered bandgap reference, external source, and AVDD. The internal 2.5V bandgap reference has high initial accuracy and temperature coefficient of typically less than 100ppm/°C. When operating in internal reference mode, either the buffered output of the internal reference or AVDD connects to the SAR ADC while the buffered output of the internal reference connects to the sigma-delta ADC. When operating in external reference mode, an external source ranging between 1V and V_{AVDD} applied at either the REF or REFBG inputs provides the reference to the SAR ADC and sigma-delta ADC. Bypass REFBG and REF to AGND with a 0.47µF capacitor for optimum performance. See Section 14 of the *MAXQ7667 User's Guide*.

Schedule Timer

The MAXQ7667's schedule timer provides general timekeeping and software synchronization to an external I/O. The schedule timer features include the following:

- 16-bit autoreload up-counter for the timer
- Programmable 16-bit alarm register
- Alarm interrupts
- Schedule timer incremented by a programmable system clock prescaler (1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128)
- Schedule timer up-counter resettable through an external I/O pin, which allows synchronization of a schedule timer to an external event
- Wake-up alarm to pull the system clock from stop-mode to normal operation

Figure 8 shows a simplified block diagram of the schedule timer.

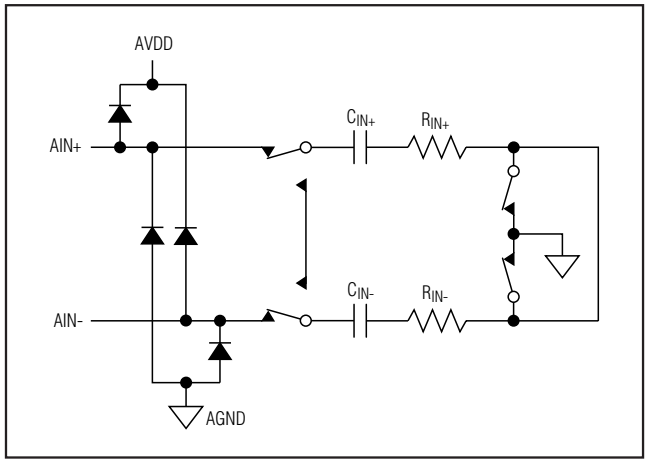


Figure 6. Equivalent Input Circuit (Track/Acquisition Mode)

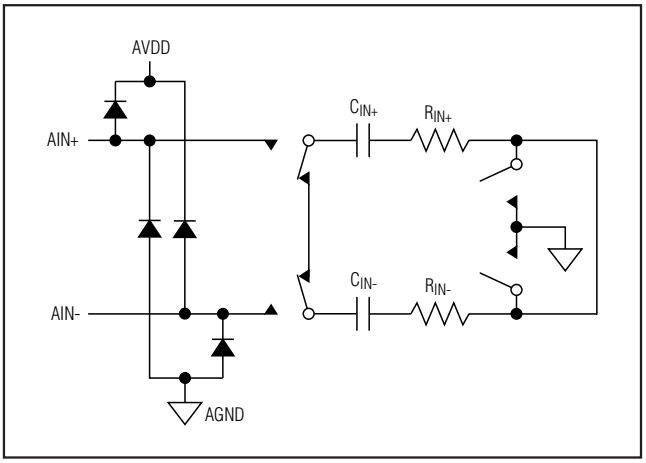


Figure 7. Equivalent Input Circuit (Hold/Conversion Mode)

16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

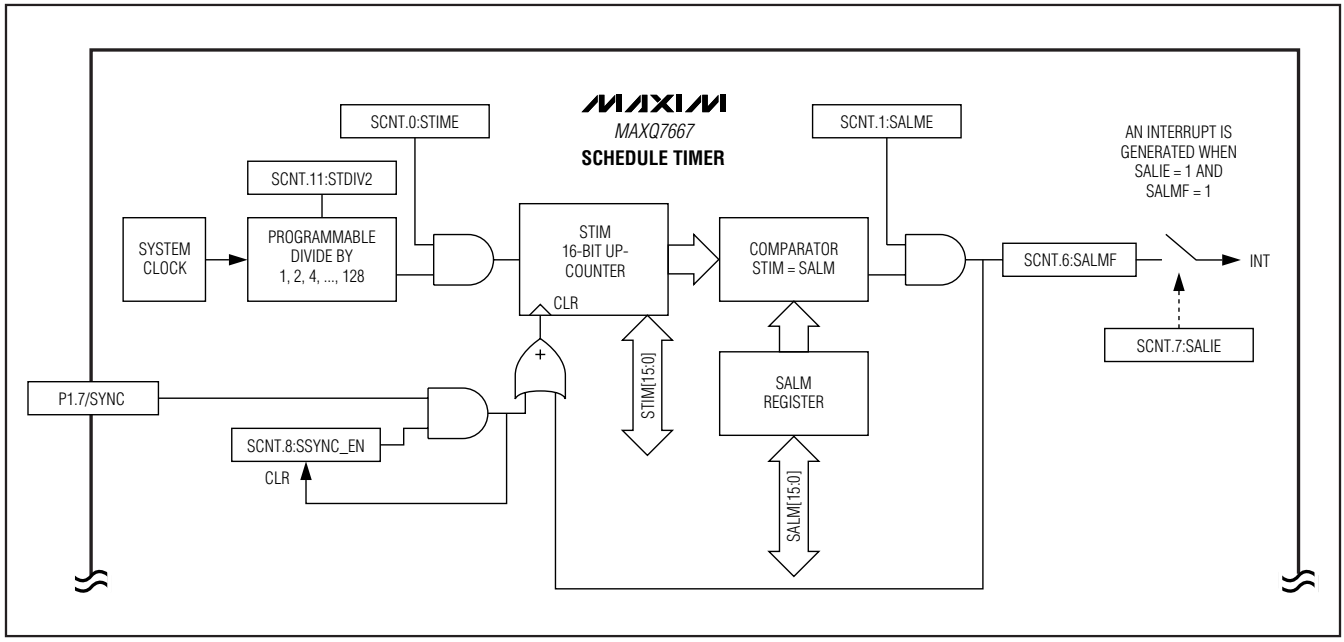


Figure 8. Schedule-Timer Module Block Diagram

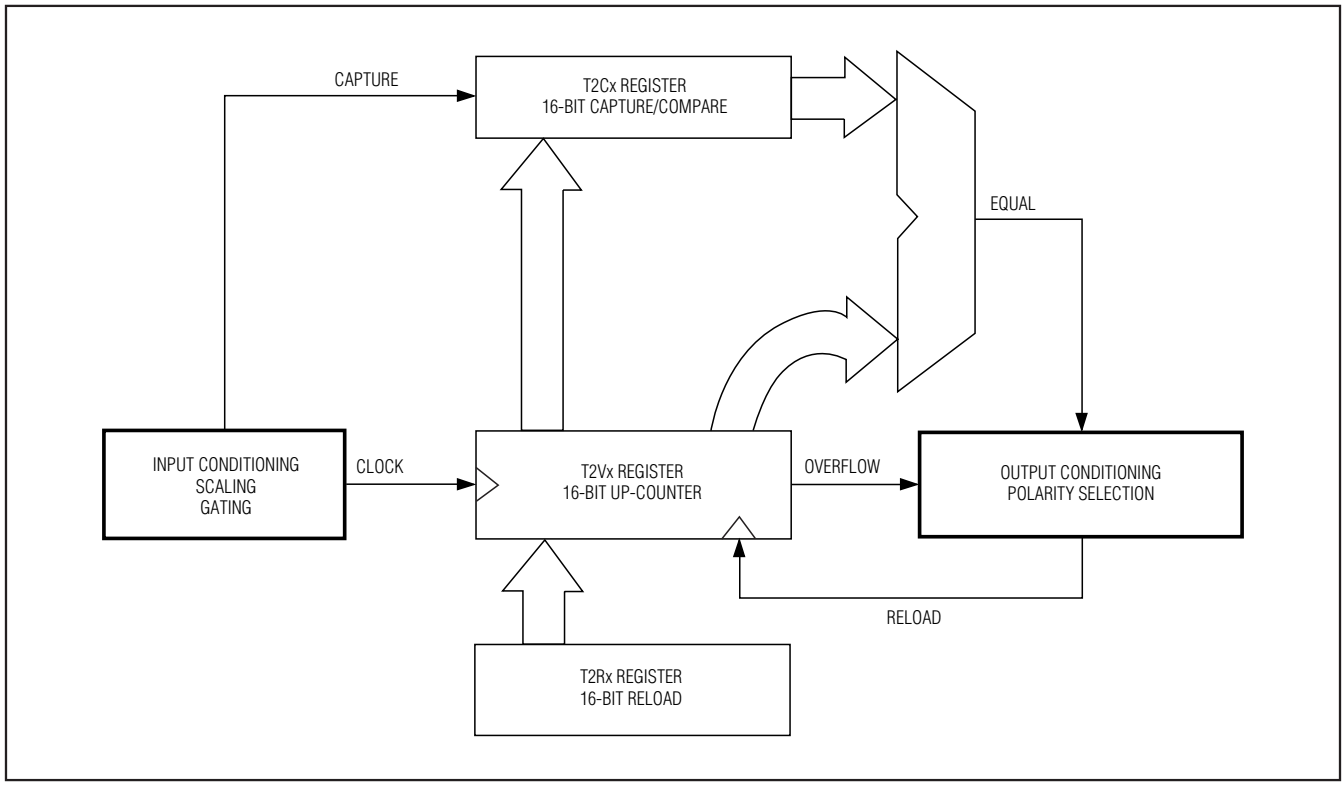


Figure 9. Type 2 Timer/Counter in 16-Bit Mode

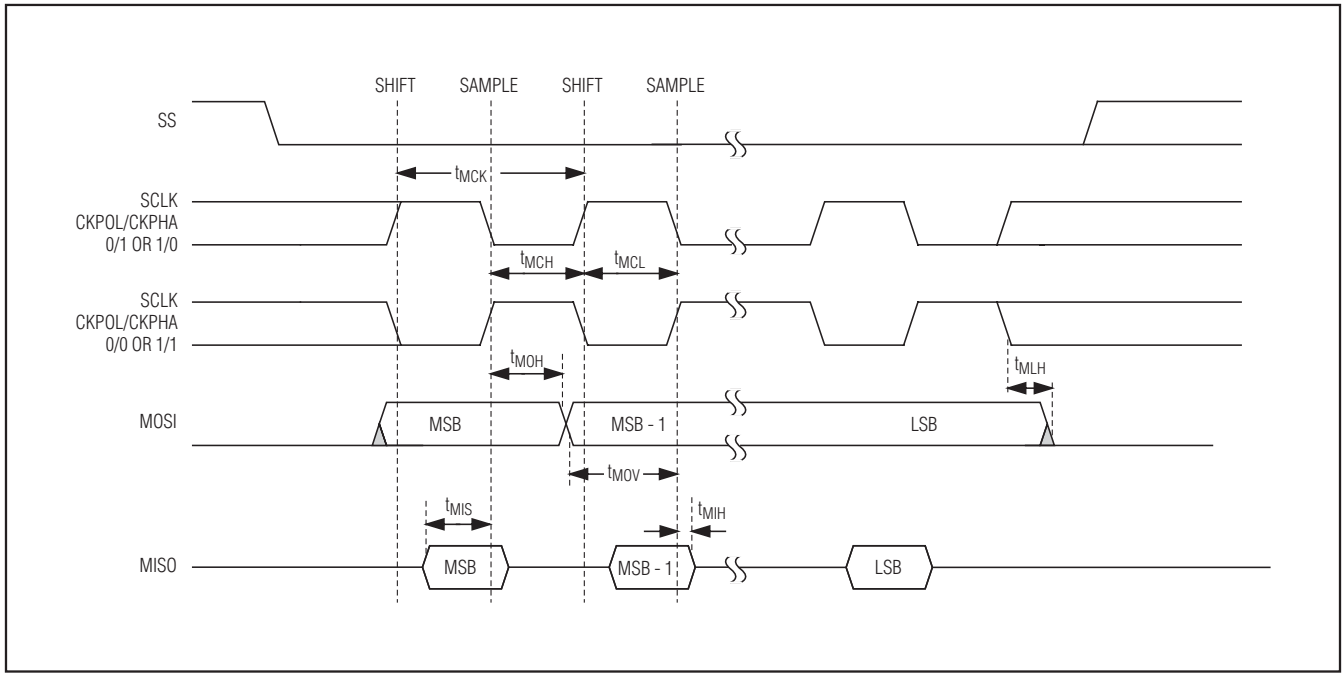


Figure 11. SPI Timing Diagram in Master Mode

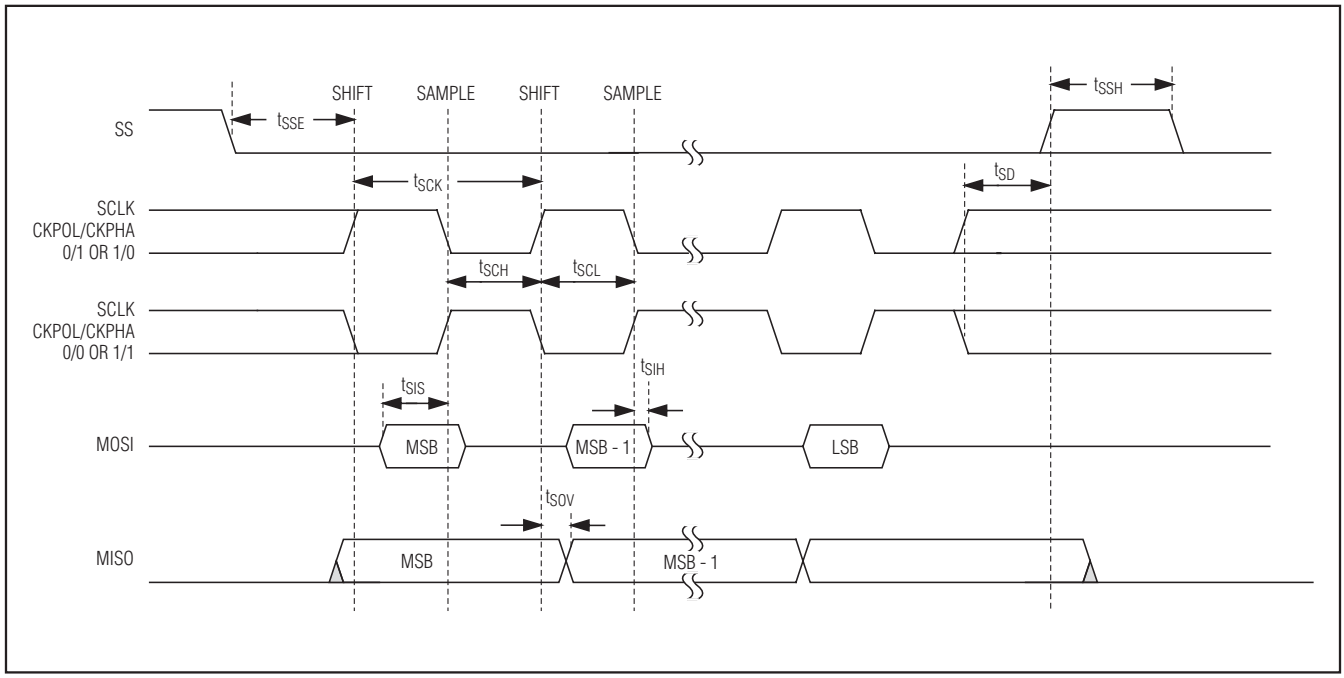


Figure 12. SPI Timing Diagram in Slave Mode

16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

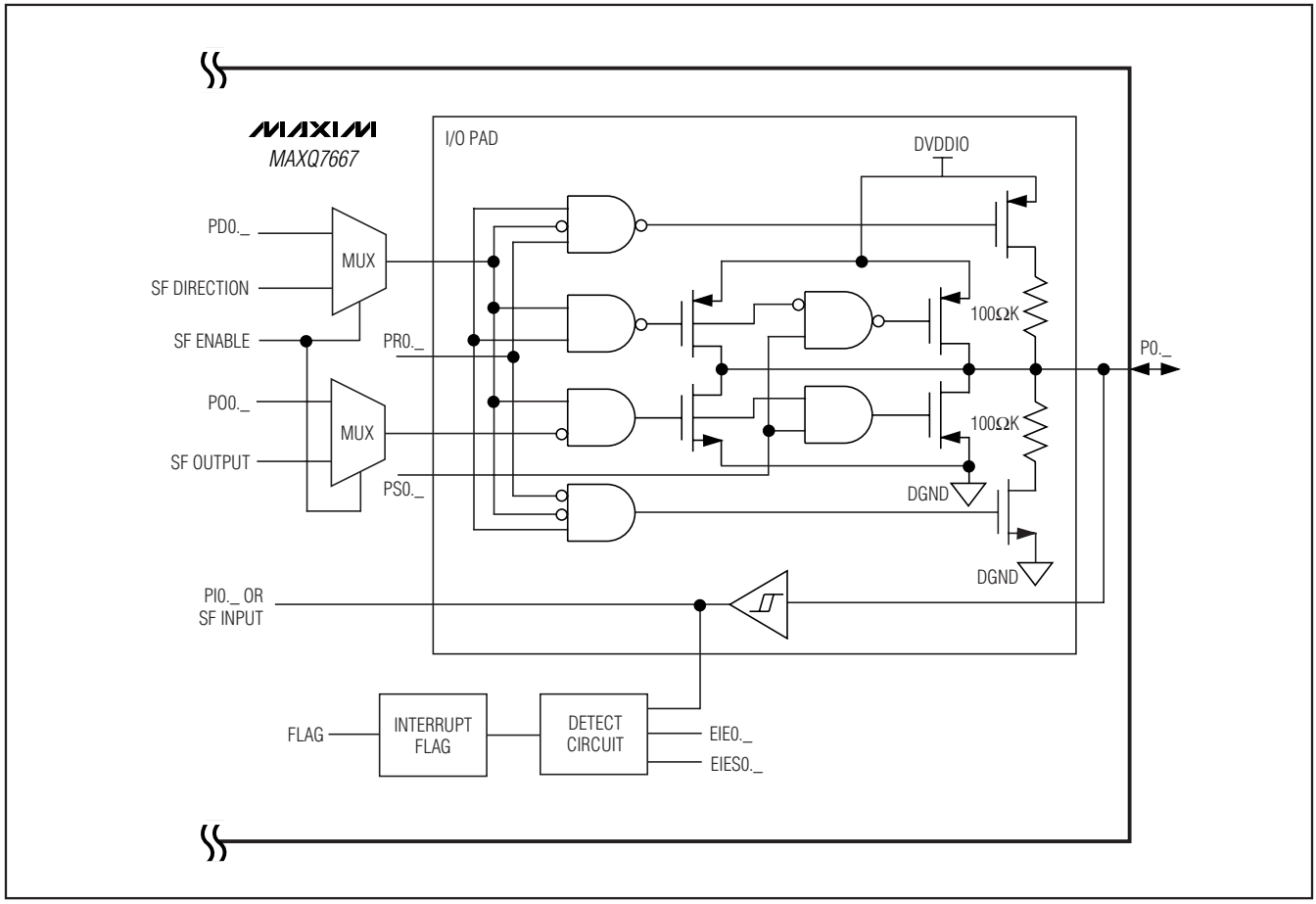


Figure 13. Port 0 Digital I/O Basic Circuitry. Port 1 Circuitry is the Same as Port 2.

Connect bypass capacitors at each power-supply input as close as possible to the device. Use a bypass capacitor less than 0.47µF on DVDDIO. For most applications, 0.1µF bypass capacitors are adequate.

Supply Brownout Monitor

Power supplies DVDD, AVDD, and DVDDIO each include a brownout monitor/supervisor that alerts the µC when their corresponding supply voltages drop below the interrupt threshold. Activate each brownout monitor independently using the corresponding brownout enable bits: VDBE, VIBE, and VABE.

Reset

In reset mode, no instruction execution occurs and all inputs/outputs return to their default states. Code execution resumes at address 8000h (in the utility ROM) once the reset condition is removed.

Four different sources reset the MAXQ7667: POR, watchdog timer reset, external reset, and internal system reset.

During normal operation, force $\overline{\text{RESET}}$ low for at least four system clock cycles for an external reset. Set the ROD bit in the SC register, while the SPE bit in the ICDF register is set, for an internal system reset. See Section 16 of the *MAXQ7667 User's Guide*.

Power-On Reset (POR)

The MAXQ7667 includes a DVDD voltage supervisor to control the µC POR. On power-up, internal circuitry pulls $\overline{\text{RESET}}$ low and resets all the internal registers. $\overline{\text{RESET}}$ is held low for the duration of the power-on delay after V_{DVDD} rises above the DVDD reset threshold. The internal RC oscillator starts up and software execution begins at the reset vector location 8000h immediately after the device exits POR while $\overline{\text{RESET}}$ is

not externally forced low. An internal POR flag indicates the source of a reset. Ramp up the DVDD supply at a minimum rate of 60mV/ms to keep the device in POR until DVDD fully settles.

Watchdog Timer

The primary function of the watchdog timer is to watch for stalled or stuck software. The watchdog timer performs a controlled system restart when the µP fails to write to the watchdog timer register before a selectable timeout interval expires. The internal 13.5MHz RC oscillator drives the MAXQ7667's watchdog timer.

Figure 14 shows the watchdog timer functions as the source of both the watchdog interrupt and watchdog reset. The watchdog interrupt timeout period is programmable to 2^{12}, 2^{15}, 2^{18}, or 2^{21} cycles of the RC oscillator resulting in a nominal range of 273µs to 139.8ms. The watchdog reset timeout period is a fixed 512 RC clock cycles (34µs). When enabled, the watchdog generates an interrupt upon expiration; then, if not reset within 512 RC clock cycles, the watchdog asserts $\overline{\text{RESET}}$ low for eight RC clock cycles.

Hardware Multiplier/Accumulator

A hardware multiplier supports high-speed multiplications. The multiplier completes a 16-bit x 16-bit multiplication in a single clock cycle and contains a 48-bit accumulator. The multiplier is a peripheral that performs seven different multiplication operations:

- Unsigned 16-bit multiplication
- Unsigned 16-bit multiplication and accumulation
- Unsigned 16-bit multiplication and subtraction

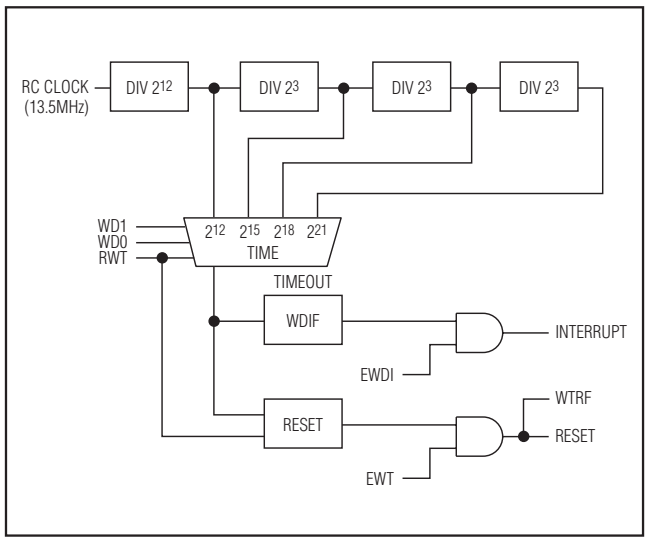


Figure 14. Watchdog Functional Diagram

- Signed 16-bit multiplication
- Signed 16-bit multiplication and negation
- Signed 16-bit multiplication and accumulation
- Signed 16-bit multiplication and subtraction

MAXQ Core Architecture

The MAXQ20 µC is an accumulator-based Harvard memory architecture. Fetch and execution operations complete in one clock cycle without pipelining because the instruction contains both the op code and data. The µC streamlines 16 million instructions per second (MIPS). Integrated 16-level hardware stack enables fast subroutine calling and task switching. Manipulate data quickly and efficiently with three internal data pointers. Multiple data pointers allow more than one function to access data memory without having to save and restore data pointers each time. The data pointers automatically increment or decrement following an operation, eliminating the need for software intervention.

Instruction Set

The instruction set consists of a total of 33 fixed-length 16-bit instructions that operate on registers and memory locations. The highly orthogonal instruction set allows arithmetic and logical operations to use any register along with the accumulator. System registers control functionality common to all MAXQ µCs, while peripheral registers control peripherals and functions specific to the MAXQ7667. All registers are subdivided into register modules.

The architecture is transport-triggered. Writes or reads from certain register locations potentially have side effects. These side effects form the basis for the higher level op codes defined by the assembler, such as ADDC, OR, JUMP, etc. The op codes are implemented as MOVE instructions between system registers. The assembler handles all the instruction encoding.

Memory Organization

In addition to the internal register space, the device incorporates several memory areas:

- 16Kwords of flash memory for program storage
- 2Kword of SRAM for storage of temporary variables
- 4Kwords utility ROM
- 16-level, 16-bit-wide hardware stack for storage of program return addresses and general-purpose use

Use the internal memory-management unit (MMU) to map data memory space into a predefined program memory segment for code execution from data memory. Use the MMU to map program memory space as data space for access to constant data stored in program

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memory. Access physical memory segments (other than the stack and register memories) as either program memory or data memory, but not both at once.

By default, the memory is arranged in a Harvard architecture, with separate address spaces for program and data memory. The configuration of program and data space depends on the current execution location.

- When executing code from flash memory, access the SRAM and utility ROM in data space.
- When executing code from SRAM, access the flash memory and utility ROM in data space.
- When executing code from the utility ROM, access the flash memory and SRAM in data space.

Utility ROM (see Section 18 of the MAXQ7667 User's Guide)

The utility ROM is a 4K x 16 block of internal ROM memory that defaults to a starting address of 8000h. The utility ROM consists of subroutines called from application software. The subroutines include:

- In-system programming (bootloader) over the JTAG or UART interface
- In-circuit debug routines
- Test routines (internal memory tests, memory loader, etc.)
- User-callable routines for in-application flash programming and code space table lookup

Following any reset, execution begins in the utility ROM. The ROM software determines whether the program execution immediately jumps to the start of the user-application code (located at address 0000h) or to one of the special routines mentioned above. Call the routines within the utility ROM using the application software. Refer to the *MAXQ7667 User's Guide* for more information on the utility ROM contents.

Password protect in-system programming, in-application programming, and in-circuit debugging functions using a password-lock (PWL) bit. The PWL bit is implemented in the SC register. When the PWL bit is set to one (POR default), the password is required to access the utility ROM, including in-circuit debug and in-system programming routines that allow reading or writing of internal memory. When the PWL bit is cleared to zero, these utilities are fully accessible without the password. The password is automatically set to all ones following a mass erase.

Data Memory

The 2K x 16 internal data SRAM maps into either program or data space. The contents of the SRAM are maintained during stop mode and across non-POR resets, as long as DVDD remains within the operating voltage range.

A data memory cycle requires only one system clock period to support fast internal execution. This allows a complete read or write operation on SRAM in one clock cycle. The MMU handles data memory mapping and access control. Read or write to the data memory with word or byte-wide commands.

Stack Memory

The MAXQ7667 provides a 16 x 16 hardware stack to support subroutine calls and system interrupts. A 16-bit wide internal hardware stack provides storage for program return addresses and general-purpose use. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and interrupts serviced.

Register Set

Sets of registers control most functions. These registers provide a working space for memory operations as well as configuring and addressing peripheral registers on the device. Registers are divided into two major types; system registers and peripheral registers. The register set common to most MAXQ-based devices, also known as the system registers, includes the ALU, accumulator registers, data pointers, interrupt vectors and control, and stack pointer. The peripheral registers define additional functionality. Tables 1 and 3 show the MAXQ7667 register set.

Programming

Two different methods program the flash memory: in-system programming and in-application programming. Both methods afford great flexibility in system design as well as reduce the life-cycle cost of the embedded system. The MAXQ7667 password protects these features to prevent unauthorized access to code memory.

In-System Programming

An internal bootstrap loader reloads the device over a simple JTAG or UART interface allowing cost savings in system software upgrade. During power-up, the MAXQ7667 first checks for activity on the JTAG port. If no activity is present, the device checks if a password-protected program is present. If the password is set,

the application code executes. The application codes initiate reprogramming. If the password is not set, the MAXQ7667 monitors the UART for an autobaud character (0x0D). If this character is received, the device sets its serial baud rate and initiates a boot loader procedure. If 0x0D is not received after five seconds, the device begins execution of the application code.

The following bootloader functions are supported:

- Load
- Dump
- CRC
- Verify
- Erase

In-Application Programming

The in-application programming feature allows the µC to modify its own flash program memory while simultaneously executing its application software. This allows on the fly software updates in mission-critical applications that cannot afford downtime. Erase and program the flash memory using the flash programming functions in the utility ROM. Refer to Section 18 of the *MAXQ7667 User's Guide* for a detailed description of the utility ROM functions.

Stop Mode

Power consumption reaches its minimum in stop mode (STOP = 1). In this mode, the external oscillator, internal RC oscillator, system clock, and all processing halts. Trigger an enabled external interrupt input or directly apply an external reset on $\overline{\text{RESET}}$ to exit stop mode. Upon exiting stop mode, the µC either waits for the external high-frequency crystal to complete its warmup period or starts execution immediately from its internal RC oscillator while the crystal warms up.

Interrupts

Multiple interrupt sources quickly respond to internal and external events. The MAXQ architecture uses a single interrupt vector (IV) and single interrupt-service routine (ISR) design. Enable interrupts globally, individually, or by module. When an interrupt condition occurs, its individual flag is set even if the interrupt source is disabled at the local, module, or global level. Clear interrupt flags within the interrupt routine to avoid repeated false interrupts from the same source. Provide an adequate delay between the write to the flag and the RETI instruction using application software to allow time for the interrupt hardware to remove the internal interrupt condition. Asynchronous interrupt flags require a one-instruction delay and synchronous interrupt flags require a two-instruction delay.

When an enabled interrupt is detected, software jumps to a user-programmable interrupt vector location. The IV register defaults to 0000h on reset or power-up. Once software control transfers to the ISR, use the interrupt identification register (IIR) to determine if the source of the interrupt is a system register or peripheral register. The specified module identifies the specific interrupt source. The following interrupt sources are available:

- Watchdog interrupt
- External interrupts 0–7 on port 0 and port 1
- Timer 0 low compare, low overflow, capture/compare, and overflow interrupts
- Timer 1 low compare, low overflow, capture/compare, and overflow interrupts
- Timer 2 low compare, low overflow, and overflow interrupts
- Schedule timer alarm interrupt
- SPI data transfer complete, mode fault, write collision and receive overrun interrupts
- UART transmit, receive interrupts
- LIN mode master or slave interrupt
- SAR ADC data ready interrupt
- Echo envelope LPF output, FIFO full, and comparator interrupts
- Digital and I/O voltage brownout interrupts
- High-frequency oscillator failure interrupt

Table 1. System Register Map

REGISTER INDEX	MODULE NAME (BASE SPECIFIER)						
	AP (8h)	A (9h)	PFX (Bh)	IP (Ch)	SP (Dh)	DPC (Eh)	DP (Fh)
0h	AP	**A[0]**	**PFX[0]**	**IP**	—	—	—
1h	APC	**A[1]**	**PFX[1]**	—	**SP**	—	—
2h	—	**A[2]**	**PFX[2]**	—	**IV**	—	—
3h	—	**A[3]**	**PFX[3]**	—	—	OFFS	**DP[0]**
4h	PSF	**A[4]**	**PFX[4]**	—	—	**DPC**	—
5h	IC	**A[5]**	**PFX[5]**	—	—	**GR**	—
6h	IMR	**A[6]**	**PFX[6]**	—	**LC[0]**	GRL	—
7h	—	**A[7]**	**PFX[7]**	—	**LC[1]**	**BP**	**DP[1]**
8h	SC	**A[8]**		—	—	***GRS***	—
9h	—	**A[9]**	—	—	—	GRH	—
Ah	—	**A[10]**	—	—	—	***GRXL***	—
Bh	*IIR*	**A[11]**	—	—	—	***FP***	—
Ch	—	**A[12]**	—	—	—	—	—
Dh	—	**A[13]**	—	—	—	—	—
Eh	CKCN	**A[14]**	—	—	—	—	—
Fh	WDCN	**A[15]**	—	—	—	—	—

Note: *Registers in italics are read-only. Registers in bold are 16-bit wide.*

Table 2. System Register Bit and Reset Values

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AP									—	—	—	—	AP (4 Bits)			
									0	0	0	0	0	0	0	0
APC									CLR	IDS	—	—	—	MOD2	MOD1	MOD0
									0	0	0	0	0	0	0	0
PSF									Z	S	—	GPF1	GPF0	OV	C	E
									1	0	0	0	0	0	0	0
IC									—	—	CGDS	—	—	—	INS	IGE
									0	0	0	0	0	0	0	0
IMR									IMS	—	IM5	IM4	IM3	IM2	IM1	IM0
									0	0	0	0	0	0	0	0
SC									TAP	—	CDA1	CDA0	—	ROD	PWL	—
									1	0	0	0	0	0	s*	0
IIR									IIS	—	II5	II4	II3	II2	II1	II0
									0	0	0	0	0	0	0	0
CKCN									XTRC	—	RGMD	STOP	SWB	PMME	CD1	CD0
									s*	0	0	0	0	0	0	0
WDCN									POR	EWDI	WD1	WD0	WDIF	WTRF	EWT	RWT
									s*	s*	0	0	0	s*	s*	0
A[n] (0..15)	A[n] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PFX[n] (0..7)	PFX[n] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IP	IP (16 Bits)															
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SP	—	—	—	—	—	—	—	—	—	—	—	—	SP (4 Bits)			
	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
IV	IV (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LC[0]	LC[0] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LC[1]	LC[1] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**Bits indicated by an "s" are only affected by a POR and not by other forms of reset. These bits are set to 0 after a POR. Refer to the* MAXQ7667 User's Guide *for more information.*

Table 2. System Register Bit and Reset Values (continued)

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFS									OFFS (8 Bits)							
									0	0	0	0	0	0	0	0
DPC	—	—	—	—	—	—	—	—	—	—	—	WBS2	WBS1	WBS0	SDPS1	SDPS0
	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0
GR	GR15	GR14	GR13	GR12	GR11	GR10	GR9	GR8	GR7	GR6	GR5	GR4	GR3	GR2	GR1	GR0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRL									GRL7	GRL6	GRL5	GRL4	GRL3	GRL2	GRL1	GRL0
									0	0	0	0	0	0	0	0
BP	BP (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRS	GRS15	GRS14	GRS13	GRS12	GRS11	GRS10	GRS9	GRS8	GRS7	GRS6	GRS5	GRS4	GRS3	GRS2	GRS1	GRS0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRH									GR15	GR14	GR13	GR12	GR11	GR10	GR9	GR8
									0	0	0	0	0	0	0	0
GRXL	GRXL15	GRXL14	GRXL13	GRXL12	GRXL11	GRXL10	GRXL9	GRXL8	GRXL7	GRXL6	GRXL5	GRXL4	GRXL3	GRXL2	GRXL1	GRXL0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FP	FP (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DP[0]	DP[0] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DP[1]	DP[1] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**Bits indicated by an "s" are only affected by a POR and not by other forms of reset. These bits are set to 0 after a POR. Refer to the* MAXQ7667 User's Guide *for more information.*

Table 3. Peripheral Register Map

REGISTER INDEX	MODULE NAME (BASE SPECIFIER)					
	M0 (0h)	M1 (1h)	M2 (2h)	M3 (3h)	M4 (4h)	M5 (5h)
0h	PO0	MCNT	T2CNA0	T2CNA2	—	BPH
1h	PO1	MA	T2H0	T2H2	—	BTRN
2h	—	MB	T2RH0	T2RH2	—	SARC
3h	EIF0	MC2	T2CH0	T2CH2	—	RCVC
4h	EIF1	MC1	T2CNA1	—	—	PLLF
5h	—	MC0	T2H1	CNT1	—	AIE
6h	—	SPIB	T2RH1	SCON	—	CMPC
7h	—	SPICN	T2CH1	SBUF	—	CMPT
8h	PI0	SPICF	T2CNB0	T2CNB2	—	ASR
9h	PI1	SPICK	T2V0	T2V2	—	SARD
Ah	—	—	T2R0	T2R2	—	LPFC
Bh	EIE0	—	T2C0	T2C2	—	OSCC
Ch	EIE1	MC1R	T2CNB1	FSTAT	—	BPFI
Dh	—	MC0R	T2V1	ERRR	—	BPFO
Eh	—	SCNT	T2R1	CHKSUM	—	LPFD
Fh	—	STIM	T2C1	ISVEC	—	LPFF
10h	PD0	SALM	T2CFG0	T2CFG2	—	APE
11h	PD1	FPCTL	T2CFG1	STA0	—	—
12h	—	—	—	SMD	—	FGAIN
13h	EIES0	—	—	FCON	—	B1COEF
14h	EIES1	—	—	CNT0	—	B2COEF
15h	—	—	—	CNT2	—	B3COEF
16h	—	—	—	IDFB	—	A2A
17h	—	RCTRM	—	SADDR	—	A2B
18h	PS0	—	ICDT0	SADEN	—	—
19h	PS1	—	ICDT1	BT	—	A2D
1Ah	—	—	ICDC	TMR	—	—
1Bh	PR0	—	ICDF	—	—	A3A
1Ch	PR1	ID0	ICDB	—	—	A3B
1Dh	—	ID1	ICDA	—	—	—
1Eh	—	—	ICDD	—	—	A3D
1Fh	—	—	—	—	—	—

Table 4. Peripheral Register Bit Functions and Reset Values (continued)

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICDF	—	—	—	—	—	—	—	—	—	—	—	—	PSS1	PSS0	SPE	TXC
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDB	—	—	—	—	—	—	—	—	ICDB.7	ICDB.6	ICDB.5	ICDB.4	ICDB.3	ICDB.2	ICDB.1	ICDB.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDA	ICDA15	ICDA14	ICDA13	ICDA12	ICDA11	ICDA10	ICDA9	ICDA8	ICDA7	ICDA6	ICDA5	ICDA4	ICDA3	ICDA2	ICDA1	ICDA0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDD	ICDD15	ICDD14	ICDD13	ICDD12	ICDD11	ICDD10	ICDD9	ICDD8	ICDD7	ICDD6	ICDD5	ICDD4	ICDD3	ICDD2	ICDD1	ICDD0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNA2	—	—	—	—	—	—	—	—	ET2	T2OE0	T2POL0	TR2L	TR2	CPRL2	SS2	G2EN
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2H2	—	—	—	—	—	—	—	—	T2H27	T2H26	T2H25	T2H24	T2H23	T2H22	T2H21	T2H20
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2RH2	—	—	—	—	—	—	—	—	T2RH27	T2RH26	T2RH25	T2RH24	T2RH23	T2RH22	T2RH21	T2RH20
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CH2	—	—	—	—	—	—	—	—	T2CH27	T2CH26	T2CH25	T2CH24	T2CH23	T2CH22	T2CH21	T2CH20
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CNT1	—	—	—	—	—	—	—	—	RTN	CK	FL5	FL4	FL3	FL2	FL1	FL0
	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
SCON	—	—	—	—	—	—	—	—	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SBUF	—	—	—	—	—	—	—	—	SBUF7	SBUF6	SBUF5	SBUF4	SBUF3	SBUF2	SBUF1	SBUF0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNB2	—	—	—	—	—	—	—	—	ET2L	T2OE1	T2POL1	—	TF2	TF2L	TCC2	TC2L
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2V2	T2V215	T2V214	T2V213	T2V212	T2V211	T2V210	T2V29	T2V28	T2V27	T2V26	T2V25	T2V24	T2V23	T2V22	T2V21	T2V20
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2R2	T2R215	T2R214	T2R213	T2R212	T2R211	T2R210	T2R29	T2R28	T2R27	T2R26	T2R25	T2R24	T2R23	T2R22	T2R21	T2R20
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2C2	T2C215	T2C214	T2C213	T2C212	T2C211	T2C210	T2C29	T2C28	T2C27	T2C26	T2C25	T2C24	T2C23	T2C22	T2C21	T2C20
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FSTAT	—	—	—	—	—	—	—	—	—	—	TFF	TFAE	TFE	RFF	RFAF	RFE
	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
ERRR	—	—	—	—	—	—	—	—	—	OTE	DME	CKE	P1	PIE	P0	POE
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CHKSUM	CHKSUM15	CHKSUM14	CHKSUM13	CHKSUM12	CHKSUM11	CHKSUM10	CHKSUM9	CHKSUM8	CHKSUM7	CHKSUM6	CHKSUM5	CHKSUM4	CHKSUM3	CHKSUM2	CHKSUM1	CHKSUM0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ISVEC	—	—	—	—	—	—	—	—	—	—	—	—	ISVEC3	ISVEC2	ISVEC1	ISVEC0
	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
T2CFG2	—	—	—	—	—	—	—	—	T2C1	T2DIV2	T2DIV1	T2DIV0	T2MD	CCF1	CCF0	C/T2
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
STA0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INP	BUSY
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SMD	—	—	—	—	—	—	—	—	EIR	OFS	—	—	—	IE	SMOD	FEDE
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FCON	—	—	—	—	—	—	—	—	FTF	FRF	TXFT1	TXFT0	RXFT1	RXFT0	OE	FEN
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CNT0	—	—	—	—	—	—	—	—	WU	FP1	FP0	INE	AUT	INIT	LUN1	LUN0
	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0
CNT2	—	—	—	—	—	—	—	—	—	—	—	DMIS	PM	HDO	FBS	BTH
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IDFB	—	—	IDFBH5	IDFBH4	IDFBH3	IDFBH2	IDFBH1	IDFBH0	—	—	IDFBL5	IDFBL4	IDFBL3	IDFBL2	IDFBL1	IDFBL0
	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
SADDR	—	—	—	—	—	—	—	—	SADDR7	SADDR6	SADDR5	SADDR4	SADDR3	SADDR2	SADDR1	SADDR0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SADEN	—	—	—	—	—	—	—	—	SADEN7	SADEN6	SADEN5	SADEN4	SADEN3	SADEN2	SADEN1	SADEN0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

16-Bit, RISC, Microcontroller-Based, Ultrasonic Distance-Measuring System

Applications Information

Development and Technical Support

A variety of highly versatile, affordably priced development tools for this µC are available from Maxim and third-party suppliers, including:

– Compilers

– Evaluation kit

– Integrated development environments (IDEs)

– JTAG-to-serial converters for programming and debugging

A partial list of development tool vendors can be found at **www.maxim-ic.com/MAXQ_tools**.

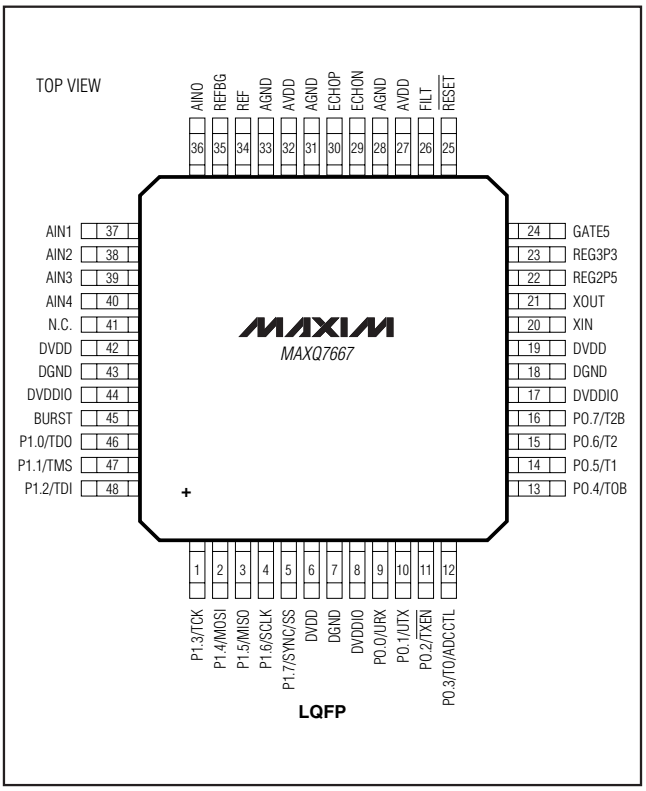
Technical support is available at **https://support.maxim-ic.com/micro**.

Additional Documentation

Designers must have the following documents to fully use all the features of this device. This data sheet contains pin descriptions, feature overviews, and electrical specifications. Errata sheets contain deviations from published specifications. The user's guides offer detailed information about device features and operation. The following documents can be downloaded from **www.maxim-ic.com/microcontrollers**.

- This MAXQ7667 data sheet, which contains electrical/timing specifications and pin descriptions.
- The MAXQ7667 revision-specific errata sheet (**www.maxim-ic.com/errata**).
- The *MAXQ7667 Family User's Guide*, which contains detailed information on core features and operation, including programming.

Pin Configuration



Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 LQFP	C48+2	**21-0054**