Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	119
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs1500-1fgg256i

Global Clocking

Fusion devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there are on-chip oscillators as well as a comprehensive global clock distribution network.

The integrated RC oscillator generates a 100 MHz clock. It is used internally to provide a known clock source to the flash memory read and write control. It can also be used as a source for the PLLs.

The crystal oscillator supports the following operating modes:

- Crystal (32.768 KHz to 20 MHz)
- Ceramic (500 KHz to 8 MHz)
- RC (32.768 KHz to 4 MHz)

Each VersaTile input and output port has access to nine VersaNets: six main and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via MUXes. The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

Digital I/Os with Advanced I/O Standards

The Fusion family of FPGAs features a flexible digital I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). Fusion FPGAs support many different digital I/O standards, both single-ended and differential.

The I/Os are organized into banks, with four or five banks per device. The configuration of these banks determines the I/O standards supported. The banks along the east and west sides of the device support the full range of I/O standards (single-ended and differential). The south bank supports the Analog Quads (analog I/O). In the family's two smaller devices, the north bank supports multiple single-ended digital I/O standards. In the family's larger devices, the north bank is divided into two banks of digital Pro I/Os, supporting a wide variety of single-ended, differential, and voltage-referenced I/O standards.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following applications:

- Single-Data-Rate (SDR) applications
- Double-Data-Rate (DDR) applications—DDR LVDS I/O for chip-to-chip communications
- Fusion banks support LVPECL, LVDS, BLVDS, and M-LVDS with 20 multi-drop points.

VersaTiles

The Fusion core consists of VersaTiles, which are also used in the successful ProASIC3 family. The Fusion VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set and optional enable

Refer to Figure 1-2 for the VersaTile configuration arrangement.

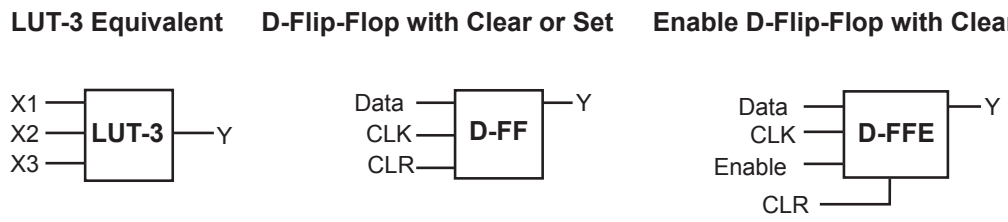


Figure 1-2 • **VersaTile Configurations**

Table 2-7 • AFS250 Global Resource Timing
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.89	1.12	1.02	1.27	1.20	1.50	ns
t_{RCKH}	Input High Delay for Global Clock	0.88	1.14	1.00	1.30	1.17	1.53	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock							ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock							ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.30		0.35	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

Table 2-8 • AFS090 Global Resource Timing
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.84	1.07	0.96	1.21	1.13	1.43	ns
t_{RCKH}	Input High Delay for Global Clock	0.83	1.10	0.95	1.25	1.12	1.47	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock							ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock							ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27		0.30		0.36	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

Offset Error

Offset error indicates how well the actual transfer function matches the ideal transfer function at a single point. For an ideal ADC, the first transition occurs at 0.5 LSB above zero. The offset voltage is measured by applying an analog input such that the ADC outputs all zeroes and increases until the first transition occurs (Figure 2-86).

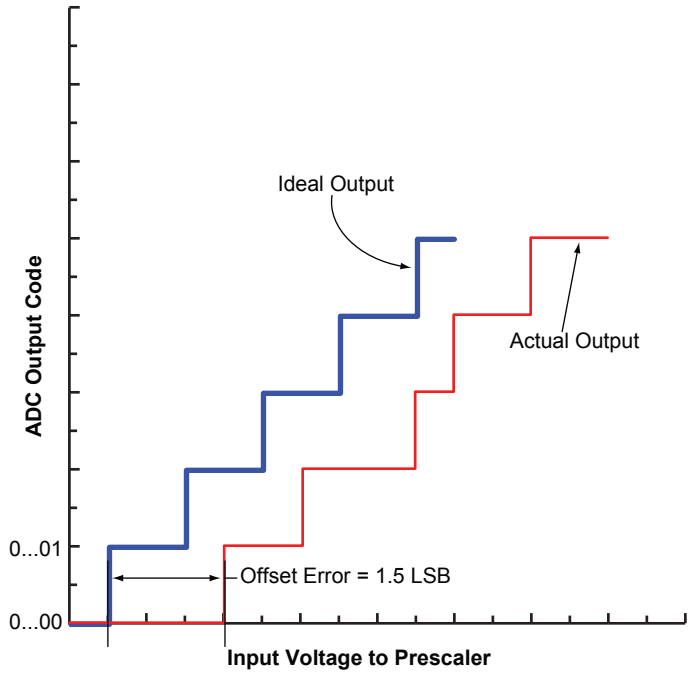


Figure 2-86 • **Offset Error**

Resolution

ADC resolution is the number of bits used to represent an analog input signal. To more accurately replicate the analog signal, resolution needs to be increased.

Sampling Rate

Sampling rate or sample frequency, specified in samples per second (sps), is the rate at which an ADC acquires (samples) the analog input.

SNR – Signal-to-Noise Ratio

SNR is the ratio of the amplitude of the desired signal to the amplitude of the noise signals at a given point in time. For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR (EQ 14) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum ADC noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB[MAX]} = 6.02_{dB} \times N + 1.76_{dB}$$

EQ 14

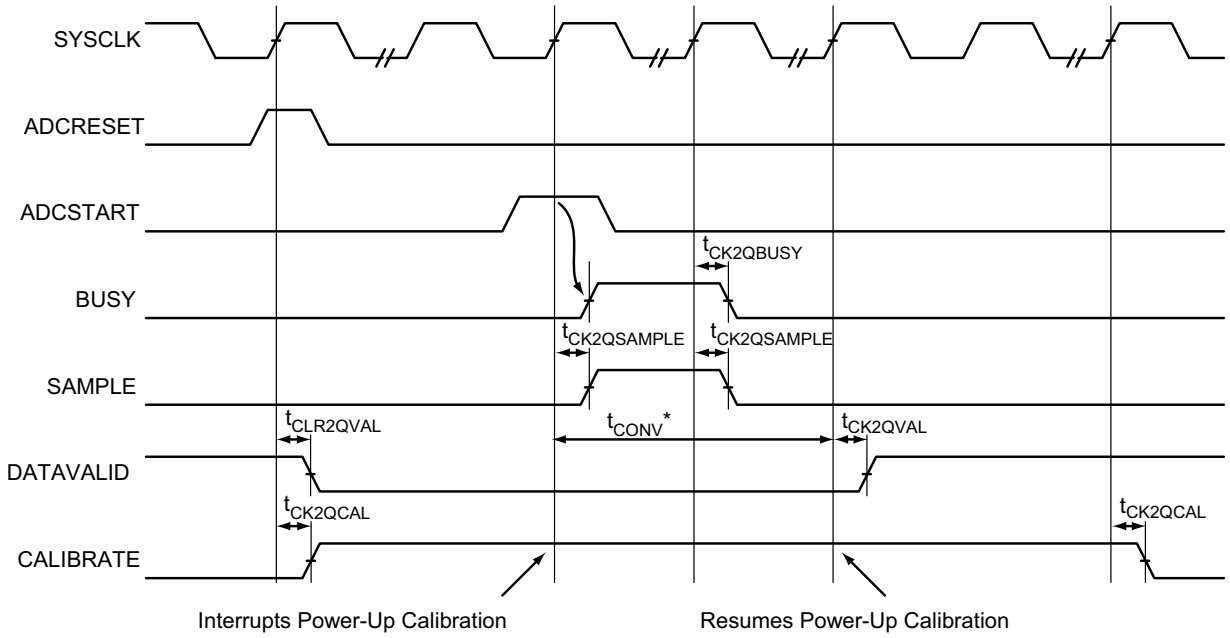
SINAD – Signal-to-Noise and Distortion

SINAD is the ratio of the rms amplitude to the mean value of the root-sum-square of the all other spectral components, including harmonics, but excluding DC. SINAD is a good indication of the overall dynamic performance of an ADC because it includes all components which make up noise and distortion.

Total Harmonic Distortion

THD measures the distortion content of a signal, and is specified in decibels relative to the carrier (dBc). THD is the ratio of the RMS sum of the selected harmonics of the input signal to the fundamental itself. Only harmonics within the Nyquist limit are included in the measurement.

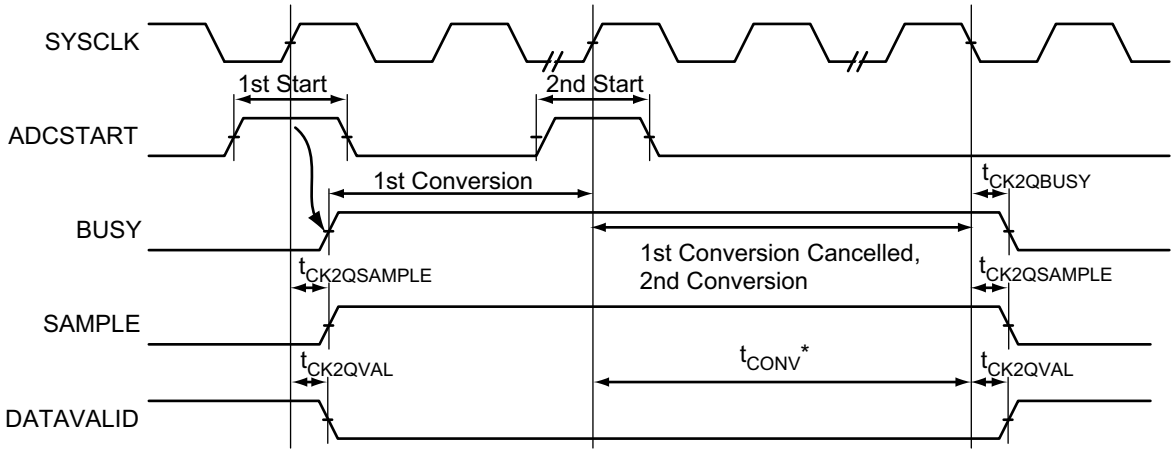
Intra-Conversion



*Note: *t_{CONV} represents the conversion time of the second conversion. See EQ 23 on page 2-109 for calculation of the conversion time, t_{CONV}.*

Figure 2-92 • **Intra-Conversion Timing Diagram**

Injected Conversion



*Note: *See EQ 23 on page 2-109 for calculation on the conversion time, t_{CONV}.*

Figure 2-93 • **Injected Conversion Timing Diagram**

Table 2-50 • ADC Characteristics in Direct Input Mode (continued)
Commercial Temperature Range Conditions, T_J = 85°C (unless noted otherwise),
Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Typ.	Max.	Units
Dynamic Performance						
SNR	Signal-to-Noise Ratio	8-bit mode	48.0	49.5		dB
		10-bit mode	58.0	60.0		dB
		12-bit mode	62.9	64.5		dB
SINAD	Signal-to-Noise Distortion	8-bit mode	47.6	49.5		dB
		10-bit mode	57.4	59.8		dB
		12-bit mode	62.0	64.2		dB
THD	Total Harmonic Distortion	8-bit mode		–74.4	–63.0	dBc
		10-bit mode		–78.3	–63.0	dBc
		12-bit mode		–77.9	–64.4	dBc
ENOB	Effective Number of Bits	8-bit mode	7.6	7.9		bits
		10-bit mode	9.5	9.6		bits
		12-bit mode	10.0	10.4		bits
Conversion Rate						
	Conversion Time	8-bit mode	1.7			µs
		10-bit mode	1.8			µs
		12-bit mode	2			µs
	Sample Rate	8-bit mode			600	Ksps
		10-bit mode			550	Ksps
		12-bit mode			500	Ksps

Notes:

1. *Accuracy of the external reference is 2.56 V ± 4.6 mV.*
2. *Data is based on characterization.*
3. *The sample rate is time-shared among active analog inputs.*

Hot-Swap Support

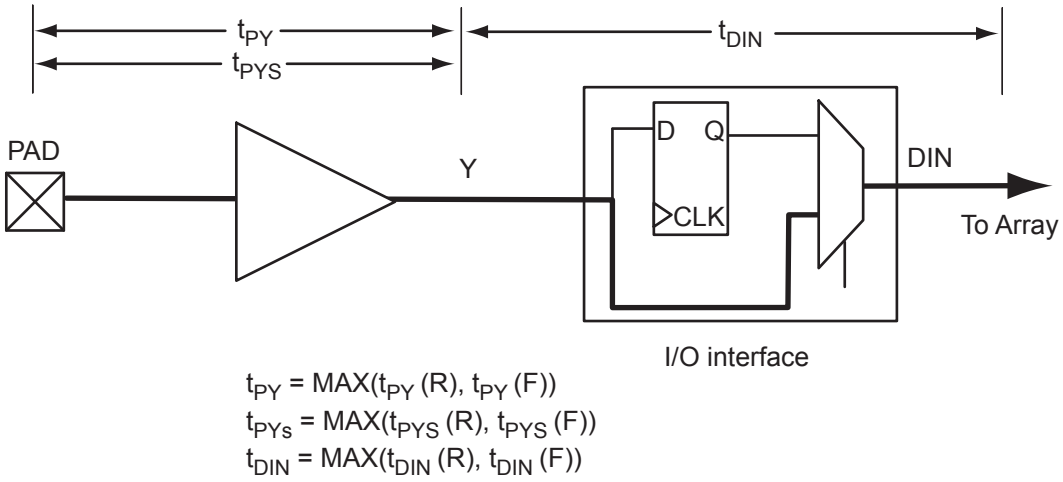
Hot-swapping (also called hot plugging) is the operation of hot insertion or hot removal of a card in (or from) a powered-up system. The levels of hot-swap support and examples of related applications are described in Table 2-74. The I/Os also need to be configured in hot insertion mode if hot plugging compliance is required.

***Table 2-74* • Levels of Hot-Swap Support**

Hot Swapping Level	Description	Power Applied to Device	Bus State	Card Ground Connection	Device Circuitry Connected to Bus Pins	Example of Application with Cards that Contain Fusion Devices	Compliance of Fusion Devices
1	Cold-swap	No	–	–	–	System and card with Microsemi FPGA chip are powered down, then card gets plugged into system, then power supplies are turned on for system but not for FPGA on card.	Compliant I/Os can but do not have to be set to hot insertion mode.
2	Hot-swap while reset	Yes	Held in reset state	Must be made and maintained for 1 ms before, during, and after insertion/removal	–	In PCI hot plug specification, reset control circuitry isolates the card busses until the card supplies are at their nominal operating levels and stable.	Compliant I/Os can but do not have to be set to hot insertion mode.
3	Hot-swap while bus idle	Yes	Held idle (no ongoing I/O processes during insertion/removal)	Same as Level 2	Must remain glitch-free during power-up or power-down	Board bus shared with card bus is "frozen," and there is no toggling activity on bus. It is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal.	Compliant with cards with two levels of staging. I/Os have to be set to hot insertion mode.
4	Hot-swap on an active bus	Yes	Bus may have active I/O processes ongoing, but device being inserted or removed must be idle.	Same as Level 2	Same as Level 3	There is activity on the system bus, and it is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal.	Compliant with cards with two levels of staging. I/Os have to be set to hot insertion mode.

***Table 2-85* • Fusion Pro I/O Attributes vs. I/O Standard Applications**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER	IN_DELAY (input only)	IN_DELAY_VAL (input only)	SCHMITT_TRIGGER (input only)	HOT_SWAPPABLE
LVTTL/LVCMOS 3.3 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 2.5 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 2.5/5.0 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 1.8 V	3	3	3	3	3	3	3	3	3	3
LVCMOS 1.5 V	3	3	3	3	3	3	3	3	3	3
PCI (3.3 V)			3		3	3	3	3		
PCI-X (3.3 V)	3		3		3	3	3	3		
GTL+ (3.3 V)			3		3	3	3	3		3
GTL+ (2.5 V)			3		3	3	3	3		3
GTL (3.3 V)			3		3	3	3	3		3
GTL (2.5 V)			3		3	3	3	3		3
HSTL Class I			3		3	3	3	3		3
HSTL Class II			3		3	3	3	3		3
SSTL2 Class I and II			3		3	3	3	3		3
SSTL3 Class I and II			3		3	3	3	3		3
LVDS, BLVDS, M-LVDS			3			3	3	3		3
LVPECL						3	3	3		3



$t_{PY} = MAX(t_{PY}(R), t_{PY}(F))$
$t_{PYs} = MAX(t_{PYS}(R), t_{PYS}(F))$
$t_{DIN} = MAX(t_{DIN}(R), t_{DIN}(F))$

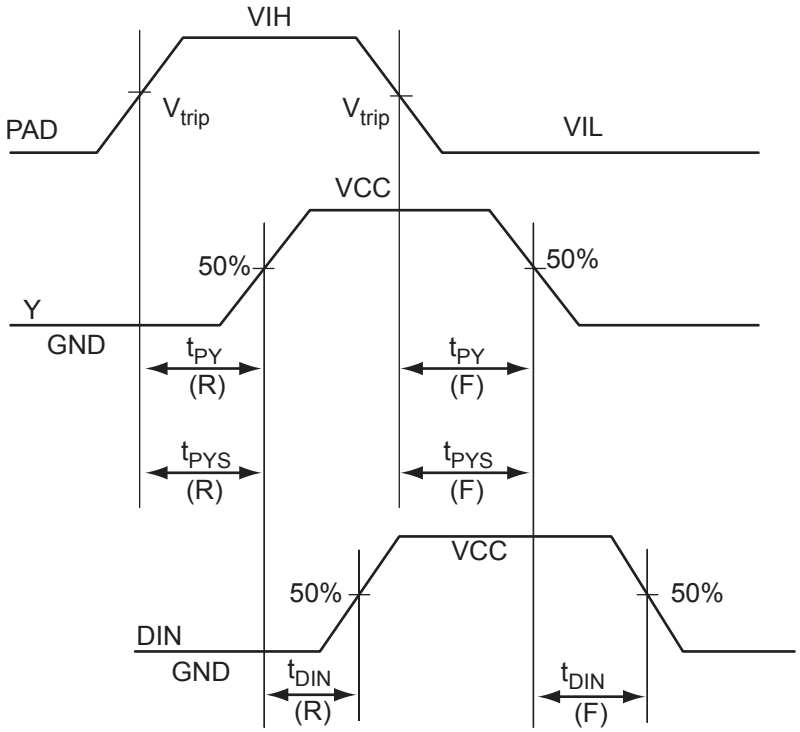


***Figure 2-116* • Input Buffer Timing Model and Delays (example)**

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-165 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
21 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21	109	103	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

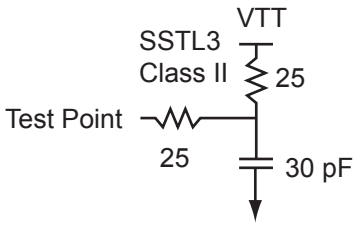


Figure 2-133 • AC Loading

Table 2-166 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-167 • SSTL3- Class II
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.07	0.04	1.25	0.43	2.10	1.67			4.34	3.91	ns
–1	0.56	1.76	0.04	1.06	0.36	1.79	1.42			3.69	3.32	ns
–2	0.49	1.54	0.03	0.93	0.32	1.57	1.25			3.24	2.92	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Output DDR

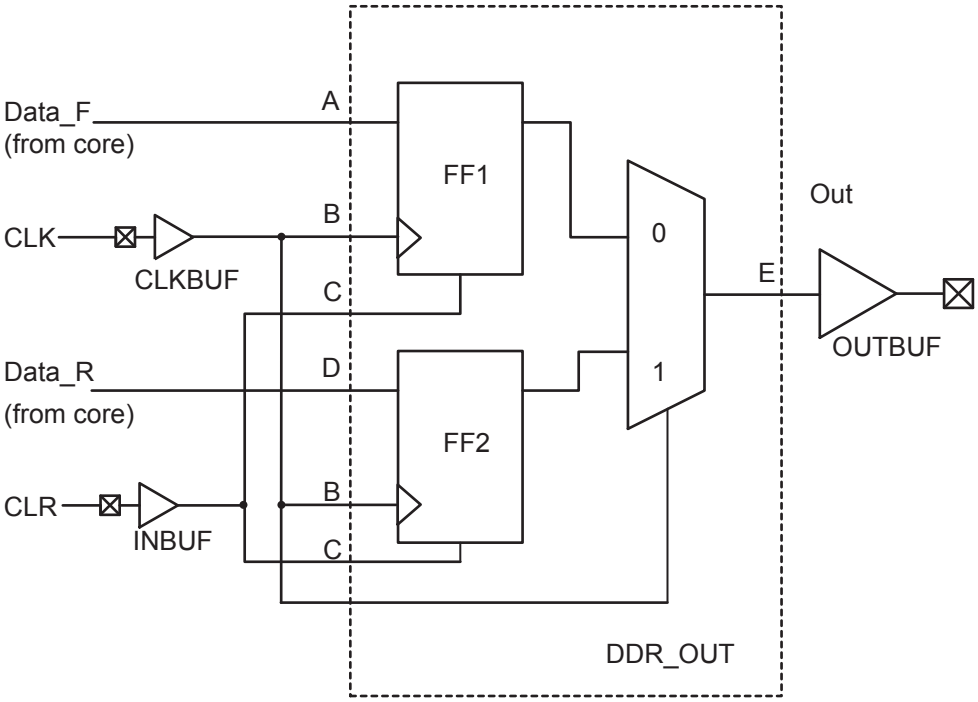


Figure 2-144 • **Output DDR Timing Model**

Table 2-181 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (From, To)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

XTAL2 Crystal Oscillator Circuit Input

Input to crystal oscillator circuit. Pin for connecting external crystal, ceramic resonator, RC network, or external clock input. When using an external crystal or ceramic oscillator, external capacitors are also recommended (Please refer to the crystal oscillator manufacturer for proper capacitor value).

If using external RC network or clock input, XTAL1 should be used and XTAL2 left unconnected. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.

Security

Fusion devices have a built-in 128-bit AES decryption core. The decryption core facilitates highly secure, in-system programming of the FPGA core array fabric and the FlashROM. The FlashROM and the FPGA core fabric can be programmed independently from each other, allowing the FlashROM to be updated without the need for change to the FPGA core fabric. The AES master key is stored in on-chip nonvolatile memory (flash). The AES master key can be preloaded into parts in a security-protected programming environment (such as the Microsemi in-house programming center), and then "blank" parts can be shipped to an untrusted programming or manufacturing center for final personalization with an AES-encrypted bitstream. Late stage product changes or personalization can be implemented easily and with high level security by simply sending a STAPL file with AES-encrypted data. Highly secure remote field updates over public networks (such as the Internet) are possible by sending and programming a STAPL file with AES-encrypted data. For more information, refer to the *Fusion Security* application note.

128-Bit AES Decryption

The 128-bit AES standard (FIPS-197) block cipher is the National Institute of Standards and Technology (NIST) replacement for DES (Data Encryption Standard FIPS46-2). AES has been designed to protect sensitive government information well into the 21st century. It replaces the aging DES, which NIST adopted in 1977 as a Federal Information Processing Standard used by federal agencies to protect sensitive, unclassified information. The 128-bit AES standard has 3.4×10^{38} possible 128-bit key variants, and it has been estimated that it would take 1,000 trillion years to crack 128-bit AES cipher text using exhaustive techniques. Keys are stored (protected with security) in Fusion devices in nonvolatile flash memory. All programming files sent to the device can be authenticated by the part prior to programming to ensure that bad programming data is not loaded into the part that may possibly damage it. All programming verification is performed on-chip, ensuring that the contents of Fusion devices remain as secure as possible.

AES decryption can also be used on the 1,024-bit FlashROM to allow for remote updates of the FlashROM contents. This allows for easy support of subscription model products and protects them with measures designed to provide the highest level of security available. See the application note *Fusion Security* for more details.

AES for Flash Memory

AES decryption can also be used on the flash memory blocks. This provides the best available security during update of the flash memory blocks. During runtime, the encrypted data can be clocked in via the JTAG interface. The data can be passed through the internal AES decryption engine, and the decrypted data can then be stored in the flash memory block.

Programming

Programming can be performed using various programming tools, such as Silicon Sculptor II (BP Micro Systems) or FlashPro3 (Microsemi).

The user can generate STP programming files from the Designer software and can use these files to program a device.

Fusion devices can be programmed in-system. During programming, VCCOSC is needed in order to power the internal 100 MHz oscillator. This oscillator is used as a source for the 20 MHz oscillator that is used to drive the charge pump for programming.

Table 3-2 • **Recommended Operating Conditions**[1]

Symbol	Parameter[2]		Commercial	Industrial	Units
T_J	Junction temperature		0 to +85	–40 to +100	°C
VCC	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage	Programming mode[3]	3.15 to 3.45	3.15 to 3.45	V
		Operation[4]	0 to 3.6	0 to 3.6	V
VCCPLL	Analog power supply (PLL)		1.425 to 1.575	1.425 to 1.575	V
VCCI	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V
VCC33A	+3.3 V power supply		2.97 to 3.63	2.97 to 3.63	V
VCC33PMP	+3.3 V power supply		2.97 to 3.63	2.97 to 3.63	V
VAREF	Voltage reference for ADC		2.527 to 2.593	2.527 to 2.593	V
VCC15A [5]	Digital power supply for the analog system		1.425 to 1.575	1.425 to 1.575	V
VCCNVM	Embedded flash power supply		1.425 to 1.575	1.425 to 1.575	V
VCCOSC	Oscillator power supply		2.97 to 3.63	2.97 to 3.63	V
AV, AC [6]	Unpowered, ADC reset asserted or unconfigured		–10.5 to 12.0	–10.5 to 11.6	V
	Analog input (+16 V to +2 V prescaler range)		–0.3 to 12.0	–0.3 to 11.6	V
	Analog input (+1 V to + 0.125 V prescaler range)		–0.3 to 3.6	–0.3 to 3.6	V
	Analog input (–16 V to –2 V prescaler range)		–10.5 to 0.3	–10.5 to 0.3	V
	Analog input (–1 V to –0.125 V prescaler range)		–3.6 to 0.3	–3.6 to 0.3	V
	Analog input (direct input to ADC)		–0.3 to 3.6	–0.3 to 3.6	V
	Digital input		–0.3 to 12.0	–0.3 to 11.6	V
AG [6]	Unpowered, ADC reset asserted or unconfigured		–10.5 to 12.0	–10.5 to 11.6	V
	Low Current Mode (1 µA, 3 µA, 10 µA, 30 µA)		–0.3 to 12.0	–0.3 to 11.6	V
	Low Current Mode (–1 µA, –3 µA, –10 µA, –30 µA)		–10.5 to 0.3	–10.5 to 0.3	V
	High Current Mode [7]		–10.5 to 12.0	–10.5 to 11.6	V
AT [6]	Unpowered, ADC reset asserted or unconfigured		–0.3 to 15.5	–0.3 to 14.5	V
	Analog input (+16 V, +4 V prescaler range)		–0.3 to 15.5	–0.3 to 14.5	V
	Analog input (direct input to ADC)		–0.3 to 3.6	–0.3 to 3.6	V
	Digital input		–0.3 to 15.5	–0.3 to 14.5	V

Notes:

1. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-85 on page 2-157.*
2. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
3. *The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.*
4. *VPUMP can be left floating during normal operation (not programming mode).*
5. *Violating the V_{CC15A} recommended voltage supply during an embedded flash program cycle can corrupt the page being programmed.*
6. *The input voltage may overshoot by up to 500 mV above the Recommended Maximum (150 mV in Direct mode), provided the duration of the overshoot is less than 50% of the operating lifetime of the device.*
7. *The AG pad should also conform to the limits as specified in Table 2-48 on page 2-114.*

The 1.76 W power is less than the required 3.00 W. The design therefore requires a heat sink, or the airflow where the device is mounted should be increased. The design's total junction-to-air thermal resistance requirement can be estimated by EQ 7:

$$\theta_{ja(total)} = \frac{T_J - T_A}{P} = \frac{100°C - 70°C}{3.00\ W} = 10.00°C/W$$

EQ 7

Determining the heat sink's thermal performance proceeds as follows:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 8

where

θ_{JA} = 0.37°C/W

= Thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

θ_{SA} = Thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 9

$$\theta_{SA} = 13.33°C/W - 8.28°C/W - 0.37°C/W = 5.01°C/W$$

A heat sink with a thermal resistance of 5.01°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with increased airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Microsemi FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device.

Note: The junction-to-air and junction-to-board thermal resistances are based on JEDEC standard (JESD-51) and assumptions made in building the model. It may not be realized in actual application and therefore should be used with a degree of caution. Junction-to-case thermal resistance assumes that all power is dissipated through the case.

Temperature and Voltage Derating Factors

Table 3-7 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, Worst-Case VCC = 1.425 V)**

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	**0°C**	**25°C**	**70°C**	**85°C**	**100°C**
1.425	0.88	0.93	0.95	1.00	1.02	1.05
1.500	0.83	0.88	0.90	0.95	0.96	0.99
1.575	0.80	0.85	0.87	0.91	0.93	0.96

Dynamic Power Consumption of Various Internal Resources

***Table 3-14* • Different Components Contributing to the Dynamic Power Consumption in Fusion Devices**

Parameter	Definition	Power Supply		Device-Specific Dynamic Contributions				Units
		Name	Setting	AFS1500	AFS600	AFS250	AFS090	
PAC1	Clock contribution of a Global Rib	VCC	1.5 V	14.5	12.8	11	11	µW/MHz
PAC2	Clock contribution of a Global Spine	VCC	1.5 V	2.5	1.9	1.6	0.8	µW/MHz
PAC3	Clock contribution of a VersaTile row	VCC	1.5 V	0.81				µW/MHz
PAC4	Clock contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.11				µW/MHz
PAC5	First contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.07				µW/MHz
PAC6	Second contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.29				µW/MHz
PAC7	Contribution of a VersaTile used as a combinatorial module	VCC	1.5 V	0.29				µW/MHz
PAC8	Average contribution of a routing net	VCC	1.5 V	0.70				µW/MHz
PAC9	Contribution of an I/O input pin (standard dependent)	VCCI	See Table 3-12 on page 3-18					
PAC10	Contribution of an I/O output pin (standard dependent)	VCCI	See Table 3-13 on page 3-20					
PAC11	Average contribution of a RAM block during a read operation	VCC	1.5 V	25				µW/MHz
PAC12	Average contribution of a RAM block during a write operation	VCC	1.5 V	30				µW/MHz
PAC13	Dynamic Contribution for PLL	VCC	1.5 V	2.6				µW/MHz
PAC15	Contribution of NVM block during a read operation (F < 33MHz)	VCC	1.5 V	358				µW/MHz
PAC16	1st contribution of NVM block during a read operation (F > 33 MHz)	VCC	1.5 V	12.88				mW
PAC17	2nd contribution of NVM block during a read operation (F > 33 MHz)	VCC	1.5 V	4.8				µW/MHz
PAC18	Crystal Oscillator contribution	VCC33A	3.3 V	0.63				mW
PAC19	RC Oscillator contribution	VCC33A	3.3 V	3.3				mW
PAC20	Analog Block dynamic power contribution of ADC	VCC	1.5 V	3				mW

QN180		
Pin Number	AFS090 Function	AFS250 Function
A1	GNDQ	GNDQ
A2	VCCIB3	VCCIB3
A3	GAB2/IO52NDB3V0	IO74NDB3V0
A4	GFA2/IO51NDB3V0	IO71NDB3V0
A5	GFC2/IO50NDB3V0	IO69NPB3V0
A6	VCCIB3	VCCIB3
A7	GFA1/IO47PPB3V0	GFB1/IO67PPB3V0
A8	GEB0/IO45NDB3V0	NC
A9	XTAL1	XTAL1
A10	GNDOSC	GNDOSC
A11	GEC2/IO43PPB3V0	GEA1/IO61PPB3V0
A12	IO43NPB3V0	GEA0/IO61NPB3V0
A13	NC	VCCIB3
A14	GNDNVM	GNDNVM
A15	PCAP	PCAP
A16	VCC33PMP	VCC33PMP
A17	NC	NC
A18	AV0	AV0
A19	AG0	AG0
A20	ATRTN0	ATRTN0
A21	AG1	AG1
A22	AC1	AC1
A23	AV2	AV2
A24	AT2	AT2
A25	AT3	AT3
A26	AC3	AC3
A27	AV4	AV4
A28	AC4	AC4
A29	AT4	AT4
A30	NC	AG5
A31	NC	AV5
A32	ADCGNDREF	ADCGNDREF
A33	VCC33A	VCC33A
A34	GNDA	GNDA
A35	PTBASE	PTBASE
A36	VCCNVM	VCCNVM

QN180		
Pin Number	AFS090 Function	AFS250 Function
A37	VPUMP	VPUMP
A38	TDI	TDI
A39	TDO	TDO
A40	VJTAG	VJTAG
A41	GDB1/IO39PPB1V0	GDA1/IO54PPB1V0
A42	GDC1/IO38PDB1V0	GDB1/IO53PDB1V0
A43	VCC	VCC
A44	GCB0/IO35NPB1V0	GCB0/IO48NPB1V0
A45	GCC1/IO34PDB1V0	GCC1/IO47PDB1V0
A46	VCCIB1	VCCIB1
A47	GBC2/IO32PPB1V0	GBB2/IO41PPB1V0
A48	VCCIB1	VCCIB1
A49	NC	NC
A50	GBA0/IO29RSB0V0	GBB1/IO37RSB0V0
A51	VCCIB0	VCCIB0
A52	GBB0/IO27RSB0V0	GBC0/IO34RSB0V0
A53	GBC1/IO26RSB0V0	IO33RSB0V0
A54	IO24RSB0V0	IO29RSB0V0
A55	IO21RSB0V0	IO26RSB0V0
A56	VCCIB0	VCCIB0
A57	IO15RSB0V0	IO21RSB0V0
A58	IO10RSB0V0	IO13RSB0V0
A59	IO07RSB0V0	IO10RSB0V0
A60	GAC0/IO04RSB0V0	IO06RSB0V0
A61	GAB1/IO03RSB0V0	GAC1/IO05RSB0V0
A62	VCC	VCC
A63	GAA1/IO01RSB0V0	GAB0/IO02RSB0V0
A64	NC	NC
B1	VCOMPLA	VCOMPLA
B2	GAA2/IO52PDB3V0	GAC2/IO74PDB3V0
B3	GAC2/IO51PDB3V0	GFA2/IO71PDB3V0
B4	GFB2/IO50PDB3V0	GFB2/IO70PSB3V0
B5	VCC	VCC
B6	GFC0/IO49NDB3V0	GFC0/IO68NDB3V0
B7	GEB1/IO45PDB3V0	NC
B8	VCCOSC	VCCOSC

PQ208

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/default.aspx.

FG484		
Pin Number	AFS600 Function	AFS1500 Function
L17	VCCIB2	VCCIB2
L18	IO46PDB2V0	IO69PDB2V0
L19	GCA1/IO45PDB2V0	GCA1/IO64PDB2V0
L20	VCCIB2	VCCIB2
L21	GCC0/IO43NDB2V0	GCC0/IO62NDB2V0
L22	GCC1/IO43PDB2V0	GCC1/IO62PDB2V0
M1	NC	IO103PDB4V0
M2	XTAL1	XTAL1
M3	VCCIB4	VCCIB4
M4	GNDOSC	GNDOSC
M5	GFC0/IO72NDB4V0	GFC0/IO107NDB4V0
M6	VCCIB4	VCCIB4
M7	GFB0/IO71NDB4V0	GFB0/IO106NDB4V0
M8	VCCIB4	VCCIB4
M9	VCC	VCC
M10	GND	GND
M11	VCC	VCC
M12	GND	GND
M13	VCC	VCC
M14	GND	GND
M15	VCCIB2	VCCIB2
M16	IO48NDB2V0	IO70NDB2V0
M17	VCCIB2	VCCIB2
M18	IO46NDB2V0	IO69NDB2V0
M19	GCA0/IO45NDB2V0	GCA0/IO64NDB2V0
M20	VCCIB2	VCCIB2
M21	GCB0/IO44NDB2V0	GCB0/IO63NDB2V0
M22	GCB1/IO44PDB2V0	GCB1/IO63PDB2V0
N1	NC	IO103NDB4V0
N2	GND	GND
N3	IO68PDB4V0	IO101PDB4V0
N4	NC	IO100NPB4V0
N5	GND	GND
N6	NC	IO99PDB4V0
N7	NC	IO97PDB4V0

FG484		
Pin Number	AFS600 Function	AFS1500 Function
N8	GND	GND
N9	GND	GND
N10	VCC	VCC
N11	GND	GND
N12	VCC	VCC
N13	GND	GND
N14	VCC	VCC
N15	GND	GND
N16	GDB2/IO56PDB2V0	GDB2/IO83PDB2V0
N17	NC	IO78PDB2V0
N18	GND	GND
N19	IO47NDB2V0	IO72NDB2V0
N20	IO47PDB2V0	IO72PDB2V0
N21	GND	GND
N22	IO49PDB2V0	IO71PDB2V0
P1	GFA1/IO70PDB4V0	GFA1/IO105PDB4V0
P2	GFA0/IO70NDB4V0	GFA0/IO105NDB4V0
P3	IO68NDB4V0	IO101NDB4V0
P4	IO65PDB4V0	IO96PDB4V0
P5	IO65NDB4V0	IO96NDB4V0
P6	NC	IO99NDB4V0
P7	NC	IO97NDB4V0
P8	VCCIB4	VCCIB4
P9	VCC	VCC
P10	GND	GND
P11	VCC	VCC
P12	GND	GND
P13	VCC	VCC
P14	GND	GND
P15	VCCIB2	VCCIB2
P16	IO56NDB2V0	IO83NDB2V0
P17	NC	IO78NDB2V0
P18	GDA1/IO54PDB2V0	GDA1/IO81PDB2V0
P19	GDB1/IO53PDB2V0	GDB1/IO80PDB2V0
P20	IO51NDB2V0	IO73NDB2V0

FG676	
Pin Number	AFS1500 Function
R21	IO72NDB2V0
R22	IO72PDB2V0
R23	GND
R24	IO71PDB2V0
R25	VCCIB2
R26	IO67NDB2V0
T1	GND
T2	NC
T3	GFA1/IO105PDB4V0
T4	GFA0/IO105NDB4V0
T5	IO101NDB4V0
T6	IO96PDB4V0
T7	IO96NDB4V0
T8	IO99NDB4V0
T9	IO97NDB4V0
T10	VCCIB4
T11	VCC
T12	GND
T13	VCC
T14	GND
T15	VCC
T16	GND
T17	VCCIB2
T18	IO83NDB2V0
T19	IO78NDB2V0
T20	GDA1/IO81PDB2V0
T21	GDB1/IO80PDB2V0
T22	IO73NDB2V0
T23	IO73PDB2V0
T24	IO71NDB2V0
T25	NC
T26	GND
U1	NC
U2	NC
U3	IO102PDB4V0
U4	IO102NDB4V0

FG676	
Pin Number	AFS1500 Function
U5	VCCIB4
U6	IO91PDB4V0
U7	IO91NDB4V0
U8	IO92PDB4V0
U9	GND
U10	GND
U11	VCC33A
U12	GNDA
U13	VCC33A
U14	GNDA
U15	VCC33A
U16	GNDA
U17	VCC
U18	GND
U19	IO74NDB2V0
U20	GDA0/IO81NDB2V0
U21	GDB0/IO80NDB2V0
U22	VCCIB2
U23	IO75NDB2V0
U24	IO75PDB2V0
U25	NC
U26	NC
V1	NC
V2	VCCIB4
V3	IO100PPB4V0
V4	GND
V5	IO95PDB4V0
V6	IO95NDB4V0
V7	VCCIB4
V8	IO92NDB4V0
V9	GNDNVM
V10	GNDA
V11	NC
V12	AV4
V13	NC
V14	AV5

FG676	
Pin Number	AFS1500 Function
V15	AC5
V16	NC
V17	GNDA
V18	IO77PPB2V0
V19	IO74PDB2V0
V20	VCCIB2
V21	IO82NDB2V0
V22	GDA2/IO82PDB2V0
V23	GND
V24	GDC1/IO79PDB2V0
V25	VCCIB2
V26	NC
W1	GND
W2	IO94PPB4V0
W3	IO98PDB4V0
W4	IO98NDB4V0
W5	GEC1/IO90PDB4V0
W6	GEC0/IO90NDB4V0
W7	GND
W8	VCCNVM
W9	VCCIB4
W10	VCC15A
W11	GNDA
W12	AC4
W13	VCC33A
W14	GNDA
W15	AG5
W16	GNDA
W17	PUB
W18	VCCIB2
W19	TDI
W20	GND
W21	IO84NDB2V0
W22	GDC2/IO84PDB2V0
W23	IO77NPB2V0
W24	GDC0/IO79NDB2V0

Revision	Changes	Page
Advance v0.3 (continued)	The "Temperature Monitor" section was updated.	2-96
	EQ 2 is new.	2-103
	The "ADC Description" section was updated.	2-102
	Figure 2-16 • Fusion Clocking Options was updated.	2-20
	Table 2-46 · Analog Channel Specifications was updated.	2-118
	The notes in Table 2-72 • Fusion Standard and Advanced I/O – Hot-Swap and 5 V Input Tolerance Capabilities were updated.	2-144
	The "Simultaneously Switching Outputs and PCB Layout" section is new.	2-149
	LVPECL and LVDS were updated in Table 2-81 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications.	2-157
	LVPECL and LVDS were updated in Table 2-82 • Fusion Pro I/O Attributes vs. I/O Standard Applications.	2-158
	The "Timing Model" was updated.	2-161
	All voltage-referenced Minimum and Maximum DC Input and Output Level tables were updated.	N/A
	All Timing Characteristic tables were updated	N/A
	Table 2-83 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions was updated.	2-165
	Table 2-79 • Summary of I/O Timing Characteristics – Software Default Settings was updated.	2-134
	Table 2-93 • I/O Output Buffer Maximum Resistances [1] was updated.	2-171
	The "BLVDS/M-LVDS" section is new. BLVDS and M-LVDS are two new I/O standards included in the datasheet.	2-211
	The "CoreMP7 and Cortex-M1 Software Tools" section is new.	2-257
	Table 2-83 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions was updated.	2-165
	Table 2-79 • Summary of I/O Timing Characteristics – Software Default Settings was updated.	2-134
	Table 2-93 • I/O Output Buffer Maximum Resistances [1] was updated.	2-171
	The "BLVDS/M-LVDS" section is new. BLVDS and M-LVDS are two new I/O standards included in the datasheet.	2-211
	The "108-Pin QFN" table for the AFS090 device is new.	3-2
	The "180-Pin QFN" table for the AFS090 device is new.	3-4
	The "208-Pin PQFP" table for the AFS090 device is new.	3-8
	The "256-Pin FBGA" table for the AFS090 device is new.	3-12
	The "256-Pin FBGA" table for the AFS250 device is new.	3-12

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.

51700092-6/03.14