Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	223
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs1500-1fgg484i

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

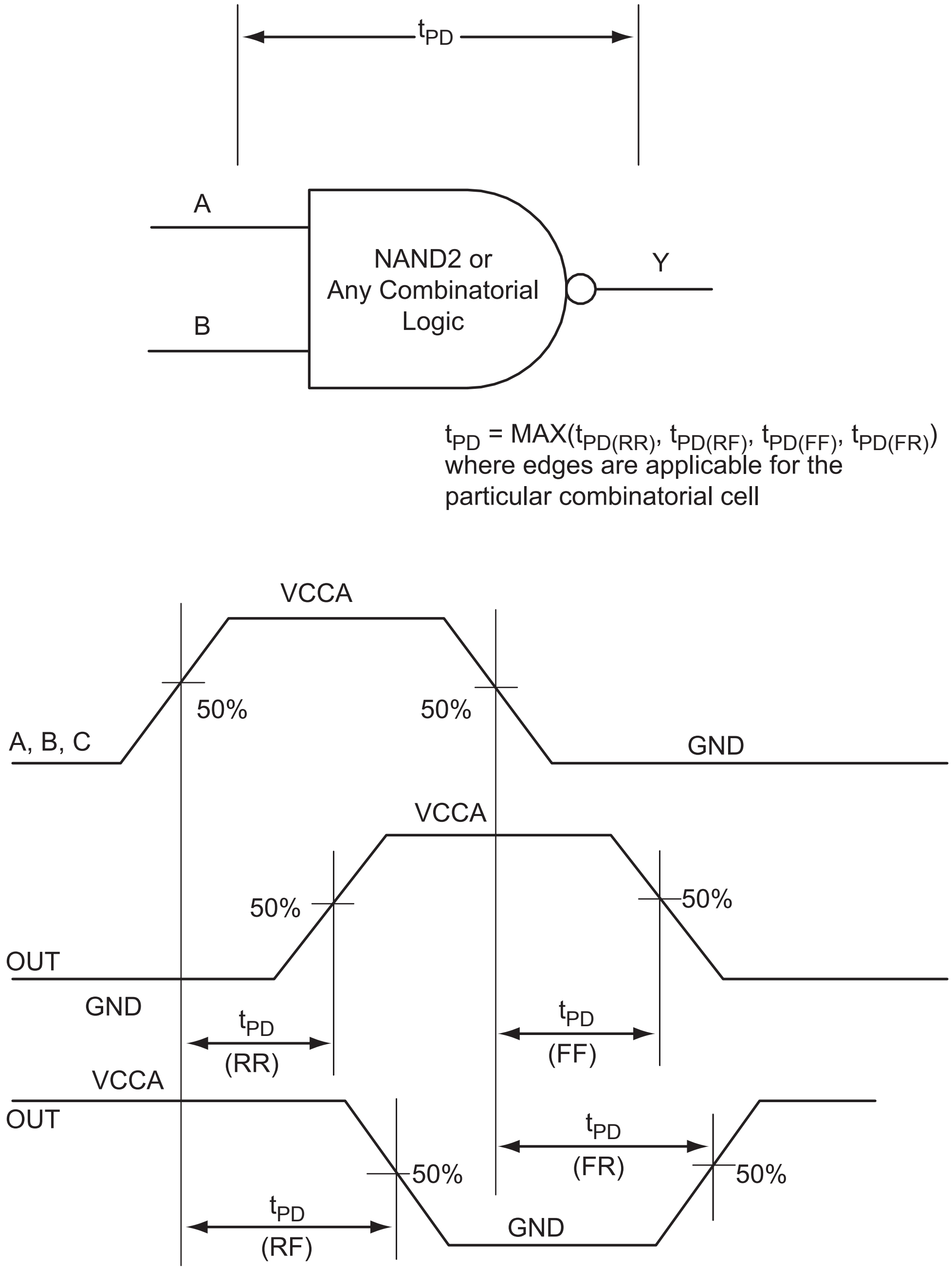

Figure 2-4 • **Combinatorial Timing Model and Waveforms**

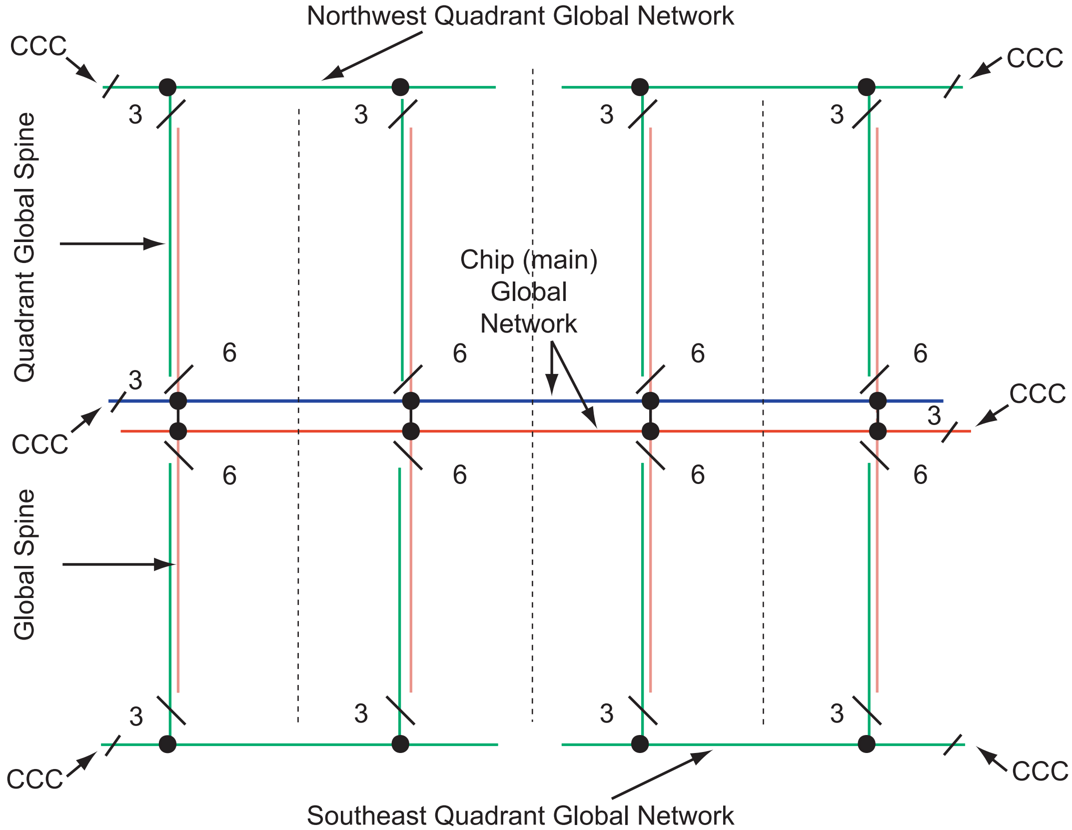

***Figure 2-12* • Global Network Architecture**

***Table 2-4* • Globals/Spines/Rows by Device**

	AFS090	AFS250	AFS600	AFS1500
Global VersaNets (trees)*	9	9	9	9
VersaNet Spines/Tree	4	8	12	20
Total Spines	36	72	108	180
VersaTiles in Each Top or Bottom Spine	384	768	1,152	1,920
Total VersaTiles	2,304	6,144	13,824	38,400

*Note: *There are six chip (main) globals and three globals per quadrant.*

Table 2-16 **• RTC Control/Status Register**

Bit	Name	Description	Default Value
7	rtc_rst	RTC Reset 1 – Resets the RTC 0 – Deassert reset on after two ACM_CLK cycle.	
6	cntr_en	Counter Enable 1 – Enables the counter; rtc_rst must be deasserted as well. First counter increments after 64 RTCCLK positive edges. 0 – Disables the crystal prescaler but does not reset the counter value. Counter value can only be updated when the counter is disabled.	0
5	vr_en_mat	Voltage Regulator Enable on Match 1 – Enables RTCMATCH and RTCPSMMATCH to output 1 when the counter value equals the Match Register value. This enables the 1.5 V voltage regulator when RTCPSMMATCH connects to the RTCPSMMATCH signal in VRPSM. 0 – RTCMATCH and RTCPSMMATCH output 0 at all times.	0
4:3	xt_mode[1:0]	Crystal Mode Controls RTCXTLMODE[1:0]. Connects to RTC_MODE signal in XTLOSC. XTL_MODE uses this value when xtal_en is 1. See the "Crystal Oscillator" section on page 2-20 for mode configuration.	00
2	rst_cnt_omat	Reset Counter on Match 1 – Enables the sync clear of the counter when the counter value equals the Match Register value. The counter clears on the rising edge of the clock. If all the Match Registers are set to 0, the clear is disabled. 0 – Counter increments indefinitely	0
1	rstb_cnt	Counter Reset, active Low 0 - Resets the 40-bit counter value	0
0	xtal_en	Crystal Enable Controls RTCXTLSEL. Connects to SELMODE signal in XTLOSC. 0 – XTLOSC enables control by FPGA_EN; xt_mode is not used. Sleep mode requires this bit to equal 0. 1 – Enables XTLOSC, XTL_MODE control by xt_mode Standby mode requires this bit to be set to 1. See the "Crystal Oscillator" section on page 2-20 for further details on SELMODE configuration.	0

Program Operation

A Program operation is initiated by asserting the PROGRAM signal on the interface. Program operations save the contents of the Page Buffer to the FB Array. Due to the technologies inherent in the FB, the total programming (including erase) time per page of the eNVM is 6.8 ms. While the FB is writing the data to the array, the BUSY signal will be asserted.

During a Program operation, the sector and page addresses on ADDR are compared with the stored address for the page (and sector) in the Page Buffer. If there is a mismatch between the two addresses, the Program operation will be aborted and an error will be reported on the STATUS output.

It is possible to write the Page Buffer to a different page in memory. When asserting the PROGRAM pin, if OVERWRITEPAGE is asserted as well, the FB will write the contents of the Page Buffer to the sector and page designated on the ADDR inputs if the destination page is not Overwrite Protected.

A Program operation can be utilized to either modify the contents of the page in the flash memory block or change the protections for the page. Setting the OVERWRITEPROTECT bit on the interface while asserting the PROGRAM pin will put the page addressed into Overwrite Protect Mode. Overwrite Protect Mode safeguards a page from being inadvertently overwritten during subsequent Program or Erase operations.

Program operations that result in a STATUS value of '01' do not modify the addressed page. For all other values of STATUS, the addressed page is modified. Program errors include the following:

1. Attempting to program a page that is Overwrite Protected (STATUS = '01')
2. Attempting to program a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection Mode (STATUS = '01')
3. Attempting to perform a program with OVERWRITEPAGE set when the page addressed has been Overwrite Protected (STATUS = '01')
4. The Write Count of the page programmed exceeding the Write Threshold defined in the part specification (STATUS = '11')
5. The ECC Logic determining that there is an uncorrectable error within the programmed page (STATUS = '10')
6. Attempting to program a page that is **not** in the Page Buffer when OVERWRITEPAGE is not set and the page in the Page Buffer is modified (STATUS = '01')
7. Attempting to program the page in the Page Buffer when the Page Buffer is **not** modified

The waveform for a Program operation is shown in Figure 2-36.

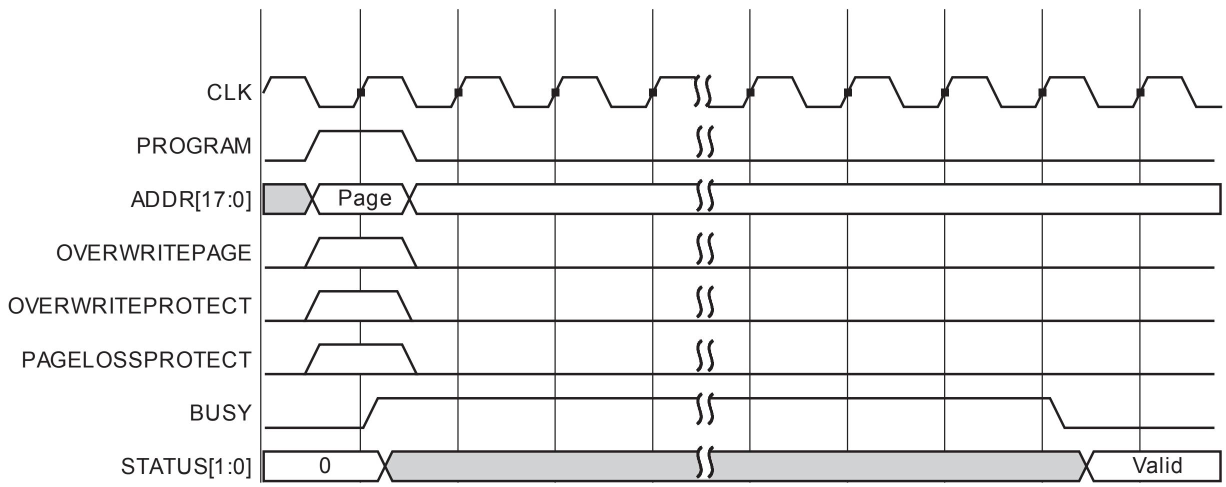

Figure 2-36 • **FB Program Waveform**

Note: OVERWRITEPAGE is only sampled when the PROGRAM or ERASEPAGE pins are asserted. OVERWRITEPAGE is ignored in all other operations.

Erase Page Operation

The Erase Page operation is initiated when the ERASEPAGE pin is asserted. The Erase Page operation allows the user to erase (set user data to zero) any page within the FB.

The use of the OVERWRITEPAGE and PAGELOSSPROTECT pins is the same for erase as for a Program Page operation.

As with the Program Page operation, a STATUS of '01' indicates that the addressed page is not erased.

A waveform for an Erase Page operation is shown in Figure 2-37.

Erase errors include the following:

1. Attempting to erase a page that is Overwrite Protected (STATUS = '01')
2. Attempting to erase a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection mode (STATUS = '01')
3. The Write Count of the erased page exceeding the Write Threshold defined in the part specification (STATUS = '11')
4. The ECC Logic determining that there is an uncorrectable error within the erased page (STATUS = '10')

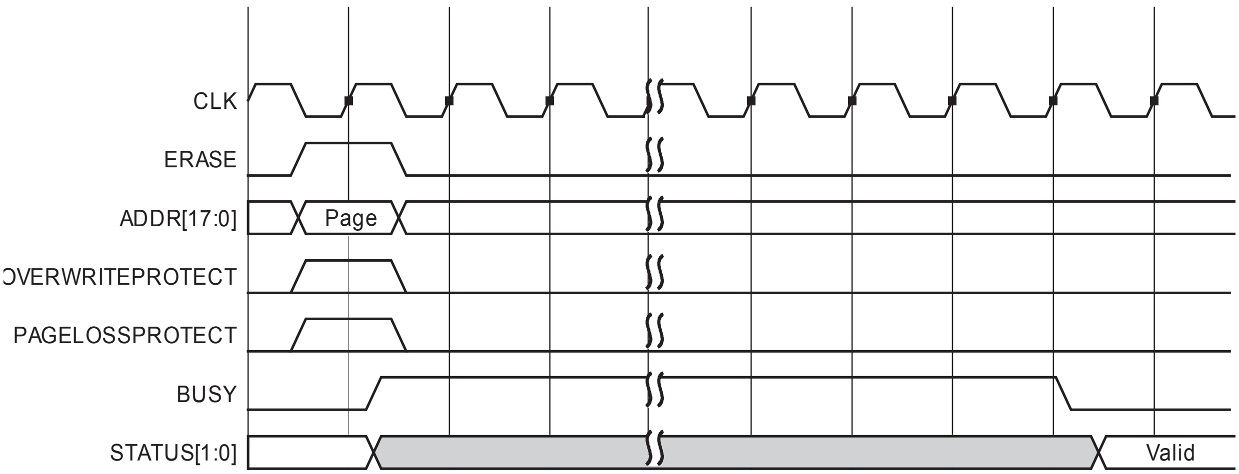

***Figure 2-37* • FB Erase Page Waveform**

The following error indications are possible for Read operations:

1. STATUS = '01' when a single-bit data error was detected and corrected within the block addressed.
2. STATUS = '10' when a double-bit error was detected in the block addressed (note that the error is uncorrected).

In addition to data reads, users can read the status of any page in the FB by asserting PAGESTATUS along with REN. The format of the data returned by a page status read is shown in Table 2-23, and the definition of the page status bits is shown in Table 2-24.

Table 2-23 **• Page Status Read Data Format**

31	8	7	4	3	2	1	0
Write Count		Reserved		Over Threshold	Read Protected	Write Protected	Overwrite Protected

Table 2-24 **• Page Status Bit Definition**

Page Status Bit(s)	Definition
31–8	The number of times the page addressed has been programmed/erased
7–4	Reserved; read as 0
3	Over Threshold indicator (see the"Program Operation" section on page 2-46)
2	Read Protected; read protect bit for page, which is set via the JTAG interface and only affects JTAG operations. This bit can be overridden by using the correct user key value.
1	Write Protected; write protect bit for page, which is set via the JTAG interface and only affects JTAG operations. This bit can be overridden by using the correct user key value.
0	Overwrite Protected; designates that the user has set the OVERWRITEPROTECT bit on the interface while doing a Program operation. The page cannot be written without first performing an Unprotect Page operation.

Table 2-32 **• RAM512X18**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.28	0.33	ns
t_{AH}	Address hold time	0.00	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.09	0.10	0.12	ns
t_{ENH}	REN, WEN hold time	0.06	0.07	0.08	ns
t_{DS}	Input data (WD) setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	2.16	2.46	2.89	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	0.90	1.02	1.20	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.50	0.43	0.38	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge	0.59	0.50	0.44	ns
t_{RSTBQ}[1]	RESET Low to data out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to data out Low on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.21	0.24	0.29	ns
t_{CYC}	Clock cycle time	3.23	3.68	4.32	ns
F_{MAX}	Maximum frequency	310	272	231	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For the derating values at specific junction temperature and voltage supply levels, refer to* *Table 3-7 on page 3-9*.

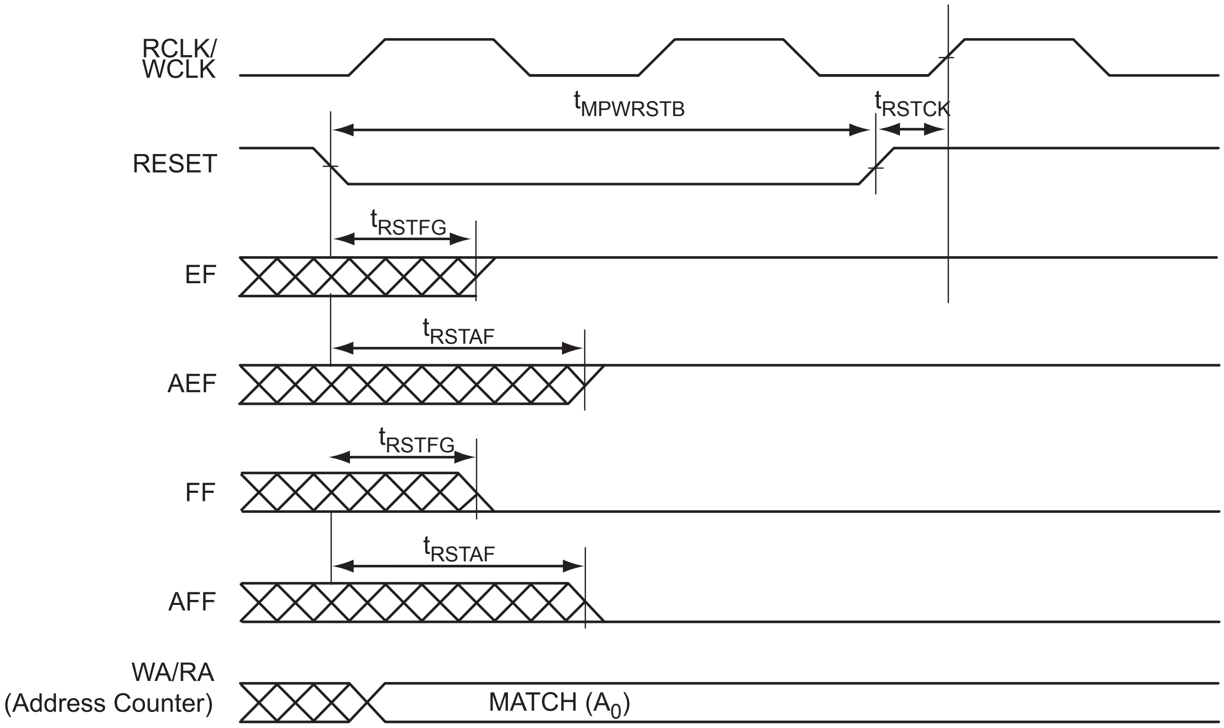

Figure 2-59 **• FIFO Reset**

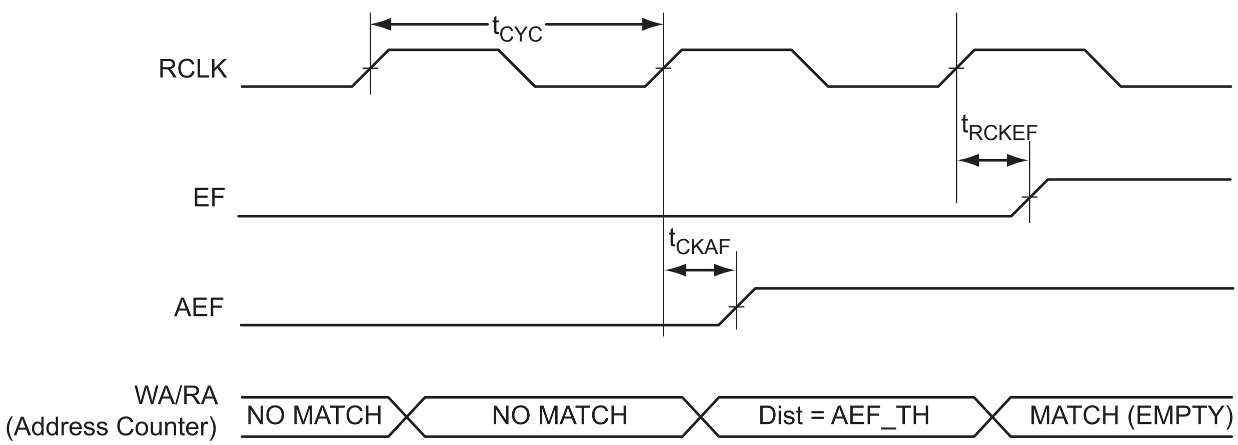

Figure 2-60 **• FIFO EMPTY Flag and AEMPTY Flag Assertion**

User I/Os

Introduction

Fusion devices feature a flexible I/O structure, supporting a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) through a bank-selectable voltage. Table 2-68, Table 2-69, Table 2-70, and Table 2-71 on page 2-135 show the voltages and the compatible I/O standards. I/Os provide programmable slew rates, drive strengths, weak pull-up, and weak pull-down circuits. 3.3 V PCI and 3.3 V PCI-X are 5 V–tolerant. See the "5 V Input Tolerance" section on page 2-144 for possible implementations of 5 V tolerance.

All I/Os are in a known state during power-up, and any power-up sequence is allowed without current impact. Refer to the "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" section on page 3-5 for more information. In low power standby or sleep mode (VCC is OFF, VCC33A is ON, VCCI is ON) or when the resource is not used, digital inputs are tristated, digital outputs are tristated, and digital bibufs (input/output) are tristated.

I/O Tile

The Fusion I/O tile provides a flexible, programmable structure for implementing a large number of I/O standards. In addition, the registers available in the I/O tile in selected I/O banks can be used to support high-performance register inputs and outputs, with register enable if desired (Figure 2-99 on page 2-133). The registers can also be used to support the JESD-79C DDR standard within the I/O structure (see the "Double Data Rate (DDR) Support" section on page 2-139 for more information).

As depicted in Figure 2-100 on page 2-138, all I/O registers share one CLR port. The output register and output enable register share one CLK port. Refer to the "I/O Registers" section on page 2-138 for more information.

I/O Banks and I/O Standards Compatibility

The digital I/Os are grouped into I/O voltage banks. There are three digital I/O banks on the AFS090 and AFS250 devices and four digital I/O banks on the AFS600 and AFS1500 devices. Figure 2-113 on page 2-158 and Figure 2-114 on page 2-159 show the bank configuration by device. The north side of the I/O in the AFS600 and AFS1500 devices comprises two banks of Pro I/Os. The Pro I/Os support a wide number of voltage-referenced I/O standards in addition to the multitude of single-ended and differential I/O standards common throughout all Microsemi digital I/Os. Each I/O voltage bank has dedicated I/O supply and ground voltages (VCCI/GNDQ for input buffers and VCCI/GND for output buffers). Because of these dedicated supplies, only I/Os with compatible standards can be assigned to the same I/O voltage bank. Table 2-69 and Table 2-70 on page 2-134 show the required voltage compatibility values for each of these voltages.

For more information about I/O and global assignments to I/O banks, refer to the specific pin table of the device in the "Package Pin Assignments" on page 4-1 and the "User I/O Naming Convention" section on page 2-158.

Each Pro I/O bank is divided into minibanks. Any user I/O in a VREF minibank (a minibank is the region of scope of a VREF pin) can be configured as a VREF pin (Figure 2-99 on page 2-133). Only one VREF pin is needed to control the entire VREF minibank. The location and scope of the VREF minibanks can be determined by the I/O name. For details, see the "User I/O Naming Convention" section on page 2-158.

Table 2-70 on page 2-134 shows the I/O standards supported by Fusion devices and the corresponding voltage levels.

I/O standards are compatible if the following are true:

- Their VCCI values are identical.
- If both of the standards need a VREF, their VREF values must be identical (Pro I/O only).

At the system level, the skew circuit can be used in applications where transmission activities on bidirectional data lines need to be coordinated. This circuit, when selected, provides a timing margin that can prevent bus contention and subsequent data loss or transmitter overstress due to transmitter-to-transmitter current shorts. Figure 2-110 presents an example of the skew circuit implementation in a bidirectional communication system. Figure 2-111 shows how bus contention is created, and Figure 2-112 on page 2-151 shows how it can be avoided with the skew circuit.

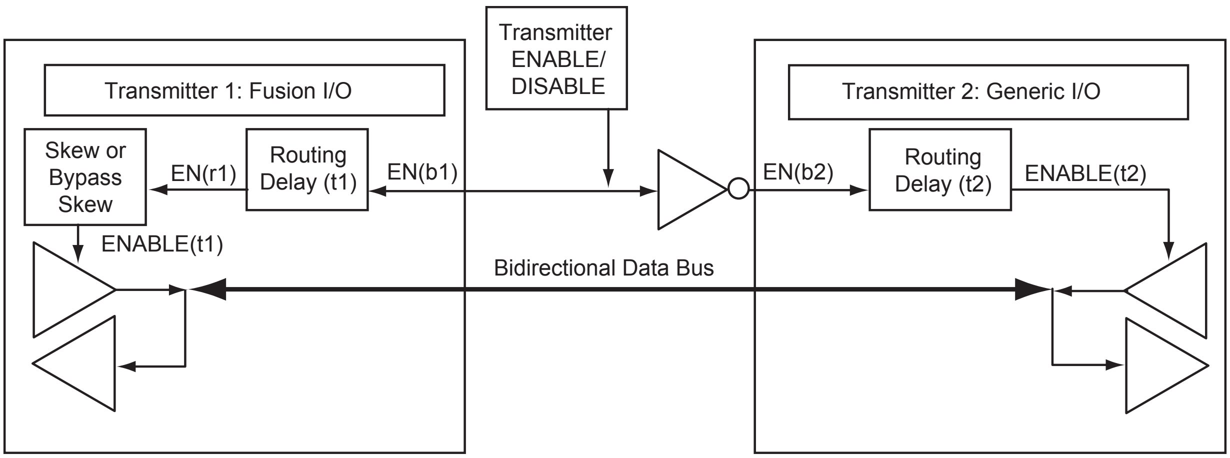

Figure 2-110 • **Example of Implementation of Skew Circuits in Bidirectional Transmission Systems Using Fusion Devices**

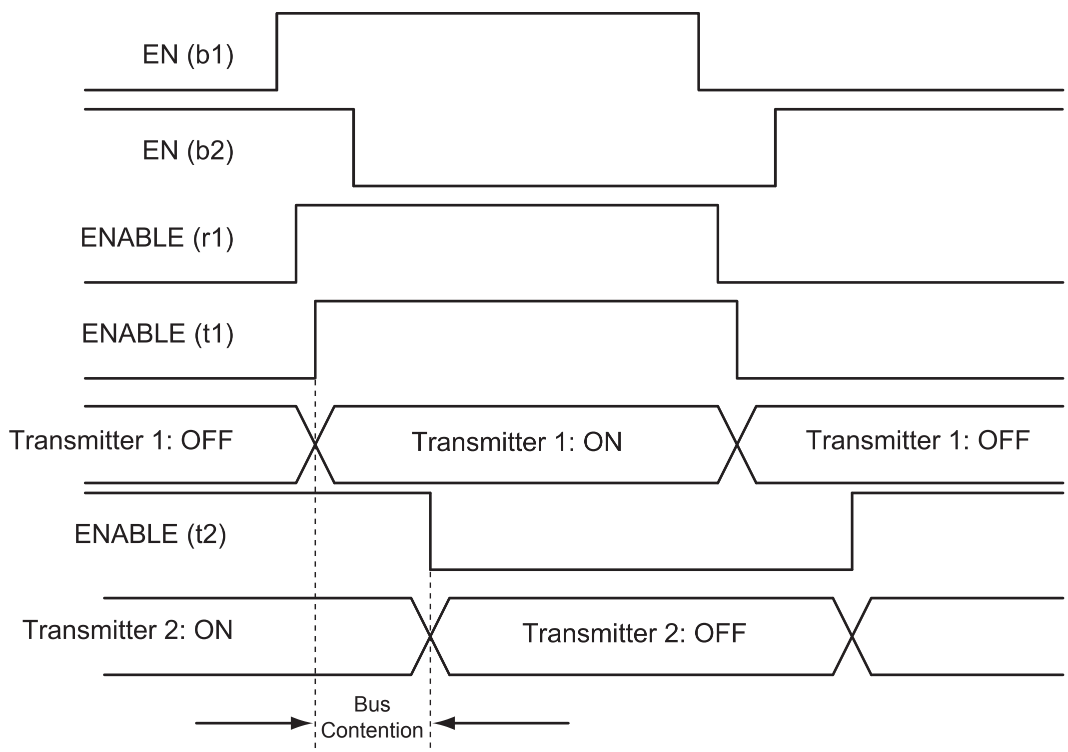

Figure 2-111 • **Timing Diagram (bypasses skew circuit)**

User I/O Characteristics

Timing Model

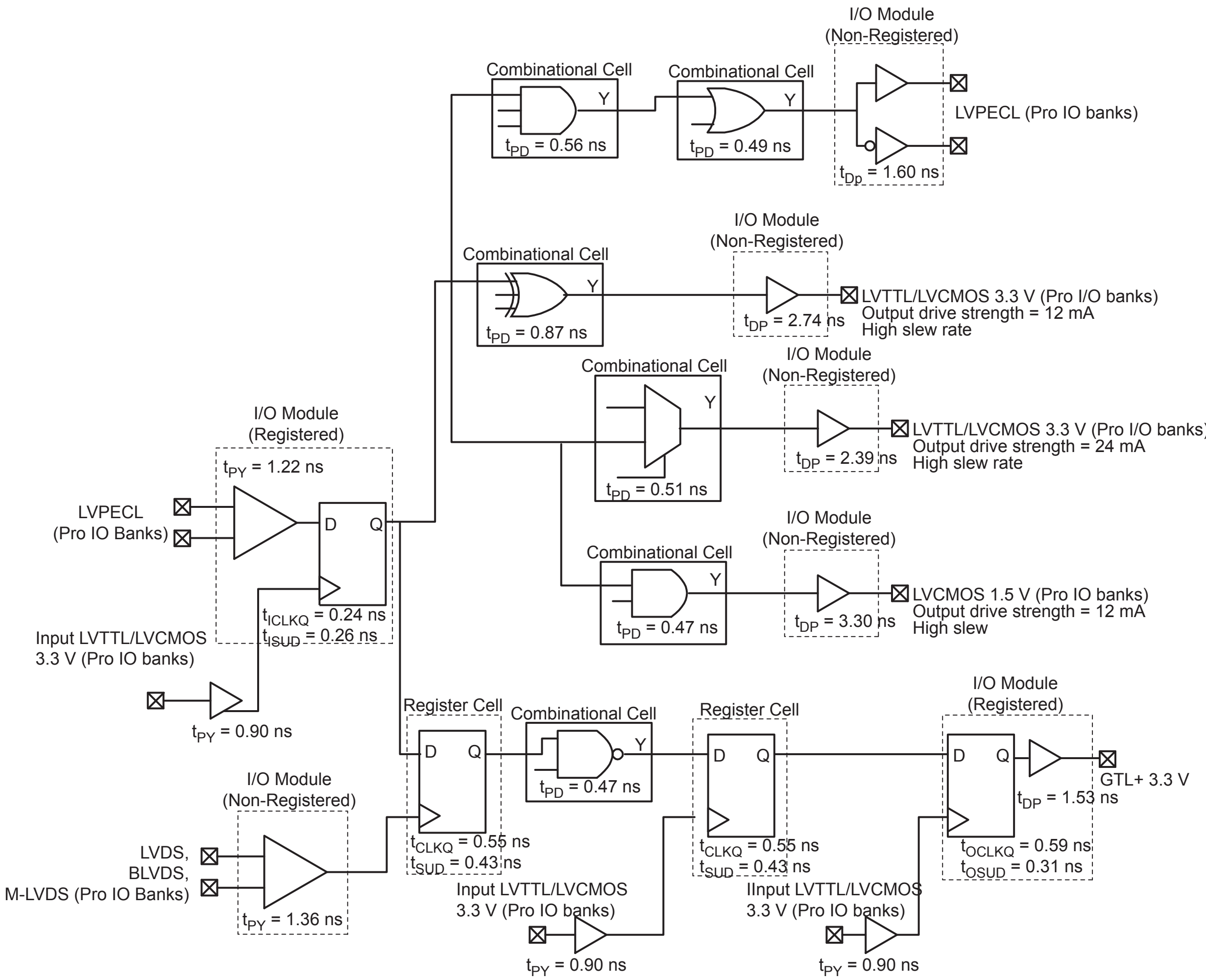

Figure 2-115 **• Timing Model**
Operating Conditions: –2 Speed, Commercial Temperature Range (T_J = 70°C), Worst-Case VCC = 1.425 V

Detailed I/O DC Characteristics

Table 2-95 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

Table 2-96 • I/O Output Buffer Maximum Resistances [1]

Standard	Drive Strength	$R_{PULL-DOWN}$ (ohms) [2]	$R_{PULL-UP}$ (ohms) [3]
Applicable to Pro I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75
3.3 V GTL	20 mA	11	–
2.5 V GTL	20 mA	14	–
3.3 V GTL+	35 mA	12	–
2.5 V GTL+	33 mA	15	–

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/techdocs/models/ibis.html.*
2. $R_{(PULL-DOWN-MAX)} = VOLspec / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (VCCImax – VOHspec) / IOHspec$

Table 2-98 • I/O Short Currents IOSH/IOSL (continued)

	Drive Strength	IOSH (mA)*	IOSL (mA)*
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109
Applicable to Standard I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
1.5 V LVCMOS	2 mA	13	16

Note: *T_J = 100°C

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

***Table 2-99* • Short Current Event Duration before Failure**

Temperature	Time Before Failure
–40°C	>20 years
0°C	>20 years
25°C	>20 years
70°C	5 years
85°C	2 years
100°C	6 months

***Table 2-100* • Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

***Table 2-101* • I/O Input Rise Time, Fall Time, and Related I/O Reliability**

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns*	20 years (100°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis	20 years (100°C)
HSTL/SSTL/GTL	No requirement	10 ns*	10 years (100°C)
LVDS/BLVDS/M-LVDS/LVPECL	No requirement	10 ns*	10 years (100°C)

*Note: * The maximum input rise/fall time is related only to the noise induced into the input buffer trace. If the noise is low, the rise time and fall time of input buffers, when Schmitt trigger is disabled, can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure there is no excessive noise coupling into input signals.*

Table 2-103 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	35

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-104 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Pro I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	11.01	0.04	1.20	1.57	0.43	11.21	9.05	2.69	2.44	13.45	11.29	ns
	–1	0.56	9.36	0.04	1.02	1.33	0.36	9.54	7.70	2.29	2.08	11.44	9.60	ns
	–2	0.49	8.22	0.03	0.90	1.17	0.32	8.37	6.76	2.01	1.82	10.04	8.43	ns
8 mA	Std.	0.66	7.86	0.04	1.20	1.57	0.43	8.01	6.44	3.04	3.06	10.24	8.68	ns
	–1	0.56	6.69	0.04	1.02	1.33	0.36	6.81	5.48	2.58	2.61	8.71	7.38	ns
	–2	0.49	5.87	0.03	0.90	1.17	0.32	5.98	4.81	2.27	2.29	7.65	6.48	ns
12 mA	Std.	0.66	6.03	0.04	1.20	1.57	0.43	6.14	5.02	3.28	3.47	8.37	7.26	ns
	–1	0.56	5.13	0.04	1.02	1.33	0.36	5.22	4.27	2.79	2.95	7.12	6.17	ns
	–2	0.49	4.50	0.03	0.90	1.17	0.32	4.58	3.75	2.45	2.59	6.25	5.42	ns
16 mA	Std.	0.66	5.62	0.04	1.20	1.57	0.43	5.72	4.72	3.32	3.58	7.96	6.96	ns
	–1	0.56	4.78	0.04	1.02	1.33	0.36	4.87	4.02	2.83	3.04	6.77	5.92	ns
	–2	0.49	4.20	0.03	0.90	1.17	0.32	4.27	3.53	2.48	2.67	5.94	5.20	ns
24 mA	Std.	0.66	5.24	0.04	1.20	1.57	0.43	5.34	4.69	3.39	3.96	7.58	6.93	ns
	–1	0.56	4.46	0.04	1.02	1.33	0.36	4.54	3.99	2.88	3.37	6.44	5.89	ns
	–2	0.49	3.92	0.03	0.90	1.17	0.32	3.99	3.50	2.53	2.96	5.66	5.17	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-130 • **1.5 V LVCMOS Low Slew**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	12.78	0.04	1.31	0.43	12.81	12.78	3.40	2.64	15.05	15.02	ns
	–1	0.56	10.87	0.04	1.11	0.36	10.90	10.87	2.89	2.25	12.80	12.78	ns
	–2	0.49	9.55	0.03	0.98	0.32	9.57	9.55	2.54	1.97	11.24	11.22	ns
4 mA	Std.	0.66	10.01	0.04	1.31	0.43	10.19	9.55	3.75	3.27	12.43	11.78	ns
	–1	0.56	8.51	0.04	1.11	0.36	8.67	8.12	3.19	2.78	10.57	10.02	ns
	–2	0.49	7.47	0.03	0.98	0.32	7.61	7.13	2.80	2.44	9.28	8.80	ns
8 mA	Std.	0.66	9.33	0.04	1.31	0.43	9.51	8.89	3.83	3.43	11.74	11.13	ns
	–1	0.56	7.94	0.04	1.11	0.36	8.09	7.56	3.26	2.92	9.99	9.47	ns
	–2	0.49	6.97	0.03	0.98	0.32	7.10	6.64	2.86	2.56	8.77	8.31	ns
12 mA	Std.	0.66	8.91	0.04	1.31	0.43	9.07	8.89	3.95	4.05	11.31	11.13	ns
	–1	0.56	7.58	0.04	1.11	0.36	7.72	7.57	3.36	3.44	9.62	9.47	ns
	–2	0.49	6.65	0.03	0.98	0.32	6.78	6.64	2.95	3.02	8.45	8.31	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-131 • **1.5 V LVCMOS High Slew**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	8.36	0.04	1.44	0.43	6.82	8.36	3.39	2.77	9.06	10.60	ns
	–1	0.56	7.11	0.04	1.22	0.36	5.80	7.11	2.88	2.35	7.71	9.02	ns
	–2	0.49	6.24	0.03	1.07	0.32	5.10	6.24	2.53	2.06	6.76	7.91	ns
4 mA	Std.	0.66	5.31	0.04	1.44	0.43	4.85	5.31	3.74	3.40	7.09	7.55	ns
	–1	0.56	4.52	0.04	1.22	0.36	4.13	4.52	3.18	2.89	6.03	6.42	ns
	–2	0.49	3.97	0.03	1.07	0.32	3.62	3.97	2.79	2.54	5.29	5.64	ns
8 mA	Std.	0.66	4.67	0.04	1.44	0.43	4.55	4.67	3.82	3.56	6.78	6.90	ns
	–1	0.56	3.97	0.04	1.22	0.36	3.87	3.97	3.25	3.03	5.77	5.87	ns
	–2	0.49	3.49	0.03	1.07	0.32	3.40	3.49	2.85	2.66	5.07	5.16	ns
12 mA	Std.	0.66	4.08	0.04	1.44	0.43	4.15	3.58	3.94	4.20	6.39	5.81	ns
	–1	0.56	3.47	0.04	1.22	0.36	3.53	3.04	3.36	3.58	5.44	4.95	ns
	–2	0.49	3.05	0.03	1.07	0.32	3.10	2.67	2.95	3.14	4.77	4.34	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 3-10 • AFS250 Quiescent Supply Current Characteristics (continued)

Parameter	Description	Conditions	Temp.	Min	Typ	Max	Unit
IPP	Programming supply current	Non-programming mode, VPUMP = 3.63 V	T_J = 25°C		37	80	µA
			T_J = 85°C		37	80	µA
			T_J = 100°C		80	100	µA
		Standby mode[5] or Sleep mode[6], VPUMP = 0 V			0	0	µA
ICCNVM	Embedded NVM current	Reset asserted, VCCNVM = 1.575 V	T_J = 25°C		10	40	µA
			T_J = 85°C		14	40	µA
			T_J = 100°C		14	40	µA
ICCPLL	1.5 V PLL quiescent current	Operational standby, VCCPLL = 1.575 V	T_J = 25°C		65	100	µA
			T_J = 85°C		65	100	µA
			T_J = 100°C		65	100	µA

Notes:

1. *ICC is the 1.5 V power supplies, ICC, ICCPLL, ICC15A, ICCNVM.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, and ICCI2.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTA G = VPUMP = 0 V.*

FG484		
Pin Number	AFS600 Function	AFS1500 Function
H13	GND	GND
H14	VCCIB1	VCCIB1
H15	GND	GND
H16	GND	GND
H17	NC	IO53NDB2V0
H18	IO38PDB2V0	IO57PDB2V0
H19	GCA2/IO39PDB2V0	GCA2/IO59PDB2V0
H20	VCCIB2	VCCIB2
H21	IO37NDB2V0	IO54NDB2V0
H22	IO37PDB2V0	IO54PDB2V0
J1	NC	IO112PPB4V0
J2	IO76NDB4V0	IO113NDB4V0
J3	GFB2/IO74PDB4V0	GFB2/IO109PDB4V0
J4	GFA2/IO75PDB4V0	GFA2/IO110PDB4V0
J5	NC	IO112NPB4V0
J6	NC	IO104PDB4V0
J7	NC	IO111PDB4V0
J8	VCCIB4	VCCIB4
J9	GND	GND
J10	VCC	VCC
J11	GND	GND
J12	VCC	VCC
J13	GND	GND
J14	VCC	VCC
J15	VCCIB2	VCCIB2
J16	GCB2/IO40PDB2V0	GCB2/IO60PDB2V0
J17	NC	IO58NDB2V0
J18	IO38NDB2V0	IO57NDB2V0
J19	IO39NDB2V0	IO59NDB2V0
J20	GCC2/IO41PDB2V0	GCC2/IO61PDB2V0
J21	NC	IO55PSB2V0
J22	IO42PDB2V0	IO56PDB2V0
K1	GFC2/IO73PDB4V0	GFC2/IO108PDB4V0
K2	GND	GND
K3	IO74NDB4V0	IO109NDB4V0

FG484		
Pin Number	AFS600 Function	AFS1500 Function
K4	IO75NDB4V0	IO110NDB4V0
K5	GND	GND
K6	NC	IO104NDB4V0
K7	NC	IO111NDB4V0
K8	GND	GND
K9	VCC	VCC
K10	GND	GND
K11	VCC	VCC
K12	GND	GND
K13	VCC	VCC
K14	GND	GND
K15	GND	GND
K16	IO40NDB2V0	IO60NDB2V0
K17	NC	IO58PDB2V0
K18	GND	GND
K19	NC	IO68NPB2V0
K20	IO41NDB2V0	IO61NDB2V0
K21	GND	GND
K22	IO42NDB2V0	IO56NDB2V0
L1	IO73NDB4V0	IO108NDB4V0
L2	VCCOSC	VCCOSC
L3	VCCIB4	VCCIB4
L4	XTAL2	XTAL2
L5	GFC1/IO72PDB4V0	GFC1/IO107PDB4V0
L6	VCCIB4	VCCIB4
L7	GFB1/IO71PDB4V0	GFB1/IO106PDB4V0
L8	VCCIB4	VCCIB4
L9	GND	GND
L10	VCC	VCC
L11	GND	GND
L12	VCC	VCC
L13	GND	GND
L14	VCC	VCC
L15	VCCIB2	VCCIB2
L16	IO48PDB2V0	IO70PDB2V0

FG676	
Pin Number	AFS1500 Function
AD5	IO94NPB4V0
AD6	GND
AD7	VCC33N
AD8	AT0
AD9	ATRTN0
AD10	AT1
AD11	AT2
AD12	ATRTN1
AD13	AT3
AD14	AT6
AD15	ATRTN3
AD16	AT7
AD17	AT8
AD18	ATRTN4
AD19	AT9
AD20	VCC33A
AD21	GND
AD22	IO76NPB2V0
AD23	NC
AD24	GND
AD25	NC
AD26	NC
AE1	GND
AE2	GND
AE3	NC
AE4	NC
AE5	NC
AE6	NC
AE7	NC
AE8	NC
AE9	GNDA
AE10	NC
AE11	NC
AE12	GNDA
AE13	NC
AE14	NC

FG676	
Pin Number	AFS1500 Function
AE15	GNDA
AE16	NC
AE17	NC
AE18	GNDA
AE19	NC
AE20	NC
AE21	NC
AE22	NC
AE23	NC
AE24	NC
AE25	GND
AE26	GND
AF1	NC
AF2	GND
AF3	NC
AF4	NC
AF5	NC
AF6	NC
AF7	NC
AF8	NC
AF9	VCC33A
AF10	NC
AF11	NC
AF12	VCC33A
AF13	NC
AF14	NC
AF15	VCC33A
AF16	NC
AF17	NC
AF18	VCC33A
AF19	NC
AF20	NC
AF21	NC
AF22	NC
AF23	NC
AF24	NC

FG676	
Pin Number	AFS1500 Function
AF25	GND
AF26	NC
B1	GND
B2	GND
B3	NC
B4	NC
B5	NC
B6	VCCIB0
B7	NC
B8	NC
B9	VCCIB0
B10	IO15NDB0V2
B11	IO15PDB0V2
B12	VCCIB0
B13	IO19NDB0V2
B14	IO19PDB0V2
B15	VCCIB1
B16	IO25NDB1V0
B17	IO25PDB1V0
B18	VCCIB1
B19	IO33NDB1V1
B20	IO33PDB1V1
B21	VCCIB1
B22	NC
B23	NC
B24	NC
B25	GND
B26	GND
C1	NC
C2	NC
C3	GND
C4	NC
C5	GAA1/IO01PDB0V0
C6	GAB0/IO02NDB0V0
C7	GAB1/IO02PDB0V0
C8	IO07NDB0V1

Revision	Changes	Page
Advance v1.0 (continued)	This change table states that in the "208-Pin PQFP" table listed under the Advance v0.8 changes, the AFS090 device had a pin change. That is incorrect. Pin 102 was updated for AFS250 and AFS600. The function name changed from $V_{CC33ACAP}$ to V_{CC33A}.	3-8
Advance v0.9 (October 2007)	In the "Package I/Os: Single-/Double-Ended (Analog)" table, the AFS1500/M7AFS1500 I/O counts were updated for the following devices: FG484: 223/109 FG676: 252/126	II
	In the "108-Pin QFN" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pin: B25	3-2
	In the "180-Pin QFN" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS090: B29 AFS250: B29	3-4
	In the "208-Pin PQFP" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS090: 102 AFS250: 102	3-8
	In the "256-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS090: T14 AFS250: T14 AFS600: T14 AFS1500: T14	3-12
Advance v0.9 (continued)	In the "484-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS600: AB18 AFS1500: AB18	3-20
	In the "676-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS1500: AD20	3-28
Advance v0.8 (June 2007)	Figure 2-16 • Fusion Clocking Options and the "RC Oscillator" section were updated to change GND_OSC and VCC_OSC to GNDOSC and VCCOSC.	2-20, 2-21
	Figure 2-19 • Fusion CCC Options: Global Buffers with the PLL Macro was updated to change the positions of OADIVRST and OADIVHALF, and a note was added.	2-25
	The "Crystal Oscillator" section was updated to include information about controlling and enabling/disabling the crystal oscillator.	2-22
	Table 2-11 · Electrical Characteristics of the Crystal Oscillator was updated to change the typical value of $I_{DYNXTAL}$ for 0.032–0.2 MHz to 0.19.	2-24
	The "1.5 V Voltage Regulator" section was updated to add "or floating" in the paragraph stating that an external pull-down is required on TRST to power down the VR.	2-41
	The "1.5 V Voltage Regulator" section was updated to include information on powering down with the VR.	2-41