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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

E·XF

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	252
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs1500-1fgg676

Email: info@E-XFL.COM

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Fusion Device Family Overview

Instant On

Flash-based Fusion devices are Level 0 Instant On. Instant On Fusion devices greatly simplify total system design and reduce total system cost by eliminating the need for CPLDs. The Fusion Instant On clocking (PLLs) replaces off-chip clocking resources. The Fusion mix of Instant On clocking and analog resources makes these devices an excellent choice for both system supervisor and system management functions. Instant On from a single 3.3 V source enables Fusion devices to initiate, control, and monitor multiple voltage supplies while also providing system clocks. In addition, glitches and brownouts in system power will not corrupt the Fusion device flash configuration. Unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables reduction or complete removal of expensive voltage monitor and brownout detection devices from the PCB design.

Flash-based Fusion devices simplify total system design and reduce cost and design risk, while increasing system reliability.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. Another source of radiation-induced firm errors is alpha particles. For an alpha to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in Fusion flash-based FPGAs. Once it is programmed, the flash cell configuration element of Fusion FPGAs cannot be altered by high-energy neutrons and is therefore immune to errors from them.

Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based Fusion devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. With Fusion devices, there is no power-on current surge and no high current transition, both of which occur on many FPGAs.

Fusion devices also have low dynamic power consumption and support both low power standby mode and very low power sleep mode, offering further power savings.

Advanced Flash Technology

The Fusion family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows very high logic utilization (much higher than competing SRAM technologies) without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Routing Architecture

The routing structure of Fusion devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources; efficient long-line resources; high-speed very-long-line resources; and the high-performance VersaNet networks.

The ultra-fast local resources are dedicated lines that allow the output of each VersaTile to connect directly to every input of the eight surrounding VersaTiles (Figure 2-8). The exception to this is that the SET/CLR input of a VersaTile configured as a D-flip-flop is driven only by the VersaNet global network.

The efficient long-line resources provide routing for longer distances and higher-fanout connections. These resources vary in length (spanning one, two, or four VersaTiles), run both vertically and horizontally, and cover the entire Fusion device (Figure 2-9 on page 2-9). Each VersaTile can drive signals onto the efficient long-line resources, which can access every input of every VersaTile. Active buffers are inserted automatically by routing software to limit loading effects.

The high-speed very-long-line resources, which span the entire device with minimal delay, are used to route very long or high-fanout nets: length ± 12 VersaTiles in the vertical direction and length ± 16 in the horizontal direction from a given core VersaTile (Figure 2-10 on page 2-10). Very long lines in Fusion devices, like those in ProASIC3 devices, have been enhanced. This provides a significant performance boost for long-reach signals.

The high-performance VersaNet global networks are low-skew, high-fanout nets that are accessible from external pins or from internal logic (Figure 2-11 on page 2-11). These nets are typically used to distribute clocks, reset signals, and other high-fanout nets requiring minimum skew. The VersaNet networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically, with signals accessing every input on all VersaTiles.





Modes of Operation

Standby Mode

Standby mode allows periodic power-up and power-down of the FPGA fabric. In standby mode, the real-time counter and crystal block are ON. The FPGA is not powered by disabling the 1.5 V voltage regulator. The 1.5 V voltage regulator can be enabled when the preset count is matched. Refer to the "Real-Time Counter (part of AB macro)" section for details. To enter standby mode, the RTC must be first configured and enabled. Then VRPSM is shut off by deasserting the VRPU signal. The 1.5 V voltage regulator is then disabled, and shuts off the 1.5 V output.

Sleep Mode

In sleep mode, the real-time counter and crystal blocks are OFF. The 1.5 V voltage regulator inside the VRPSM can only be enabled by the PUB or TRST pin. Refer to the "Voltage Regulator and Power System Monitor (VRPSM)" section on page 2-36 for details on power-up and power-down of the 1.5 V voltage regulator.

Standby and Sleep Mode Circuit Implementation

For extra power savings, VJTAG and VPUMP should be at the same voltage as VCC, floated or ground, during standby and sleep modes. Note that when VJTAG is not powered, the 1.5 V voltage regulator cannot be enabled through TRST.

VPUMP and VJTAG can be controlled through an external switch. Microsemi recommends ADG839, ADG849, or ADG841 as possible switches. Figure 2-28 shows the implementation for controlling VPUMP. The IN signal of the switch can be connected to PTBASE of the Fusion device. VJTAG can be controlled in same manner.



Figure 2-28 • Implementation to Control VPUMP

The following signals are used to configure the RAM4K9 memory element.

WIDTHA and WIDTHB

These signals enable the RAM to be configured in one of four allowable aspect ratios (Table 2-27).

|--|

WIDTHA1, WIDTHA0	WIDTHB1, WIDTHB0	D×W				
00	00	4k×1				
01	01	2k×2				
10	10	1k×4				
11 11 512×9						
Note: The aspect ratio settings are constant and cannot be changed on the fly.						

BLKA and BLKB

These signals are active low and will enable the respective ports when asserted. When a BLKx signal is deasserted, the corresponding port's outputs hold the previous value.

WENA and WENB

These signals switch the RAM between read and write mode for the respective ports. A Low on these signals indicates a write operation, and a High indicates a read.

CLKA and CLKB

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

PIPEA and PIPEB

These signals are used to specify pipelined read on the output. A Low on PIPEA or PIPEB indicates a nonpipelined read, and the data appears on the corresponding output in the same clock cycle. A High indicates a pipelined, read and data appears on the corresponding output in the next clock cycle.

WMODEA and WMODEB

These signals are used to configure the behavior of the output when the RAM is in write mode. A Low on these signals makes the output retain data from the previous read. A High indicates pass-through behavior, wherein the data being written will appear immediately on the output. This signal is overridden when the RAM is being read.

RESET

This active low signal resets the output to zero, disables reads and writes from the SRAM block, and clears the data hold registers when asserted. It does not reset the contents of the memory.

ADDRA and ADDRB

These are used as read or write addresses, and they are 12 bits wide. When a depth of less than 4 k is specified, the unused high-order bits must be grounded (Table 2-28).

Table 2-28 • Address Pins Unused/Used for Various Supported Bus Widths

DxW	ADDRx						
	Unused	Used					
4k×1	None	[11:0]					
2k×2	[11]	[10:0]					
1k×4	[11:10]	[9:0]					
512×9	[11:9]	[8:0]					

Note: The "x" in ADDRx implies A or B.



SRAM Characteristics

Timing Waveforms







Figure 2-51 • RAM Read for Pipelined Output. Applicable to both RAM4K9 and RAM512x18.



Direct Digital Input

The AV, AC, and AT pads can also be configured as high-voltage digital inputs (Figure 2-69). As these pads are 12 V–tolerant, the digital input can also be up to 12 V. However, the frequency at which these pads can operate is limited to 10 MHz.

To enable one of these analog input pads to operate as a digital input, its corresponding Digital Input Enable (DENAxy) pin on the Analog Block must be pulled High, where x is either V, C, or T (for AV, AC, or AT pads, respectively) and y is in the range 0 to 9, corresponding to the appropriate Analog Quad.

When the pad is configured as a digital input, the signal will come out of the Analog Block macro on the appropriate DAxOUTy pin, where x represents the pad type (V for AV pad, C for AC pad, or T for AT pad) and y represents the appropriate Analog Quad number. Example: If the AT pad in Analog Quad 5 is configured as a digital input, it will come out on the DATOUT5 pin of the Analog Block macro.



Figure 2-69 • Analog Quad Direct Digital Input Configuration



Device Architecture

ADC Description

The Fusion ADC is a 12-bit SAR ADC. It offers a wide variety of features for different use models. Figure 2-80 shows a block diagram of the Fusion ADC.

- · Configurable resolution: 8-bit, 10-bit, and 12-bit mode
- DNL: 0.6 LSB for 10-bit mode
- INL: 0.4 LSB for 10-bit mode
- No missing code
- Internal VAREF = 2.56 V
- Maximum Sample Rate = 600 Ksps
- Power-up calibration and dynamic calibration after every sample to compensate for temperature drift over time



Figure 2-80 • ADC Simplified Block Diagram

ADC Theory of Operation

An analog-to-digital converter is used to capture discrete samples of a continuous analog voltage and provide a discrete binary representation of the signal. Analog-to-digital converters are generally characterized in three ways:

- Input voltage range
- Resolution
- Bandwidth or conversion rate

The input voltage range of an ADC is determined by its reference voltage (VREF). Fusion devices include an internal 2.56 V reference, or the user can supply an external reference of up to 3.3 V. The following examples use the internal 2.56 V reference, so the full-scale input range of the ADC is 0 to 2.56 V.

The resolution (LSB) of the ADC is a function of the number of binary bits in the converter. The ADC approximates the value of the input voltage using 2n steps, where n is the number of bits in the converter. Each step therefore represents VREF÷ 2n volts. In the case of the Fusion ADC configured for 12-bit operation, the LSB is 2.56 V / 4096 = 0.625 mV.

Finally, bandwidth is an indication of the maximum number of conversions the ADC can perform each second. The bandwidth of an ADC is constrained by its architecture and several key performance characteristics.



Device Architecture

Table 2-50 • ADC Characteristics in Direct Input Mode (continued)

Commercial Temperature Range Conditions, $T_J = 85^{\circ}C$ (unless noted otherwise), Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Тур.	Max.	Units
Dynamic Pe	erformance					
SNR	Signal-to-Noise Ratio	8-bit mode	48.0	49.5		dB
		10-bit mode	58.0	60.0		dB
		12-bit mode	62.9	64.5		dB
SINAD	Signal-to-Noise Distortion	8-bit mode	47.6	49.5		dB
		10-bit mode	57.4	59.8		dB
		12-bit mode	62.0	64.2		dB
THD	Total Harmonic Distortion	8-bit mode		-74.4	-63.0	dBc
		10-bit mode		-78.3	-63.0	dBc
		12-bit mode		-77.9	-64.4	dBc
ENOB	Effective Number of Bits	8-bit mode	7.6	7.9		bits
		10-bit mode	9.5	9.6		bits
		12-bit mode	10.0	10.4		bits
Conversion	Rate	ŀ				
	Conversion Time	8-bit mode	1.7			μs
		10-bit mode	1.8			μs
		12-bit mode	2			μs
	Sample Rate	8-bit mode			600	Ksps
		10-bit mode			550	Ksps
		12-bit mode			500	Ksps

Notes:

1. Accuracy of the external reference is 2.56 V \pm 4.6 mV.

2. Data is based on characterization.

3. The sample rate is time-shared among active analog inputs.

Features Supported on Pro I/Os

Table 2-72 lists all features supported by transmitter/receiver for single-ended and differential I/Os.

Table 2-72 • Fusion Pro I/O Features

Feature	Description
Single-ended and voltage- referenced transmitter	 Hot insertion in every mode except PCI or 5 V input tolerant (these modes use clamp diodes and do not allow hot insertion)
features	Activation of hot insertion (disabling the clamp diode) is selectable by I/Os.
	Weak pull-up and pull-down
	Two slew rates
	 Skew between output buffer enable/disable time: 2 ns delay (rising edge) and 0 ns delay (falling edge); see "Selectable Skew between Output Buffer Enable/Disable Time" on page 2-149 for more information
	Five drive strengths
	5 V-tolerant receiver ("5 V Input Tolerance" section on page 2-144)
	 LVTTL/LVCMOS 3.3 V outputs compatible with 5 V TTL inputs ("5 V Output Tolerance" section on page 2-148)
	High performance (Table 2-76 on page 2-143)
Single-ended receiver features	Schmitt trigger option
	ESD protection
	 Programmable delay: 0 ns if bypassed, 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V)
	High performance (Table 2-76 on page 2-143)
	 Separate ground planes, GND/GNDQ, for input buffers only to avoid output- induced noise in the input circuitry
Voltage-referenced differential receiver features	 Programmable Delay: 0 ns if bypassed, 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V)
	High performance (Table 2-76 on page 2-143)
	 Separate ground planes, GND/GNDQ, for input buffers only to avoid output- induced noise in the input circuitry
CMOS-style LVDS, BLVDS, M-LVDS, or LVPECL	 Two I/Os and external resistors are used to provide a CMOS-style LVDS, BLVDS, M-LVDS, or LVPECL transmitter solution.
transmitter	Activation of hot insertion (disabling the clamp diode) is selectable by I/Os.
	Weak pull-up and pull-down
	Fast slew rate
LVDS/LVPECL differential	ESD protection
receiver teatures	High performance (Table 2-76 on page 2-143)
	 Programmable delay: 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V)
	 Separate input buffer ground and power planes to avoid output-induced noise in the input circuitry





Figure 2-118 • Tristate Output Buffer Timing Model and Delays (example)

Timing Characteristics

Table 2-120 • 1.8 V LVCMOS Low Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V Applicable to Pro I/Os

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{zLS}	t _{zHS}	Units
2 mA	Std.	0.66	15.84	0.04	1.45	1.91	0.43	15.65	15.84	2.78	1.58	17.89	18.07	ns
	-1	0.56	13.47	0.04	1.23	1.62	0.36	13.31	13.47	2.37	1.35	15.22	15.37	ns
	-2	0.49	11.83	0.03	1.08	1.42	0.32	11.69	11.83	2.08	1.18	13.36	13.50	ns
4 mA	Std.	0.66	11.39	0.04	1.45	1.91	0.43	11.60	10.76	3.26	2.77	13.84	12.99	ns
	-1	0.56	9.69	0.04	1.23	1.62	0.36	9.87	9.15	2.77	2.36	11.77	11.05	ns
	-2	0.49	8.51	0.03	1.08	1.42	0.32	8.66	8.03	2.43	2.07	10.33	9.70	ns
8 mA	Std.	0.66	8.97	0.04	1.45	1.91	0.43	9.14	8.10	3.57	3.36	11.37	10.33	ns
	-1	0.56	7.63	0.04	1.23	1.62	0.36	7.77	6.89	3.04	2.86	9.67	8.79	ns
	-2	0.49	6.70	0.03	1.08	1.42	0.32	6.82	6.05	2.66	2.51	8.49	7.72	ns
12 mA	Std.	0.66	8.35	0.04	1.45	1.91	0.43	8.50	7.59	3.64	3.52	10.74	9.82	ns
	-1	0.56	7.10	0.04	1.23	1.62	0.36	7.23	6.45	3.10	3.00	9.14	8.35	ns
	-2	0.49	6.24	0.03	1.08	1.42	0.32	6.35	5.66	2.72	2.63	8.02	7.33	ns
16 mA	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	-1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	-2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



Device Architecture

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for generalpurpose 1.5 V applications. It uses a 1.5 V input buffer and push-pull output buffer.

1.5 V LVCMOS		VIL	VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
Applicable	to Pro I	/O Banks								1		
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	6	6	39	32	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	8	8	55	66	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12	55	66	10	10
Applicable	to Adva	inced I/O Ban	iks						-	-		
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	6	6	39	32	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	8	8	55	66	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12	55	66	10	10
Applicable	to Pro I	/O Banks	-		• •	• •		-	-	-	-	
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.



Figure 2-122 • AC Loading

Table 2-127 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C _{LOAD} (pF)		
0	1.5	0.75	-	35		

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.



I/O Register Specifications Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Figure 2-137 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset





connected to the internal core logic I/O tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

Figure 2-146 • Boundary Scan Chain in Fusion

Table 2-185 • Boundary Scan Opcodes

	Hex Opcode
EXTEST	00
HIGHZ	07
USERCODE	0E
SAMPLE/PRELOAD	01
IDCODE	0F
CLAMP	05
BYPASS	FF



Static Power Consumption of Various Internal Resources

Table 3-15 • Different Components Contributing to the Static Power Consumption in Fusion Devices

		Power		Device-Specific Static Contributions					
Parameter	Definition	Supply		AFS1500	AFS600	AFS250	AFS090	Units	
PDC1	Core static power contribution in operating mode	VCC	1.5 V	18	7.5	4.50	3.00	mW	
PDC2	Device static power contribution in standby mode	VCC33A	3.3 V	0.66				mW	
PDC3	Device static power contribution in sleep mode	VCC33A	3.3 V	0.03				mW	
PDC4	NVM static power contribution	VCC	1.5 V	1.19				mW	
PDC5	Analog Block static power contribution of ADC	VCC33A	3.3 V	8.25				mW	
PDC6	Analog Block static power contribution per Quad	VCC33A	3.3 V		3.	.3		mW	
PDC7	Static contribution per input pin – standard dependent contribution	VCCI	See Table 3-12 on page 3-18			3-18			
PDC8	Static contribution per input pin – standard dependent contribution	VCCI		See	Table 3-13	3 on page 3	3-20		
PDC9	Static contribution for PLL	VCC	1.5 V		2.	55		mW	

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- · The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- · The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- The number of NVM blocks used in the design
- The number of Analog Quads used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 3-16 on page 3-27.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 3-17 on page 3-27.
- Read rate and write rate to the RAM—guidelines are provided for typical applications in Table 3-17 on page 3-27.
- Read rate to the NVM blocks

The calculation should be repeated for each clock domain defined in the design.



PQ208



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/default.aspx.



Package Pin Assignments

PQ208			PQ208			
Pin Number	AFS250 Function	AFS600 Function	Pin Number	AFS250 Function	AFS600 Function	
147	GCC1/IO47PDB1V0	IO39NDB2V0	184	IO18RSB0V0	IO10PPB0V1	
148	IO42NDB1V0	GCA2/IO39PDB2V0	185	IO17RSB0V0	IO09PPB0V1	
149	GBC2/IO42PDB1V0	IO31NDB2V0	186	IO16RSB0V0	IO10NPB0V1	
150	VCCIB1	GBB2/IO31PDB2V0	187	IO15RSB0V0	IO09NPB0V1	
151	GND	IO30NDB2V0	188	VCCIB0	IO08PPB0V1	
152	VCC	GBA2/IO30PDB2V0	189	GND	IO07PPB0V1	
153	IO41NDB1V0	VCCIB2	190	VCC	IO08NPB0V1	
154	GBB2/IO41PDB1V0	GNDQ	191	IO14RSB0V0	IO07NPB0V1	
155	IO40NDB1V0	VCOMPLB	192	IO13RSB0V0	IO06PPB0V0	
156	GBA2/IO40PDB1V0	VCCPLB	193	IO12RSB0V0	IO05PPB0V0	
157	GBA1/IO39RSB0V0	VCCIB1	194	IO11RSB0V0	IO06NPB0V0	
158	GBA0/IO38RSB0V0	GNDQ	195	IO10RSB0V0	IO04PPB0V0	
159	GBB1/IO37RSB0V0	GBB1/IO27PPB1V1	196	IO09RSB0V0	IO05NPB0V0	
160	GBB0/IO36RSB0V0	GBA1/IO28PPB1V1	197	IO08RSB0V0	IO04NPB0V0	
161	GBC1/IO35RSB0V0	GBB0/IO27NPB1V1	198	IO07RSB0V0	GAC1/IO03PDB0V0	
162	VCCIB0	GBA0/IO28NPB1V1	199	IO06RSB0V0	GAC0/IO03NDB0V0	
163	GND	VCCIB1	200	GAC1/IO05RSB0V0	VCCIB0	
164	VCC	GND	201	VCCIB0	GND	
165	GBC0/IO34RSB0V0	VCC	202	GND	VCC	
166	IO33RSB0V0	GBC1/IO26PDB1V1	203	VCC	GAB1/IO02PDB0V0	
167	IO32RSB0V0	GBC0/IO26NDB1V1	204	GAC0/IO04RSB0V0	GAB0/IO02NDB0V0	
168	IO31RSB0V0	IO24PPB1V1	205	GAB1/IO03RSB0V0	GAA1/IO01PDB0V0	
169	IO30RSB0V0	IO23PPB1V1	206	GAB0/IO02RSB0V0	GAA0/IO01NDB0V0	
170	IO29RSB0V0	IO24NPB1V1	207	GAA1/IO01RSB0V0	GNDQ	
171	IO28RSB0V0	IO23NPB1V1	208	GAA0/IO00RSB0V0	VCCIB0	
172	IO27RSB0V0	IO22PPB1V0				
173	IO26RSB0V0	IO21PPB1V0				
174	IO25RSB0V0	IO22NPB1V0				
175	VCCIB0	IO21NPB1V0				
176	GND	IO20PSB1V0				
177	VCC	IO19PSB1V0				
178	IO24RSB0V0	IO14NSB0V1				
179	IO23RSB0V0	IO12PDB0V1				
180	IO22RSB0V0	IO12NDB0V1				
181	IO21RSB0V0	VCCIB0				
182	IO20RSB0V0	GND				
183	IO19RSB0V0	VCC				

FG256					
Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function	
A1	GND	GND	GND	GND	
A2	VCCIB0	VCCIB0	VCCIB0	VCCIB0	
A3	GAB0/IO02RSB0V0	GAA0/IO00RSB0V0	GAA0/IO01NDB0V0	GAA0/IO01NDB0V0	
A4	GAB1/IO03RSB0V0	GAA1/IO01RSB0V0	GAA1/IO01PDB0V0	GAA1/IO01PDB0V0	
A5	GND	GND	GND	GND	
A6	IO07RSB0V0	IO11RSB0V0	IO10PDB0V1	IO07PDB0V1	
A7	IO10RSB0V0	IO14RSB0V0	IO12PDB0V1	IO13PDB0V2	
A8	IO11RSB0V0	IO15RSB0V0	IO12NDB0V1	IO13NDB0V2	
A9	IO16RSB0V0	IO24RSB0V0	IO22NDB1V0	IO24NDB1V0	
A10	IO17RSB0V0	IO25RSB0V0	IO22PDB1V0	IO24PDB1V0	
A11	IO18RSB0V0	IO26RSB0V0	IO24NDB1V1	IO29NDB1V1	
A12	GND	GND	GND	GND	
A13	GBC0/IO25RSB0V0	GBA0/IO38RSB0V0	GBA0/IO28NDB1V1	GBA0/IO42NDB1V2	
A14	GBA0/IO29RSB0V0	IO32RSB0V0	IO29NDB1V1	IO43NDB1V2	
A15	VCCIB0	VCCIB0	VCCIB1	VCCIB1	
A16	GND	GND	GND	GND	
B1	VCOMPLA	VCOMPLA	VCOMPLA	VCOMPLA	
B2	VCCPLA	VCCPLA	VCCPLA	VCCPLA	
B3	GAA0/IO00RSB0V0	IO07RSB0V0	IO00NDB0V0	IO00NDB0V0	
B4	GAA1/IO01RSB0V0	IO06RSB0V0	IO00PDB0V0	IO00PDB0V0	
B5	NC	GAB1/IO03RSB0V0	GAB1/IO02PPB0V0	GAB1/IO02PPB0V0	
B6	IO06RSB0V0	IO10RSB0V0	IO10NDB0V1	IO07NDB0V1	
B7	VCCIB0	VCCIB0	VCCIB0	VCCIB0	
B8	IO12RSB0V0	IO16RSB0V0	IO18NDB1V0	IO22NDB1V0	
В9	IO13RSB0V0	IO17RSB0V0	IO18PDB1V0	IO22PDB1V0	
B10	VCCIB0	VCCIB0	VCCIB1	VCCIB1	
B11	IO19RSB0V0	IO27RSB0V0	IO24PDB1V1	IO29PDB1V1	
B12	GBB0/IO27RSB0V0	GBC0/IO34RSB0V0	GBC0/IO26NPB1V1	GBC0/IO40NPB1V2	
B13	GBC1/IO26RSB0V0	GBA1/IO39RSB0V0	GBA1/IO28PDB1V1	GBA1/IO42PDB1V2	
B14	GBA1/IO30RSB0V0	IO33RSB0V0	IO29PDB1V1	IO43PDB1V2	
B15	NC	NC	VCCPLB	VCCPLB	
B16	NC	NC	VCOMPLB	VCOMPLB	
C1	VCCIB3	VCCIB3	VCCIB4	VCCIB4	
C2	GND	GND	GND	GND	
C3	VCCIB3	VCCIB3	VCCIB4	VCCIB4	
C4	NC	NC	VCCIB0	VCCIB0	
C5	VCCIB0	VCCIB0	VCCIB0	VCCIB0	
C6	GAC1/IO05RSB0V0	GAC1/IO05RSB0V0	GAC1/IO03PDB0V0	GAC1/IO03PDB0V0	



Package Pin Assignments

FG484		FG484			
Pin Number	AFS600 Function	AFS1500 Function	Pin Number	AFS600 Function	AFS1500 Function
E9	NC	IO08PDB0V1	F22	IO35PDB2V0	IO51PDB2V0
E10	GND	GND	G1	IO77PDB4V0	IO115PDB4V0
E11	IO15NDB1V0	IO22NDB1V0	G2	GND	GND
E12	IO15PDB1V0	IO22PDB1V0	G3	IO78NDB4V0	IO116NDB4V0
E13	GND	GND	G4	IO78PDB4V0	IO116PDB4V0
E14	NC	IO32PPB1V1	G5	VCCIB4	VCCIB4
E15	NC	IO36NPB1V2	G6	NC	IO117PDB4V0
E16	VCCIB1	VCCIB1	G7	VCCIB4	VCCIB4
E17	GND	GND	G8	GND	GND
E18	NC	IO47NPB2V0	G9	IO04NDB0V0	IO06NDB0V1
E19	IO33PDB2V0	IO49PDB2V0	G10	IO04PDB0V0	IO06PDB0V1
E20	VCCIB2	VCCIB2	G11	IO12NDB0V1	IO16NDB0V2
E21	IO32NDB2V0	IO46NDB2V0	G12	IO12PDB0V1	IO16PDB0V2
E22	GBC2/IO32PDB2V0	GBC2/IO46PDB2V0	G13	NC	IO28NDB1V1
F1	IO80NDB4V0	IO118NDB4V0	G14	NC	IO28PDB1V1
F2	IO80PDB4V0	IO118PDB4V0	G15	GND	GND
F3	NC	IO119NSB4V0	G16	NC	IO38PPB1V2
F4	IO84NDB4V0	IO124NDB4V0	G17	NC	IO53PDB2V0
F5	GND	GND	G18	VCCIB2	VCCIB2
F6	VCOMPLA	VCOMPLA	G19	IO36PDB2V0	IO52PDB2V0
F7	VCCPLA	VCCPLA	G20	IO36NDB2V0	IO52NDB2V0
F8	VCCIB0	VCCIB0	G21	GND	GND
F9	IO08NDB0V1	IO12NDB0V1	G22	IO35NDB2V0	IO51NDB2V0
F10	IO08PDB0V1	IO12PDB0V1	H1	IO77NDB4V0	IO115NDB4V0
F11	VCCIB0	VCCIB0	H2	IO76PDB4V0	IO113PDB4V0
F12	VCCIB1	VCCIB1	H3	VCCIB4	VCCIB4
F13	IO22NDB1V0	IO30NDB1V1	H4	IO79NDB4V0	IO114NDB4V0
F14	IO22PDB1V0	IO30PDB1V1	H5	IO79PDB4V0	IO114PDB4V0
F15	VCCIB1	VCCIB1	H6	NC	IO117NDB4V0
F16	NC	IO36PPB1V2	H7	GND	GND
F17	NC	IO38NPB1V2	H8	VCC	VCC
F18	GND	GND	H9	VCCIB0	VCCIB0
F19	IO33NDB2V0	IO49NDB2V0	H10	GND	GND
F20	IO34PDB2V0	IO50PDB2V0	H11	VCCIB0	VCCIB0
F21	IO34NDB2V0	IO50NDB2V0	H12	VCCIB1	VCCIB1

Microsemi

Package Pin Assignments

FG676		FG676		FG676	
Pin Number	AFS1500 Function	Pin Number	AFS1500 Function	Pin Number	AFS1500 Function
A1	NC	AA11	AV2	AB21	PTBASE
A2	GND	AA12	GNDA	AB22	GNDNVM
A3	NC	AA13	AV3	AB23	VCCNVM
A4	NC	AA14	AV6	AB24	VPUMP
A5	GND	AA15	GNDA	AB25	NC
A6	NC	AA16	AV7	AB26	GND
A7	NC	AA17	AV8	AC1	NC
A8	GND	AA18	GNDA	AC2	NC
A9	IO17NDB0V2	AA19	AV9	AC3	NC
A10	IO17PDB0V2	AA20	VCCIB2	AC4	GND
A11	GND	AA21	IO68PPB2V0	AC5	VCCIB4
A12	IO18NDB0V2	AA22	ТСК	AC6	VCCIB4
A13	IO18PDB0V2	AA23	GND	AC7	PCAP
A14	IO20NDB0V2	AA24	IO76PPB2V0	AC8	AG0
A15	IO20PDB0V2	AA25	VCCIB2	AC9	GNDA
A16	GND	AA26	NC	AC10	AG1
A17	IO21PDB0V2	AB1	GND	AC11	AG2
A18	IO21NDB0V2	AB2	NC	AC12	GNDA
A19	GND	AB3	GEC2/IO87PDB4V0	AC13	AG3
A20	IO39NDB1V2	AB4	IO87NDB4V0	AC14	AG6
A21	IO39PDB1V2	AB5	GEA2/IO85PDB4V0	AC15	GNDA
A22	GND	AB6	IO85NDB4V0	AC16	AG7
A23	NC	AB7	NCAP	AC17	AG8
A24	NC	AB8	AC0	AC18	GNDA
A25	GND	AB9	VCC33A	AC19	AG9
A26	NC	AB10	AC1	AC20	VAREF
AA1	NC	AB11	AC2	AC21	VCCIB2
AA2	VCCIB4	AB12	VCC33A	AC22	PTEM
AA3	IO93PDB4V0	AB13	AC3	AC23	GND
AA4	GND	AB14	AC6	AC24	NC
AA5	IO93NDB4V0	AB15	VCC33A	AC25	NC
AA6	GEB2/IO86PDB4V0	AB16	AC7	AC26	NC
AA7	IO86NDB4V0	AB17	AC8	AD1	NC
AA8	AV0	AB18	VCC33A	AD2	NC
AA9	GNDA	AB19	AC9	AD3	GND
AA10	AV1	AB20	ADCGNDREF	AD4	NC