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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

E·XFI

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	119
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs1500-2fg256

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Fusion Device Family Overview

Instant On

Flash-based Fusion devices are Level 0 Instant On. Instant On Fusion devices greatly simplify total system design and reduce total system cost by eliminating the need for CPLDs. The Fusion Instant On clocking (PLLs) replaces off-chip clocking resources. The Fusion mix of Instant On clocking and analog resources makes these devices an excellent choice for both system supervisor and system management functions. Instant On from a single 3.3 V source enables Fusion devices to initiate, control, and monitor multiple voltage supplies while also providing system clocks. In addition, glitches and brownouts in system power will not corrupt the Fusion device flash configuration. Unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables reduction or complete removal of expensive voltage monitor and brownout detection devices from the PCB design.

Flash-based Fusion devices simplify total system design and reduce cost and design risk, while increasing system reliability.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. Another source of radiation-induced firm errors is alpha particles. For an alpha to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in Fusion flash-based FPGAs. Once it is programmed, the flash cell configuration element of Fusion FPGAs cannot be altered by high-energy neutrons and is therefore immune to errors from them.

Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based Fusion devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. With Fusion devices, there is no power-on current surge and no high current transition, both of which occur on many FPGAs.

Fusion devices also have low dynamic power consumption and support both low power standby mode and very low power sleep mode, offering further power savings.

Advanced Flash Technology

The Fusion family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows very high logic utilization (much higher than competing SRAM technologies) without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Routing Architecture

The routing structure of Fusion devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources; efficient long-line resources; high-speed very-long-line resources; and the high-performance VersaNet networks.

The ultra-fast local resources are dedicated lines that allow the output of each VersaTile to connect directly to every input of the eight surrounding VersaTiles (Figure 2-8). The exception to this is that the SET/CLR input of a VersaTile configured as a D-flip-flop is driven only by the VersaNet global network.

The efficient long-line resources provide routing for longer distances and higher-fanout connections. These resources vary in length (spanning one, two, or four VersaTiles), run both vertically and horizontally, and cover the entire Fusion device (Figure 2-9 on page 2-9). Each VersaTile can drive signals onto the efficient long-line resources, which can access every input of every VersaTile. Active buffers are inserted automatically by routing software to limit loading effects.

The high-speed very-long-line resources, which span the entire device with minimal delay, are used to route very long or high-fanout nets: length ± 12 VersaTiles in the vertical direction and length ± 16 in the horizontal direction from a given core VersaTile (Figure 2-10 on page 2-10). Very long lines in Fusion devices, like those in ProASIC3 devices, have been enhanced. This provides a significant performance boost for long-reach signals.

The high-performance VersaNet global networks are low-skew, high-fanout nets that are accessible from external pins or from internal logic (Figure 2-11 on page 2-11). These nets are typically used to distribute clocks, reset signals, and other high-fanout nets requiring minimum skew. The VersaNet networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically, with signals accessing every input on all VersaTiles.







Device Architecture

Table 2-7 • AFS250 Global Resource Timing
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Paramotor	Description		·2	-	-1	St	Units	
Faranieter			Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	0.89	1.12	1.02	1.27	1.20	1.50	ns
t _{RCKH}	Input High Delay for Global Clock	0.88	1.14	1.00	1.30	1.17	1.53	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock							ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock							ns
t _{RCKSW}	Maximum Skew for Global Clock		0.26		0.30		0.35	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-8 • AFS090 Global Resource Timing

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description		2	-	1	S	Unite	
Falailletei			Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	0.84	1.07	0.96	1.21	1.13	1.43	ns
t _{RCKH}	Input High Delay for Global Clock	0.83	1.10	0.95	1.25	1.12	1.47	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock							ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock							ns
t _{RCKSW}	Maximum Skew for Global Clock		0.27		0.30		0.36	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



RC Oscillator

The RC oscillator is an on-chip free-running clock source generating a 100 MHz clock. It can be used as a source clock for both on-chip and off-chip resources. When used in conjunction with the Fusion PLL and CCC circuits, the RC oscillator clock source can be used to generate clocks of varying frequency and phase.

The Fusion RC oscillator is very accurate at $\pm 1\%$ over commercial temperature ranges and and $\pm 3\%$ over industrial temperature ranges. It is an automated clock, requiring no setup or configuration by the user. It requires only that the power and GNDOSC pins be connected; no external components are required. The RC oscillator can be used to drive either a PLL or another internal signal.

RC Oscillator Characteristics

Parameter	Description	Conditions	Min.	Тур.	Max.	Units
Fac	Operating Frequency			100		MHz
	Accuracy	Temperature: 0°C to 85°C Voltage: 3.3 V ± 5%		1		%
		Temperature: -40° C to 125° C Voltage: 3.3 V ± 5%		3		%
	Output Jitter	Period Jitter (at 5 k cycles)		100		ps
NO		Cycle–Cycle Jitter (at 5 k cycles)		100		ps
		Period Jitter (at 5 k cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps
		Cycle–Cycle Jitter (at 5 k cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps
	Output Duty Cycle			50		%
IDYNRC	Operating Current			1		mA

Table 2-9 • Electrical Characteristics of RC Oscillator



Embedded Memories

Fusion devices include four types of embedded memory: flash block, FlashROM, SRAM, and FIFO.

Flash Memory Block

Fusion is the first FPGA that offers a flash memory block (FB). Each FB block stores 2 Mbits of data. The flash memory block macro is illustrated in Figure 2-32. The port pin name and descriptions are detailed on Table 2-19 on page 2-40. All flash memory block signals are active high, except for CLK and active low RESET. All flash memory operations are synchronous to the rising edge of CLK.



Figure 2-32 • Flash Memory Block

Flash Memory Block Characteristics



Figure 2-44 • Reset Timing Diagram

Table 2-25 • Flash Memory Block TimingCommercial Temperature Range Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
	Clock-to-Q in 5-cycle read mode of the Read Data	7.99	9.10	10.70	ns
^t CLK2RD	Clock-to-Q in 6-cycle read mode of the Read Data	5.03	5.73	6.74	ns
	Clock-to-Q in 5-cycle read mode of BUSY	4.95	5.63	6.62	ns
^I CLK2BUSY	Clock-to-Q in 6-cycle read mode of BUSY	4.45	5.07	5.96	ns
	Clock-to-Status in 5-cycle read mode	11.24	12.81	15.06	ns
^I CLK2STATUS	Clock-to-Status in 6-cycle read mode	4.48	5.10	6.00	ns
t _{DSUNVM}	Data Input Setup time for the Control Logic	1.92	2.19	2.57	ns
t _{DHNVM}	Data Input Hold time for the Control Logic	0.00	0.00	0.00	ns
t _{ASUNVM}	Address Input Setup time for the Control Logic	2.76	3.14	3.69	ns
t _{AHNVM}	Address Input Hold time for the Control Logic	0.00	0.00	0.00	ns
t _{SUDWNVM}	Data Width Setup time for the Control Logic	1.85	2.11	2.48	ns
t _{HDDWNVM}	Data Width Hold time for the Control Logic	0.00	0.00	0.00	ns
t _{SURENNVM}	Read Enable Setup time for the Control Logic	3.85	4.39	5.16	ns
t _{HDRENNVM}	Read Enable Hold Time for the Control Logic				ns
t _{SUWENNVM}	Write Enable Setup time for the Control Logic	2.37	2.69	3.17	ns
t _{HDWENNVM}	Write Enable Hold Time for the Control Logic	0.00	0.00	0.00	ns
t _{SUPROGNVM}	Program Setup time for the Control Logic	2.16	2.46	2.89	ns
t _{HDPROGNVM}	Program Hold time for the Control Logic	0.00	0.00	0.00	ns
t _{SUSPAREPAGE}	SparePage Setup time for the Control Logic	3.74	4.26	5.01	ns
t _{HDSPAREPAGE}	SparePage Hold time for the Control Logic	0.00	0.00	0.00	ns
t _{SUAUXBLK}	Auxiliary Block Setup Time for the Control Logic	3.74	4.26	5.00	ns
t _{HDAUXBLK}	Auxiliary Block Hold Time for the Control Logic	0.00	0.00	0.00	ns
t _{SURDNEXT}	ReadNext Setup Time for the Control Logic	2.17	2.47	2.90	ns
t _{HDRDNEXT}	ReadNext Hold Time for the Control Logic	0.00	0.00	0.00	ns
t _{SUERASEPG}	Erase Page Setup Time for the Control Logic	3.76	4.28	5.03	ns
t _{HDERASEPG}	Erase Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
t _{SUUNPROTECTPG}	Unprotect Page Setup Time for the Control Logic	2.01	2.29	2.69	ns
t _{HDUNPROTECTPG}	Unprotect Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
t _{SUDISCARDPG}	Discard Page Setup Time for the Control Logic	1.88	2.14	2.52	ns
t _{HDDISCARDPG}	Discard Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
t _{SUOVERWRPRO}	Overwrite Protect Setup Time for the Control Logic	1.64	1.86	2.19	ns
t _{HDOVERWRPRO}	Overwrite Protect Hold Time for the Control Logic	0.00	0.00	0.00	ns



RAM4K9 Description



Figure 2-48 • RAM4K9

TUE – Total Unadjusted Error

TUE is a comprehensive specification that includes linearity errors, gain error, and offset error. It is the worst-case deviation from the ideal device performance. TUE is a static specification (Figure 2-87).



Figure 2-87 • Total Unadjusted Error (TUE)

ADC Operation

Once the ADC has powered up and been released from reset, ADCRESET, the ADC will initiate a calibration routine designed to provide optimal ADC performance. The Fusion ADC offers a robust calibration scheme to reduce integrated offset and linearity errors. The offset and linearity errors of the main capacitor array are compensated for with an 8-bit calibration capacitor array. The offset/linearity error calibration is carried out in two ways. First, a power-up calibration is carried out when the ADC comes out of reset. This is initiated by the CALIBRATE output of the Analog Block macro and is a fixed number of ADC_CLK cycles (3,840 cycles), as shown in Figure 2-89 on page 2-111. In this mode, the linearity and offset errors of the capacitors are calibrated.

To further compensate for drift and temperature-dependent effects, every conversion is followed by postcalibration of either the offset or a bit of the main capacitor array. The post-calibration ensures that, over time and with temperature, the ADC remains consistent.

After both calibration and the setting of the appropriate configurations, as explained above, the ADC is ready for operation. Setting the ADCSTART signal high for one clock period will initiate the sample and conversion of the analog signal on the channel as configured by CHNUMBER[4:0]. The status signals SAMPLE and BUSY will show when the ADC is sampling and converting (Figure 2-91 on page 2-112). Both SAMPLE and BUSY will initially go high. After the ADC has sampled and held the analog signal, SAMPLE will go low. After the entire operation has completed and the analog signal is converted, BUSY will go low and DATAVALID will go high. This indicates that the digital result is available on the RESULT[11:0] pins.

DATAVALID will remain high until a subsequent ADCSTART is issued. The DATAVALID goes low on the rising edge of SYSCLK as shown in Figure 2-90 on page 2-112. The RESULT signals will be kept constant until the ADC finishes the subsequent sample. The next sampled RESULT will be available when DATAVALID goes high again. It is ideal to read the RESULT when DATAVALID is '1'. The RESULT is latched and remains unchanged until the next DATAVLAID rising edge.

	Calib	Direct ADC ^{2,3} (%FSR)						
Input Voltage (V)	16 V (AT)	16 V (12 V) (AV/AC)	8 V (AV/AC)	4 V (AT)	4 V (AV/AC)	2 V (AV/AC)	1 V (AV/AC)	VAREF = 2.56 V
15	1							
14	1							
12	1	1						
5	2	2	1					
3.3	2	2	1	1	1			
2.5	3	2	1	1	1			1
1.8	4	4	1	1	1	1		1
1.5	5	5	2	2	2	1		1
1.2	7	6	2	2	2	1		1
0.9	9	9	4	3	3	1	1	1

Table 2-53 • Analog Channel Accuracy: Monitoring Standard Positive Voltages Typical Conditions, T_A = 25°C

Notes:

1. Requires enabling Analog Calibration using SmartGen Analog System Builder. For further details, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the Fusion FPGA Fabric User Guide.

2. Direct ADC mode using an external VAREF of 2.56V±4.6mV, without Analog Calibration macro.

3. For input greater than 2.56 V, the ADC output will saturate. A higher VAREF or prescaler usage is recommended.

Examples

Calculating Accuracy for an Uncalibrated Analog Channel

Formula

For a given prescaler range, EQ 30 gives the output voltage.

Output Voltage = (Channel Output Offset in V) + (Input Voltage x Channel Gain)

EQ 30

where

Channel Output offset in V = Channel Input offset in LSBs x Equivalent voltage per LSB Channel Gain Factor = 1 + (% Channel Gain / 100)

Example

Input Voltage = 5 V Chosen Prescaler range = 8 V range Refer to Table 2-51 on page 2-122.

Max. Output Voltage = (Max Positive input offset) + (Input Voltage x Max Positive Channel Gain)

Max. Positive input offset = (21 LSB) x (8 mV per LSB in 10-bit mode) Max. Positive input offset = 166 mV Max. Positive Gain Error = +3% Max. Positive Channel Gain = 1 + (+3% / 100) Max. Positive Channel Gain = 1.03 Max. Output Voltage = (166 mV) + (5 V x 1.03) Max. Output Voltage = **5.316 V**



Figure 2-102 • DDR Output Support in Fusion Devices

Solution 3

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-4 on page 3-4. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCIX configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the bus switch, as shown in Figure 2-105. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.





Solution 4



Figure 2-106 • Solution 4





Figure 2-114 • Naming Conventions of Fusion Devices with Four I/O Banks





Figure 2-116 • Input Buffer Timing Model and Delays (example)

Fusion Family of Mixed Signal FPGAs

Table 2-98 • I/O Short Currents IOSH/IOSL

	Drive Strength	IOSH (mA)*	IOSL (mA)*
Applicable to Pro I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
Applicable to Advanced I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181

Note: $^{*}T_{J} = 100^{\circ}C$

Table 2-99 • Short Current Event Duration before Failure

Temperature	Time Before Failure
-40°C	>20 years
0°C	>20 years
25°C	>20 years
70°C	5 years
85°C	2 years
100°C	6 months

Table 2-100 • Schmitt Trigger Input Hysteresis Hysteresis Voltage Value (typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

Table 2-101 • I/O Input Rise Time, Fall Time, and Related I/O Reliability

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns*	20 years (100°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis	20 years (100°C)
HSTL/SSTL/GTL	No requirement	10 ns*	10 years (100°C)
LVDS/BLVDS/M-LVDS/LVPECL	No requirement	10 ns*	10 years (100°C)

Note: * The maximum input rise/fall time is related only to the noise induced into the input buffer trace. If the noise is low, the rise time and fall time of input buffers, when Schmitt trigger is disabled, can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure there is no excessive noise coupling into input signals.

2.5 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-147 • Minimum and Maximum DC Input and Output Levels

2.5 V GTL+		VIL	VIH		VOL	VOH	IOL	ЮН	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
33 mA	-0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	-	33	33	124	169	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.



Figure 2-127 • AC Loading

Table 2-148 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

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Table 2-149 • 2.5 V GTL+
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Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.0 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.66	2.21	0.04	1.51	0.43	2.25	2.10			4.48	4.34	ns
-1	0.56	1.88	0.04	1.29	0.36	1.91	1.79			3.81	3.69	ns
-2	0.49	1.65	0.03	1.13	0.32	1.68	1.57			3.35	4.34	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



Device Architecture

IEEE 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/Os" section on page 2-132 for more details.

Timing Characteristics

Table 2-186 • JTAG 1532

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{DISU}	Test Data Input Setup Time	0.50	0.57	0.67	ns
t _{DIHD}	Test Data Input Hold Time	1.00	1.13	1.33	ns
t _{TMSSU}	Test Mode Select Setup Time	0.50	0.57	0.67	ns
t _{TMDHD}	Test Mode Select Hold Time	1.00	1.13	1.33	ns
t _{TCK2Q}	Clock to Q (data out)	6.00	6.80	8.00	ns
t _{RSTB2Q}	Reset to Q (data out)	20.00	22.67	26.67	ns
F _{TCKMAX}	TCK Maximum Frequency	25.00	22.00	19.00	MHz
t _{TRSTREM}	ResetB Removal Time	0.00	0.00	0.00	ns
t _{TRSTREC}	ResetB Recovery Time	0.20	0.23	0.27	ns
t _{TRSTMPW}	ResetB Minimum Pulse	TBD	TBD	TBD	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



Table 3-13 • Summary of I/O Output Buffer Power (per pin)—Default I/O Software Settings¹ (continued)

	C _{LOAD} (pF)	VCCI (V)	Static Power PDC8 (mW) ²	Dynamic Power PAC10 (µW/MHz) ³				
Differential								
LVDS	-	2.5	7.74	88.92				
LVPECL	_	3.3	19.54	166.52				
Applicable to Standard I/O Banks								
Single-Ended								
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	-	431.08				
2.5 V LVCMOS	35	2.5	-	247.36				
1.8 V LVCMOS	35	1.8	-	128.46				
1.5 V LVCMOS (JESD8-11)	35	1.5	-	89.46				

Notes:

1. Dynamic power consumption is given for standard load and software-default drive strength and output slew.

2. PDC8 is the static power (where applicable) measured on VCCI.

3. PAC10 is the total dynamic power measured on VCC and VCCI.

PLL/CCC Contribution—P_{PLL}

PLL is not used in this application.

 $P_{PLL} = 0 W$

Nonvolatile Memory—P_{NVM}

Nonvolatile memory is not used in this application.

 $P_{NVM} = 0 W$

Crystal Oscillator—P_{XTL-OSC}

The application utilizes standby mode. The crystal oscillator is assumed to be active.

Operating Mode

P_{XTL-OSC} = PAC18

 $P_{XTL-OSC} = 0.63 \text{ mW}$

Standby Mode

P_{XTL-OSC} = PAC18

P_{XTL-OSC} = 0.63 mW

Sleep Mode

 $P_{XTL-OSC} = 0 W$

RC Oscillator—P_{RC-OSC}

Operating Mode

P_{RC-OSC} = PAC19

 $P_{RC-OSC} = 3.30 \text{ mW}$

Standby Mode and Sleep Mode

 $P_{RC-OSC} = 0 W$

Analog System—P_{AB}

Number of Quads used: N_{QUADS} = 4

Operating Mode

P_{AB} = PAC20

 P_{AB} = 3.00 mW

Standby Mode and Sleep Mode

 $P_{AB} = 0 W$

Total Dynamic Power Consumption—P_{DYN}

Operating Mode

P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM}+ P_{XTL-OSC} + P_{RC-OSC} + P_{AB} P_{DYN} = 41.28 mW + 21.1 mW + 4.35 mW + 19.25 mW + 1.30 mW + 47.47 mW + 1.38 mW + 0 + 0 + 0 + 0.63 mW + 3.30 mW + 3.00 mW

P_{DYN} = 143.06 mW

Standby Mode

 $P_{DYN} = P_{XTL-OSC}$ $P_{DYN} = 0.63 \text{ mW}$

Sleep Mode

 $P_{DYN} = 0 W$



FG256



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/default.aspx.