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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	119
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs1500-2fg256i

Advanced Architecture

The proprietary Fusion architecture provides granularity comparable to standard-cell ASICs. The Fusion device consists of several distinct and programmable architectural features, including the following (Figure 1-1 on page 1-5):

- Embedded memories
 - Flash memory blocks
 - FlashROM
 - SRAM and FIFO
- Clocking resources
 - PLL and CCC
 - RC oscillator
 - Crystal oscillator
 - No-Glitch MUX (NGMUX)
- Digital I/Os with advanced I/O standards
- FPGA VersaTiles
- Analog components
 - ADC
 - Analog I/Os supporting voltage, current, and temperature monitoring
 - 1.5 V on-board voltage regulator
 - Real-time counter

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic lookup table (LUT) equivalent or a D-flip-flop or latch (with or without enable) by programming the appropriate flash switch interconnections. This versatility allows efficient use of the FPGA fabric. The VersaTile capability is unique to the Microsemi families of flash-based FPGAs. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid (3.3 V) single-voltage programming of Fusion devices via an IEEE 1532 JTAG interface.

Unprecedented Integration

Integrated Analog Blocks and Analog I/Os

Fusion devices offer robust and flexible analog mixed signal capability in addition to the high-performance flash FPGA fabric and flash memory block. The many built-in analog peripherals include a configurable 32:1 input analog MUX, up to 10 independent MOSFET gate driver outputs, and a configurable ADC. The ADC supports 8-, 10-, and 12-bit modes of operation with a cumulative sample rate up to 600 k samples per second (Ksps), differential nonlinearity (DNL) < 1.0 LSB, and Total Unadjusted Error (TUE) of 0.72 LSB in 10-bit mode. The TUE is used for characterization of the conversion error and includes errors from all sources, such as offset and linearity. Internal bandgap circuitry offers 1% voltage reference accuracy with the flexibility of utilizing an external reference voltage. The ADC channel sampling sequence and sampling rate are programmable and implemented in the FPGA logic using Designer and Libero SoC software tool support.

Two channels of the 32-channel ADCMUX are dedicated. Channel 0 is connected internally to VCC and can be used to monitor core power supply. Channel 31 is connected to an internal temperature diode which can be used to monitor device temperature. The 30 remaining channels can be connected to external analog signals. The exact number of I/Os available for external connection signals is device-dependent (refer to the "Fusion Family" table on page I for details).

Global Resource Characteristics

AFS600 VersaNet Topology

Clock delays are device-specific. Figure 2-15 is an example of a global tree used for clock routing. The global tree presented in Figure 2-15 is driven by a CCC located on the west side of the AFS600 device. It is used to drive all D-flip-flops in the device.

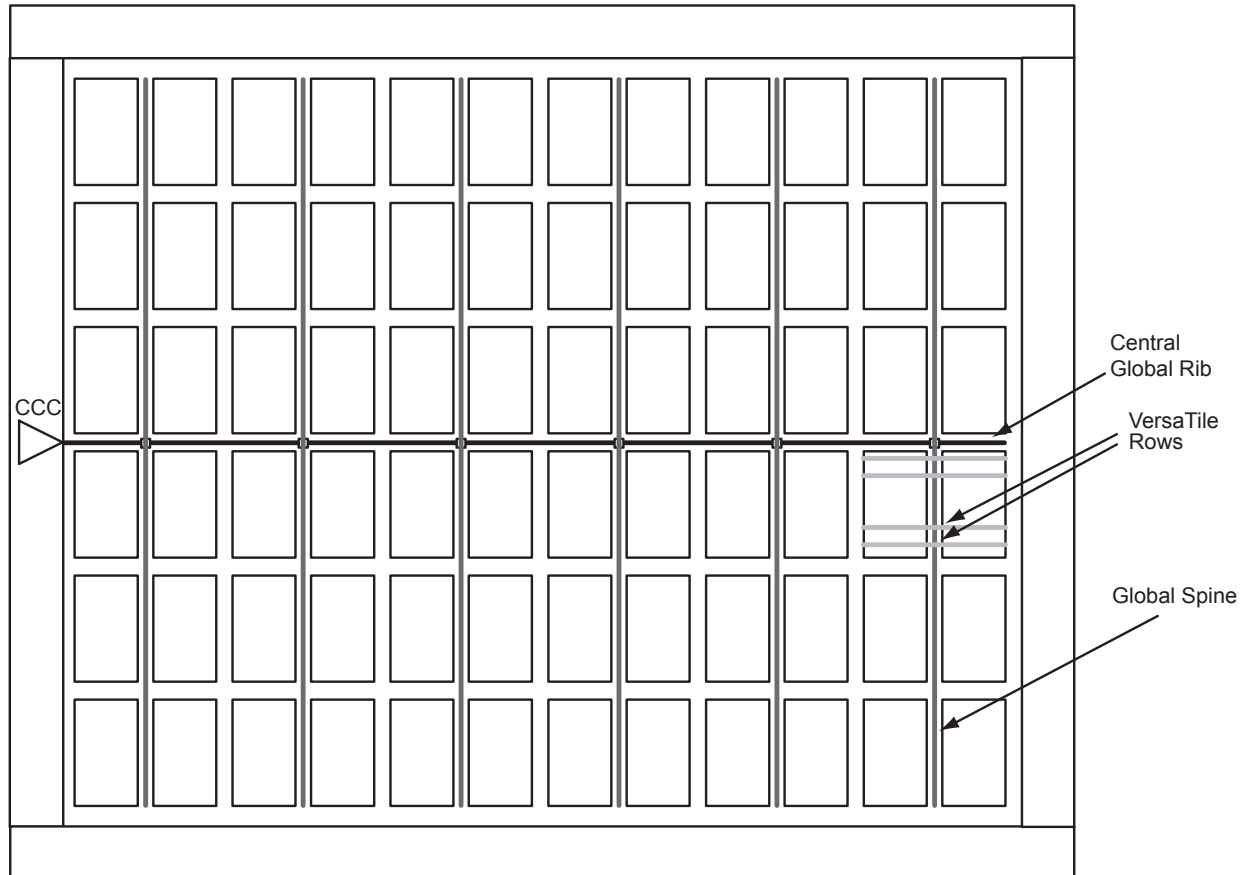


Figure 2-15 • Example of Global Tree Use in an AFS600 Device for Clock Routing

SRAM and FIFO

All Fusion devices have SRAM blocks along the north side of the device. Additionally, AFS600 and AFS1500 devices have an SRAM block on the south side of the device. To meet the needs of high-performance designs, the memory blocks operate strictly in synchronous mode for both read and write operations. The read and write clocks are completely independent, and each may operate at any desired frequency less than or equal to 350 MHz. The following configurations are available:

- 4k×1, 2k×2, 1k×4, 512×9 (dual-port RAM—two read, two write or one read, one write)
- 512×9, 256×18 (two-port RAM—one read and one write)
- Sync write, sync pipelined/nonpipelined read

The Fusion SRAM memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY).

During RAM operation, addresses are sourced by the user logic, and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Refer to [Figure 2-47](#) for more information about the implementation of the embedded FIFO controller.

The Fusion architecture enables the read and write sizes of RAMs to be organized independently, allowing for bus conversion. This is done with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1. For example, the write size can be set to 256×18 and the read size to 512×9.

Both the write and read widths for the RAM blocks can be specified independently with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1.

Refer to the allowable RW and WW values supported for each of the RAM macro types in [Table 2-27 on page 2-58](#).

When a width of one, two, or four is selected, the ninth bit is unused. For example, when writing 9-bit values and reading 4-bit values, only the first four bits and the second four bits of each 9-bit value are addressable for read operations. The ninth bit is not accessible.

The following signals are used to configure the FIFO4K18 memory element.

WW and RW

These signals enable the FIFO to be configured in one of the five allowable aspect ratios ([Table 2-33](#)).

Table 2-33 • Aspect Ratio Settings for WW[2:0]

WW2, WW1, WW0	RW2, RW1, RW0	D×W
000	000	4k×1
001	001	2k×2
010	010	1k×4
011	011	512×9
100	100	256×18
101, 110, 111	101, 110, 111	Reserved

WBLK and RBLK

These signals are active low and will enable the respective ports when Low. When the RBLK signal is High, the corresponding port's outputs hold the previous value.

WEN and REN

Read and write enables. WEN is active low and REN is active high by default. These signals can be configured as active high or low.

WCLK and RCLK

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

RPIPE

This signal is used to specify pipelined read on the output. A Low on RPIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A High indicates a pipelined read, and data appears on the output in the next clock cycle.

RESET

This active low signal resets the output to zero when asserted. It resets the FIFO counters. It also sets all the RD pins Low, the FULL and AFULL pins Low, and the EMPTY and AEMPTY pins High ([Table 2-34](#)).

Table 2-34 • Input Data Signal Usage for Different Aspect Ratios

D×W	WD/RD Unused
4k×1	WD[17:1], RD[17:1]
2k×2	WD[17:2], RD[17:2]
1k×4	WD[17:4], RD[17:4]
512×9	WD[17:9], RD[17:9]
256×18	—

WD

This is the input data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. When a data width less than 18 is specified, unused higher-order signals must be grounded ([Table 2-34](#)).

RD

This is the output data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. Like the WD bus, high-order bits become unusable if the data width is less than 18. The output data on unused pins is undefined ([Table 2-34](#)).

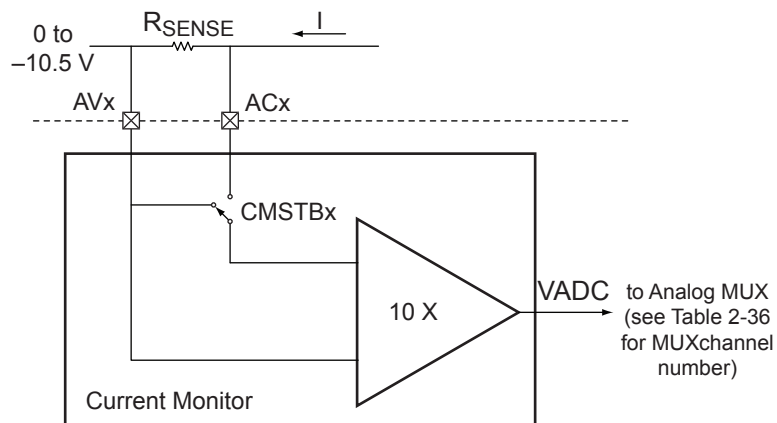


Figure 2-73 • Negative Current Monitor

Terminology

Accuracy

The accuracy of Fusion Current Monitor is ± 2 mV minimum plus 5% of the differential voltage at the input. The input accuracy can be translated to error at the ADC output by using EQ 4. The 10 V/V gain is the gain of the Current Monitor Circuit, as described in the "Current Monitor" section on page 2-86. For 8-bit mode, $N = 8$, $V_{AREF} = 2.56$ V, zero differential voltage between AV and AC, the Error (E_{ADC}) is equal to 2 LSBs.

$$E_{ADC} = (2mV + 0.05|V_{AV} - V_{AC}|) \times (10V)/V \times \frac{2^N}{V_{AREF}}$$

EQ 4

where

N is the number of bits

V_{AREF} is the Reference voltage

V_{AV} is the voltage at AV pad

V_{AC} is the voltage at AC pad

Temperature Monitor

The final pin in the Analog Quad is the Analog Temperature (AT) pin. The AT pin is used to implement an accurate temperature monitor in conjunction with an external diode-connected bipolar transistor (Figure 2-76). For improved temperature measurement accuracy, it is important to use the ATRTN pin for the return path of the current sourced by the AT pin. Each ATRTN pin is shared between two adjacent Analog Quads. Additionally, if not used for temperature monitoring, the AT pin can provide functionality similar to that of the AV pad. However, in this mode only positive voltages can be applied to the AT pin, and only two prescaler factors are available (16 V and 4 V ranges—refer to Table 2-57 on page 2-130).

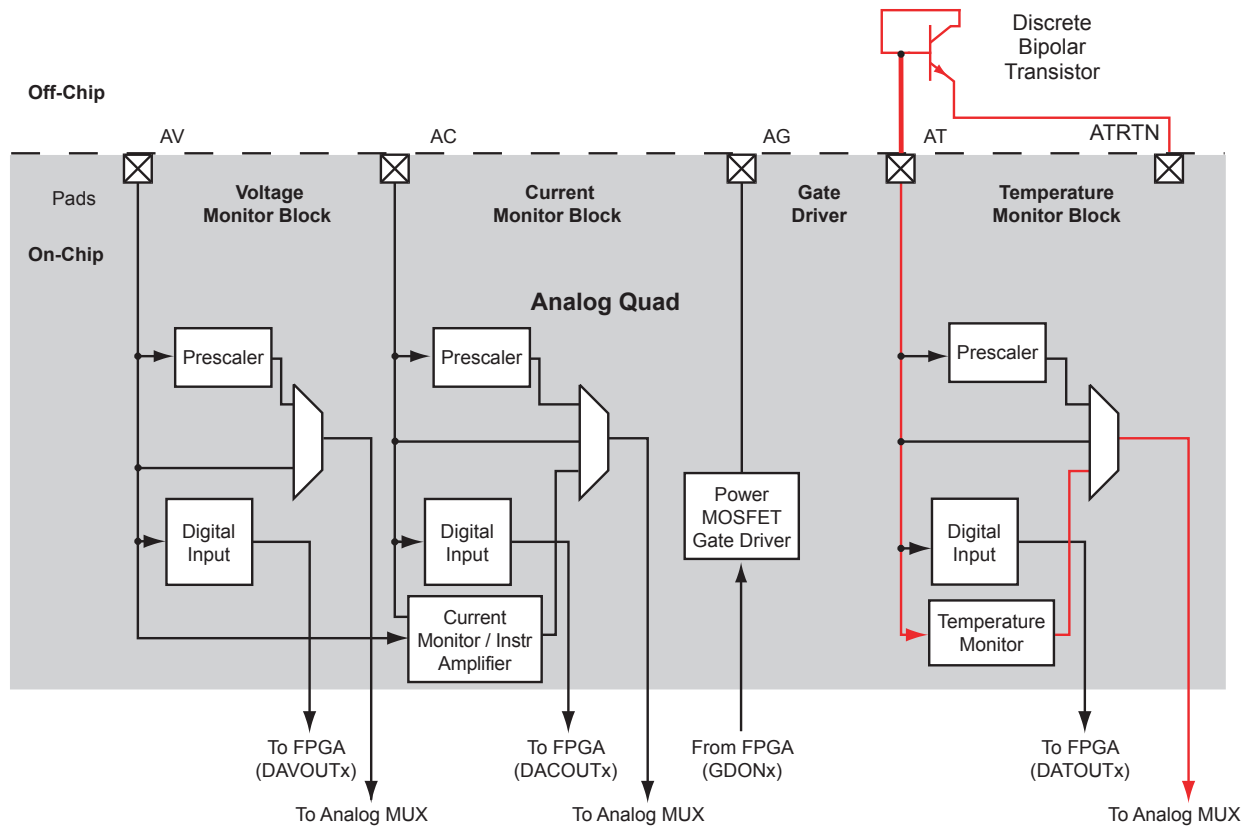


Figure 2-76 • Temperature Monitor Quad

ADC Terminology

Conversion Time

Conversion time is the interval between the release of the hold state (imposed by the input circuitry of a track-and-hold) and the instant at which the voltage on the sampling capacitor settles to within one LSB of a new input value.

DNL – Differential Non-Linearity

For an ideal ADC, the analog-input levels that trigger any two successive output codes should differ by one LSB (DNL = 0). Any deviation from one LSB is defined as DNL (Figure 2-83).

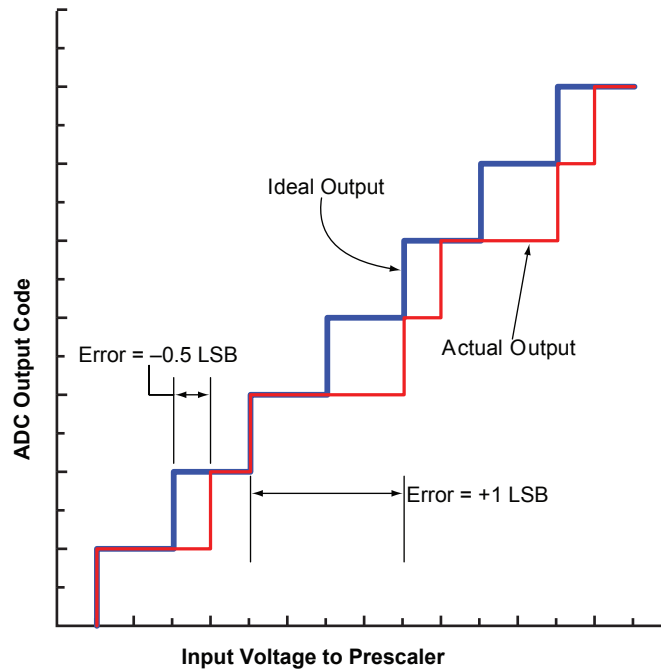


Figure 2-83 • Differential Non-Linearity (DNL)

ENOB – Effective Number of Bits

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists only of quantization of noise. As the input frequency increases, the overall noise (particularly in the distortion components) also increases, thereby reducing the ENOB and SINAD (also see "Signal-to-Noise and Distortion Ratio (SINAD)"). ENOB for a full-scale, sinusoidal input waveform is computed using EQ 12.

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

EQ 12

FS Error – Full-Scale Error

Full-scale error is the difference between the actual value that triggers that transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error.

Table 2-49 • Analog Channel Specifications (continued)
Commercial Temperature Range Conditions, $T_J = 85^\circ\text{C}$ (unless noted otherwise),
Typical: $V_{CC33A} = 3.3\text{ V}$, $V_{CC} = 1.5\text{ V}$

Parameter	Description	Condition	Min.	Typ.	Max.	Units
Digital Input using Analog Pads AV, AC and AT						
VIND ^{2,3}	Input Voltage	Refer to Table 3-2 on page 3-3				
VHYSIN	Hysteresis			0.3		V
VIHDIN	Input High			1.2		V
VILDIN	Input Low			0.9		V
VMPWDIN	Minimum Pulse Width		50			ns
F_{DIN}	Maximum Frequency				10	MHz
ISTBDIN	Input Leakage Current			2		μA
IDYNDIN	Dynamic Current			20		μA
t_{INDIN}	Input Delay			10		ns
Gate Driver Output Using Analog Pad AG						
VG	Voltage Range	Refer to Table 3-2 on page 3-3				
IG	Output Current Drive	High Current Mode ⁶ at 1.0 V			± 20	mA
		Low Current Mode: $\pm 1\text{ }\mu\text{A}$	0.8	1.0	1.3	μA
		Low Current Mode: $\pm 3\text{ }\mu\text{A}$	2.0	2.7	3.3	μA
		Low Current Mode: $\pm 10\text{ }\mu\text{A}$	7.4	9.0	11.5	μA
		Low Current Mode: $\pm 30\text{ }\mu\text{A}$	21.0	27.0	32.0	μA
IOFFG	Maximum Off Current				100	nA
F_G	Maximum switching rate	High Current Mode ⁶ at 1.0 V, 1 k Ω resistive load		1.3		MHz
		Low Current Mode: $\pm 1\text{ }\mu\text{A}$, 3 M Ω resistive load		3		KHz
		Low Current Mode: $\pm 3\text{ }\mu\text{A}$, 1 M Ω resistive load		7		KHz
		Low Current Mode: $\pm 10\text{ }\mu\text{A}$, 300 k Ω resistive load		25		KHz
		Low Current Mode: $\pm 30\text{ }\mu\text{A}$, 105 k Ω resistive load		78		KHz

Notes:

1. V_{RSM} is the maximum voltage drop across the current sense resistor.
2. Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as VIND does not exceed these limits.
3. VIND is limited to $V_{CC33A} + 0.2$ to allow reaching 10 MHz input frequency.
4. An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.
5. The temperature offset is a fixed positive value.
6. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.
7. When using SmartGen Analog System Builder, CalibIP is required to obtain specified offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the [Fusion FPGA Fabric User Guide](#).

User I/Os

Introduction

Fusion devices feature a flexible I/O structure, supporting a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) through a bank-selectable voltage. [Table 2-68](#), [Table 2-69](#), [Table 2-70](#), and [Table 2-71 on page 2-135](#) show the voltages and the compatible I/O standards. I/Os provide programmable slew rates, drive strengths, weak pull-up, and weak pull-down circuits. 3.3 V PCI and 3.3 V PCI-X are 5 V-tolerant. See the ["5 V Input Tolerance" section on page 2-144](#) for possible implementations of 5 V tolerance.

All I/Os are in a known state during power-up, and any power-up sequence is allowed without current impact. Refer to the ["I/O Power-Up and Supply Voltage Thresholds for Power-On Reset \(Commercial and Industrial\)" section on page 3-5](#) for more information. In low power standby or sleep mode (VCC is OFF, VCC33A is ON, VCCI is ON) or when the resource is not used, digital inputs are tristated, digital outputs are tristated, and digital bibufs (input/output) are tristated.

I/O Tile

The Fusion I/O tile provides a flexible, programmable structure for implementing a large number of I/O standards. In addition, the registers available in the I/O tile in selected I/O banks can be used to support high-performance register inputs and outputs, with register enable if desired ([Figure 2-99 on page 2-133](#)). The registers can also be used to support the JESD-79C DDR standard within the I/O structure (see the ["Double Data Rate \(DDR\) Support" section on page 2-139](#) for more information).

As depicted in [Figure 2-100 on page 2-138](#), all I/O registers share one CLR port. The output register and output enable register share one CLK port. Refer to the ["I/O Registers" section on page 2-138](#) for more information.

I/O Banks and I/O Standards Compatibility

The digital I/Os are grouped into I/O voltage banks. There are three digital I/O banks on the AFS090 and AFS250 devices and four digital I/O banks on the AFS600 and AFS1500 devices. [Figure 2-113 on page 2-158](#) and [Figure 2-114 on page 2-159](#) show the bank configuration by device. The north side of the I/O in the AFS600 and AFS1500 devices comprises two banks of Pro I/Os. The Pro I/Os support a wide number of voltage-referenced I/O standards in addition to the multitude of single-ended and differential I/O standards common throughout all Microsemi digital I/Os. Each I/O voltage bank has dedicated I/O supply and ground voltages (VCCI/GNDQ for input buffers and VCCI/GND for output buffers). Because of these dedicated supplies, only I/Os with compatible standards can be assigned to the same I/O voltage bank. [Table 2-69](#) and [Table 2-70 on page 2-134](#) show the required voltage compatibility values for each of these voltages.

For more information about I/O and global assignments to I/O banks, refer to the specific pin table of the device in the ["Package Pin Assignments" on page 4-1](#) and the ["User I/O Naming Convention" section on page 2-158](#).

Each Pro I/O bank is divided into minibanks. Any user I/O in a VREF minibank (a minibank is the region of scope of a VREF pin) can be configured as a VREF pin ([Figure 2-99 on page 2-133](#)). Only one VREF pin is needed to control the entire VREF minibank. The location and scope of the VREF minibanks can be determined by the I/O name. For details, see the ["User I/O Naming Convention" section on page 2-158](#).

[Table 2-70 on page 2-134](#) shows the I/O standards supported by Fusion devices and the corresponding voltage levels.

I/O standards are compatible if the following are true:

- Their VCCI values are identical.
- If both of the standards need a VREF, their VREF values must be identical (Pro I/O only).

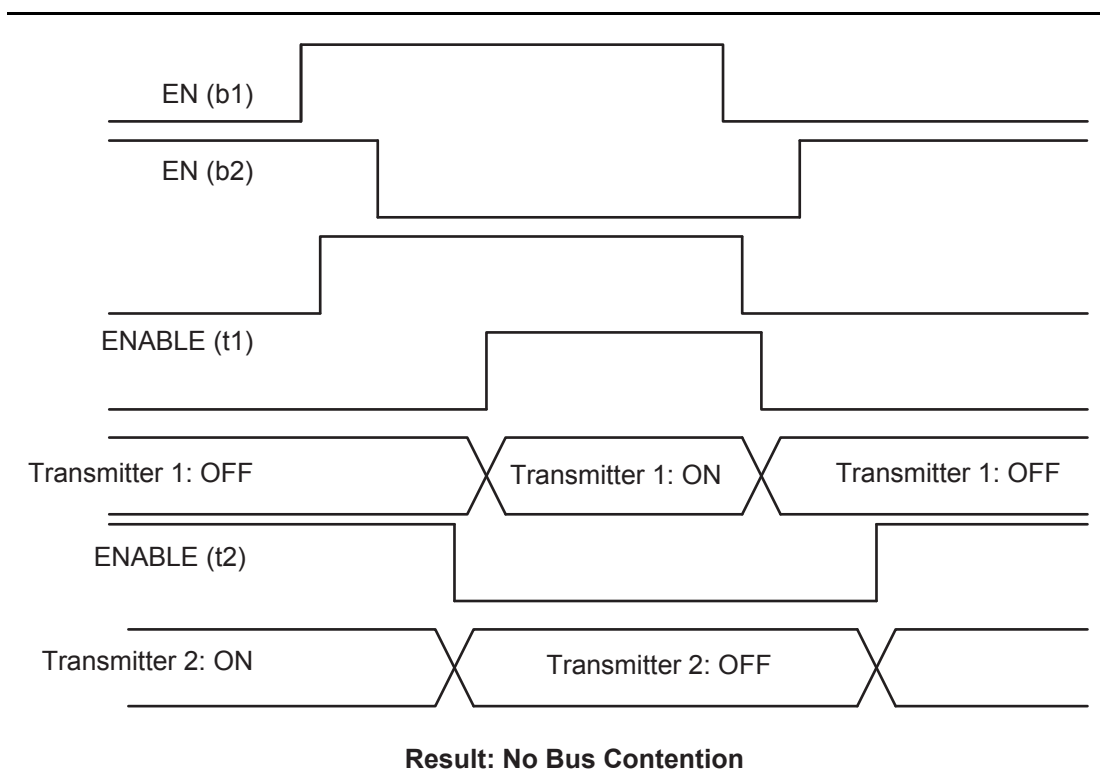


Figure 2-112 • Timing Diagram (with skew circuit selected)

Weak Pull-Up and Weak Pull-Down Resistors

Fusion devices support optional weak pull-up and pull-down resistors for each I/O pin. When the I/O is pulled up, it is connected to the VCCI of its corresponding I/O bank. When it is pulled down, it is connected to GND. Refer to [Table 2-97 on page 2-171](#) for more information.

Slew Rate Control and Drive Strength

Fusion devices support output slew rate control: high and low. The high slew rate option is recommended to minimize the propagation delay. This high-speed option may introduce noise into the system if appropriate signal integrity measures are not adopted. Selecting a low slew rate reduces this kind of noise but adds some delays in the system. Low slew rate is recommended when bus transients are expected. Drive strength should also be selected according to the design requirements and noise immunity of the system.

The output slew rate and multiple drive strength controls are available in LVTTTL/LVCMOS 3.3 V, LVCMOS 2.5 V, LVCMOS 2.5 V / 5.0 V input, LVCMOS 1.8 V, and LVCMOS 1.5 V. All other I/O standards have a high output slew rate by default.

For Fusion slew rate and drive strength specifications, refer to the appropriate I/O bank table:

- Fusion Standard I/O ([Table 2-78 on page 2-152](#))
- Fusion Advanced I/O ([Table 2-79 on page 2-152](#))
- Fusion Pro I/O ([Table 2-80 on page 2-152](#))

[Table 2-83 on page 2-155](#) lists the default values for the above selectable I/O attributes as well as those that are preset for each I/O standard.

Refer to [Table 2-78](#), [Table 2-79](#), and [Table 2-80 on page 2-152](#) for SLEW and OUT_DRIVE settings. [Table 2-81 on page 2-153](#) and [Table 2-82 on page 2-154](#) list the I/O default attributes. [Table 2-83 on page 2-155](#) lists the voltages for the supported I/O standards.

Table 2-114 • 2.5 V LVCMOS Low Slew
Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	11.40	0.04	1.31	0.43	11.22	11.40	2.68	2.20	13.45	13.63	ns
	–1	0.56	9.69	0.04	1.11	0.36	9.54	9.69	2.28	1.88	11.44	11.60	ns
	–2	0.49	8.51	0.03	0.98	0.32	8.38	8.51	2.00	1.65	10.05	10.18	ns
8 mA	Std.	0.66	7.96	0.04	1.31	0.43	8.11	7.81	3.05	2.89	10.34	10.05	ns
	–1	0.56	6.77	0.04	1.11	0.36	6.90	6.65	2.59	2.46	8.80	8.55	ns
	–2	0.49	5.94	0.03	0.98	0.32	6.05	5.84	2.28	2.16	7.72	7.50	ns
12 mA	Std.	0.66	6.18	0.04	1.31	0.43	6.29	5.92	3.30	3.32	8.53	8.15	ns
	–1	0.56	5.26	0.04	1.11	0.36	5.35	5.03	2.81	2.83	7.26	6.94	ns
	–2	0.49	4.61	0.03	0.98	0.32	4.70	4.42	2.47	2.48	6.37	6.09	ns
16 mA	Std.	0.66	6.18	0.04	1.31	0.43	6.29	5.92	3.30	3.32	8.53	8.15	ns
	–1	0.56	5.26	0.04	1.11	0.36	5.35	5.03	2.81	2.83	7.26	6.94	ns
	–2	0.49	4.61	0.03	0.98	0.32	4.70	4.42	2.47	2.48	6.37	6.09	ns
24 mA	Std.	0.66	6.18	0.04	1.31	0.43	6.29	5.92	3.30	3.32	8.53	8.15	ns
	–1	0.56	5.26	0.04	1.11	0.36	5.35	5.03	2.81	2.83	7.26	6.94	ns
	–2	0.49	4.61	0.03	0.98	0.32	4.70	4.42	2.47	2.48	6.37	6.09	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-153 • Minimum and Maximum DC Input and Output Levels

HSTL Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
15 mA ³	−0.3	VREF − 0.1	VREF + 0.1	3.6	0.4	VCCI − 0.4	15	15	55	66	10	10

Note:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Output drive strength is below JEDEC specification.

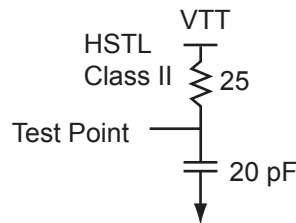


Figure 2-129 • AC Loading

Table 2-154 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF − 0.1	VREF + 0.1	0.75	0.75	0.75	20

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-155 • HSTL Class II

Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V, VREF = 0.75 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.66	3.02	0.04	2.12	0.43	3.08	2.71			5.32	4.95	ns
−1	0.56	2.57	0.04	1.81	0.36	2.62	2.31			4.52	4.21	ns
−2	0.49	2.26	0.03	1.59	0.32	2.30	2.03			3.97	3.70	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-169 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)
1.075	1.325	Cross point	—

Note: *Measuring point = V_{trip} . See [Table 2-90 on page 2-166](#) for a complete table of trip points.

Timing Characteristics

Table 2-170 • LVDS

Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case $V_{CCI} = 2.3\text{ V}$
 Applicable to Pro I/Os

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.66	2.10	0.04	1.82	ns
–1	0.56	1.79	0.04	1.55	ns
–2	0.49	1.57	0.03	1.36	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to [Table 3-7 on page 3-9](#).

BLVDS/M-LVDS

Bus LVDS (BLVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations can contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by BLVDS and M-LVDS to accommodate the loading. The driver requires series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus, since the driver can be located anywhere on the bus. These configurations can be implemented using TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in [Figure 2-135](#). The input and output buffer delays are available in the LVDS section in [Table 2-171](#).

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case industrial operating conditions at the farthest receiver: $R_S = 60\ \Omega$ and $R_T = 70\ \Omega$, given $Z_0 = 50\ \Omega$ (2") and $Z_{stub} = 50\ \Omega$ (~1.5").

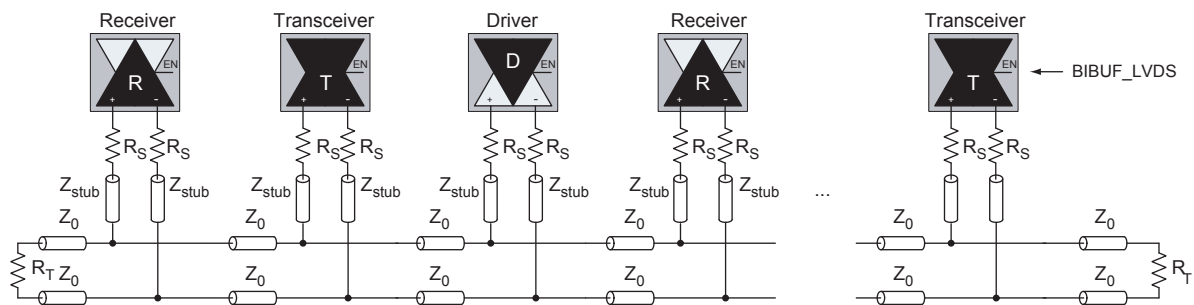


Figure 2-135 • BLVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

XTAL2 Crystal Oscillator Circuit Input

Input to crystal oscillator circuit. Pin for connecting external crystal, ceramic resonator, RC network, or external clock input. When using an external crystal or ceramic oscillator, external capacitors are also recommended (Please refer to the crystal oscillator manufacturer for proper capacitor value).

If using external RC network or clock input, XTAL1 should be used and XTAL2 left unconnected. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.

Security

Fusion devices have a built-in 128-bit AES decryption core. The decryption core facilitates highly secure, in-system programming of the FPGA core array fabric and the FlashROM. The FlashROM and the FPGA core fabric can be programmed independently from each other, allowing the FlashROM to be updated without the need for change to the FPGA core fabric. The AES master key is stored in on-chip nonvolatile memory (flash). The AES master key can be preloaded into parts in a security-protected programming environment (such as the Microsemi in-house programming center), and then "blank" parts can be shipped to an untrusted programming or manufacturing center for final personalization with an AES-encrypted bitstream. Late stage product changes or personalization can be implemented easily and with high level security by simply sending a STAPL file with AES-encrypted data. Highly secure remote field updates over public networks (such as the Internet) are possible by sending and programming a STAPL file with AES-encrypted data. For more information, refer to the [Fusion Security](#) application note.

128-Bit AES Decryption

The 128-bit AES standard (FIPS-197) block cipher is the National Institute of Standards and Technology (NIST) replacement for DES (Data Encryption Standard FIPS46-2). AES has been designed to protect sensitive government information well into the 21st century. It replaces the aging DES, which NIST adopted in 1977 as a Federal Information Processing Standard used by federal agencies to protect sensitive, unclassified information. The 128-bit AES standard has 3.4×10^{38} possible 128-bit key variants, and it has been estimated that it would take 1,000 trillion years to crack 128-bit AES cipher text using exhaustive techniques. Keys are stored (protected with security) in Fusion devices in nonvolatile flash memory. All programming files sent to the device can be authenticated by the part prior to programming to ensure that bad programming data is not loaded into the part that may possibly damage it. All programming verification is performed on-chip, ensuring that the contents of Fusion devices remain as secure as possible.

AES decryption can also be used on the 1,024-bit FlashROM to allow for remote updates of the FlashROM contents. This allows for easy support of subscription model products and protects them with measures designed to provide the highest level of security available. See the application note [Fusion Security](#) for more details.

AES for Flash Memory

AES decryption can also be used on the flash memory blocks. This provides the best available security during update of the flash memory blocks. During runtime, the encrypted data can be clocked in via the JTAG interface. The data can be passed through the internal AES decryption engine, and the decrypted data can then be stored in the flash memory block.

Programming

Programming can be performed using various programming tools, such as Silicon Sculptor II (BP Micro Systems) or FlashPro3 (Microsemi).

The user can generate STP programming files from the Designer software and can use these files to program a device.

Fusion devices can be programmed in-system. During programming, VCCOSC is needed in order to power the internal 100 MHz oscillator. This oscillator is used as a source for the 20 MHz oscillator that is used to drive the charge pump for programming.

IEEE 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/Os" section on page 2-132 for more details.

Timing Characteristics

Table 2-186 • JTAG 1532

Commercial Temperature Range Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.50	0.57	0.67	ns
t_{DIHD}	Test Data Input Hold Time	1.00	1.13	1.33	ns
t_{TMSSU}	Test Mode Select Setup Time	0.50	0.57	0.67	ns
t_{TMDHD}	Test Mode Select Hold Time	1.00	1.13	1.33	ns
t_{TCK2Q}	Clock to Q (data out)	6.00	6.80	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	20.00	22.67	26.67	ns
F_{TCKMAX}	TCK Maximum Frequency	25.00	22.00	19.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.00	0.00	0.00	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.20	0.23	0.27	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	TBD	TBD	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Methodology

Total Power Consumption— P_{TOTAL}

Operating Mode, Standby Mode, and Sleep Mode

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption— P_{STAT}

Operating Mode

$$P_{STAT} = PDC1 + (N_{NVM-BLOCKS} * PDC4) + PDC5 + (N_{QUADS} * PDC6) + (N_{INPUTS} * PDC7) + (N_{OUTPUTS} * PDC8) + (N_{PLLS} * PDC9)$$

$N_{NVM-BLOCKS}$ is the number of NVM blocks available in the device.

N_{QUADS} is the number of Analog Quads used in the design.

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{PLLS} is the number of PLLs available in the device.

Standby Mode

$$P_{STAT} = PDC2$$

Sleep Mode

$$P_{STAT} = PDC3$$

Total Dynamic Power Consumption— P_{DYN}

Operating Mode

$$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM} + P_{XTL-OSC} + P_{RC-OSC} + P_{AB}$$

Standby Mode

$$P_{DYN} = P_{XTL-OSC}$$

Sleep Mode

$$P_{DYN} = 0 \text{ W}$$

Global Clock Dynamic Contribution— P_{CLOCK}

Operating Mode

$$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S-CELL} * PAC4) * F_{CLK}$$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the [Fusion and Extended Temperature Fusion FPGA Fabric User's Guide](#).

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the [Fusion and Extended Temperature Fusion FPGA Fabric User's Guide](#).

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

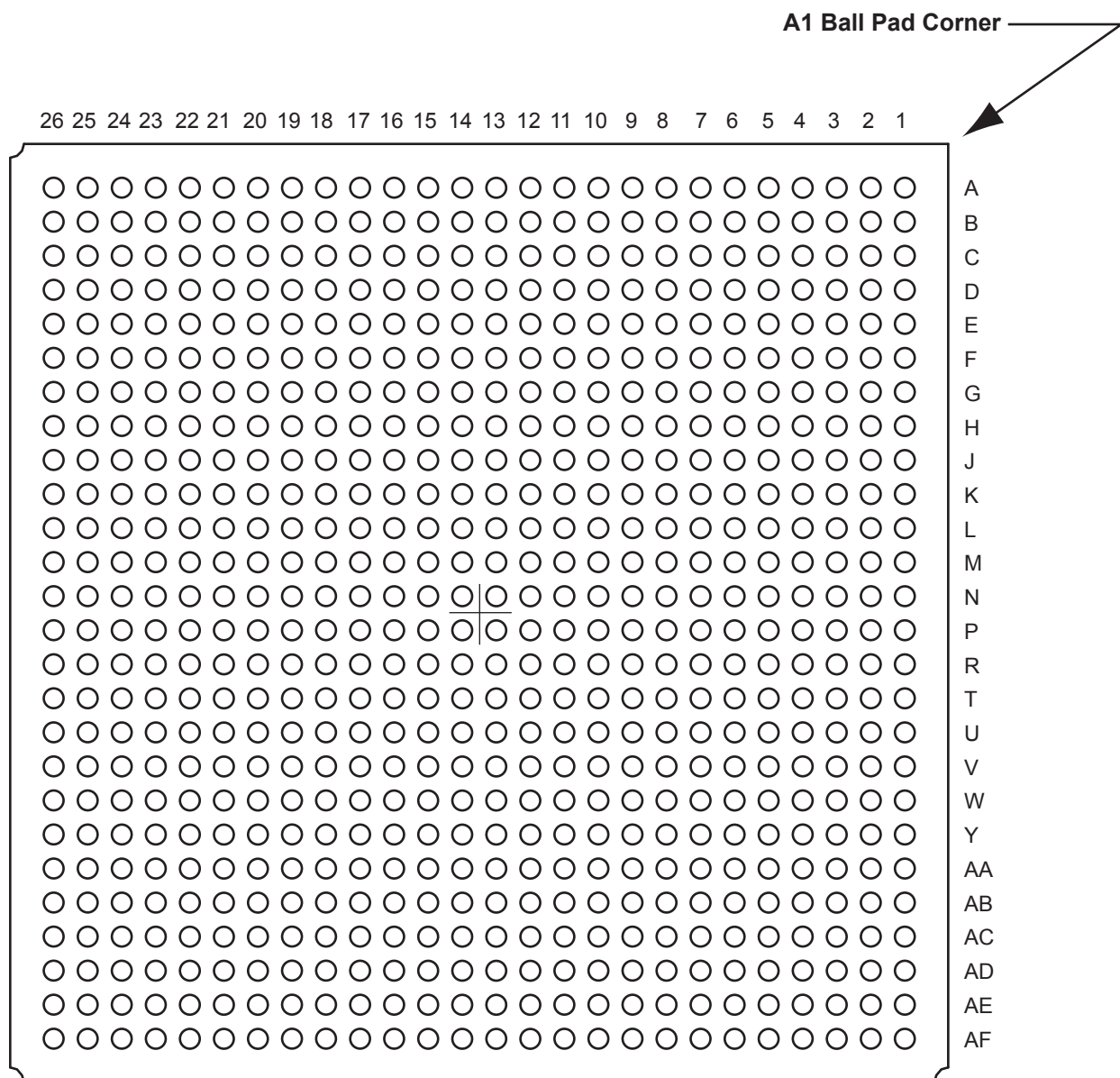
Standby Mode and Sleep Mode

$$P_{CLOCK} = 0 \text{ W}$$

Sequential Cells Dynamic Contribution— P_{S-CELL}

Operating Mode

FG676



Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/default.aspx>.

Revision	Changes	Page
Advance 1.0 (continued)	In Table 2-47 • ADC Characteristics in Direct Input Mode , the commercial conditions were updated and note 2 is new.	2-121
	The $V_{CC33ACAP}$ signal name was changed to "XTAL1 Crystal Oscillator Circuit Input".	2-228
	Table 2-48 • Uncalibrated Analog Channel Accuracy* is new.	2-123
	Table 2-49 • Calibrated Analog Channel Accuracy^{1,2,3} is new.	2-124
	Table 2-50 • Analog Channel Accuracy: Monitoring Standard Positive Voltages is new.	2-125
	In Table 2-57 • Voltage Polarity Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)* , the following I/O Bank names were changed: Hot-Swap changed to Standard LVDS changed to Advanced	2-131
	In Table 2-58 • Prescaler Op Amp Power-Down Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3) , the following I/O Bank names were changed: Hot-Swap changed to Standard LVDS changed to Advanced	2-132
	In the title of Table 2-64 • I/O Standards Supported by Bank Type , LVDS I/O was changed to Advanced I/O.	2-134
	The title was changed from "Fusion Standard, LVDS, and Standard plus Hot-Swap I/O" to Table 2-68 • Fusion Standard and Advanced I/O Features . In addition, the table headings were all updated. The heading used to be Standard and LVDS I/O and was changed to Advanced I/O. Standard Hot-Swap was changed to just Standard.	2-136
	This sentence was deleted from the "Slew Rate Control and Drive Strength" section: The Standard hot-swap I/Os do not support slew rate control. In addition, these references were changed: • From: Fusion hot-swap I/O (Table 2-69 on page 2-122) To: Fusion Standard I/O • From: Fusion LVDS I/O (Table 2-70 on page 2-122) To: Fusion Advanced I/O	2-152
	The "Cold-Sparing Support" section was significantly updated.	2-143
	In the title of Table 2-75 • Fusion Standard I/O Standards—OUT_DRIVE Settings , Hot-Swap was changed to Standard.	2-153
	In the title of Table 2-76 • Fusion Advanced I/O Standards—SLEW and OUT_DRIVE Settings , LVDS was changed to Advanced.	2-153
	In the title of Table 2-81 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications , LVDS was changed to Advanced.	2-157
	In Figure 2-111 • Naming Conventions of Fusion Devices with Three Digital I/O Banks and Figure 2-112 • Naming Conventions of Fusion Devices with Four I/O Banks the following names were changed: Hot-Swap changed to Standard LVDS changed to Advanced	2-160
	The Figure 2-113 • Timing Model was updated.	2-161
	In the notes for Table 2-86 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions , T_J was changed to T_A .	2-166

Revision	Changes	Page
Advance v0.5 (June 2006)	The low power modes of operation were updated and clarified.	N/A
	The AFS1500 digital I/O count was updated in Table 1 • Fusion Family .	i
	The AFS1500 digital I/O count was updated in the "Package I/Os: Single-/Double-Ended (Analog)" table.	ii
	The "Voltage Regulator Power Supply Monitor (VRPSM)" was updated.	2-36
	Figure 2-45 • FlashROM Timing Diagram was updated.	2-53
	The "256-Pin FBGA" table for the AFS1500 is new.	3-12
Advance v0.4 (April 2006)	The G was moved in the "Product Ordering Codes" section.	III
Advance v0.3 (April 2006)	The "Features and Benefits" section was updated.	I
	The "Fusion Family" table was updated.	I
	The "Package I/Os: Single-/Double-Ended (Analog)" table was updated.	II
	The "Product Ordering Codes" table was updated.	III
	The "Temperature Grade Offerings" table was updated.	IV
	The "General Description" section was updated to include ARM information.	1-1
	Figure 2-46 • FlashROM Timing Diagram was updated.	2-58
	The "FlashROM" section was updated.	2-57
	The "RESET" section was updated.	2-61
	The "RESET" section was updated.	2-64
	Figure 2-27 • Real-Time Counter System was updated.	2-35
	Table 2-19 • Flash Memory Block Pin Names was updated.	2-43
	Figure 2-33 • Flash Memory Block Diagram was updated to include AUX block information.	2-45
	Figure 2-34 • Flash Memory Block Organization was updated to include AUX block information.	2-46
	The note in the "Program Operation" section was updated.	2-48
	Figure 2-76 • Gate Driver Example was updated.	2-95
	The "Analog Quad ACM Description" section was updated.	2-130
	Information about the maximum pad input frequency was added to the "Gate Driver" section.	2-94
	Figure 2-65 • Analog Block Macro was updated.	2-81
	Figure 2-65 • Analog Block Macro was updated.	2-81
	The "Analog Quad" section was updated.	2-84
	The "Voltage Monitor" section was updated.	2-86
	The "Direct Digital Input" section was updated.	2-89
	The "Current Monitor" section was updated.	2-90
	Information about the maximum pad input frequency was added to the "Gate Driver" section.	2-94