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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	252
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs1500-2fg676

Clock Aggregation

Clock aggregation allows for multi-spine clock domains. A MUX tree provides the necessary flexibility to allow long lines or I/Os to access domains of one, two, or four global spines. Signal access to the clock aggregation system is achieved through long-line resources in the central rib, and also through local resources in the north and south ribs, allowing I/Os to feed directly into the clock system. As Figure 2-14 indicates, this access system is contiguous.

There is no break in the middle of the chip for north and south I/O VersaNet access. This is different from the quadrant clocks, located in these ribs, which only reach the middle of the rib. Refer to the *Using Global Resources in Actel Fusion Devices* application note.

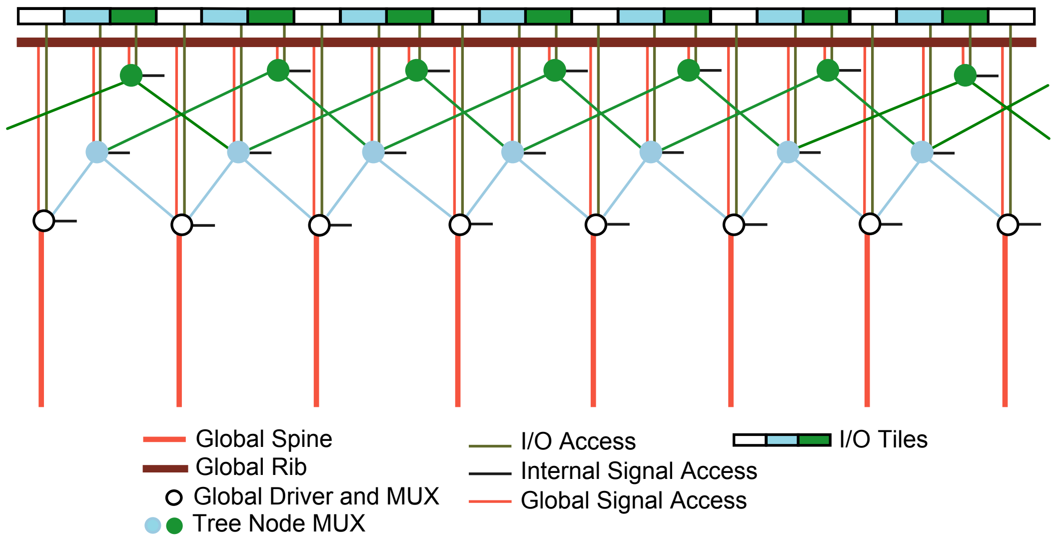


Figure 2-14 • **Clock Aggregation Tree Architecture**

Global Resource Characteristics

AFS600 VersaNet Topology

Clock delays are device-specific. Figure 2-15 is an example of a global tree used for clock routing. The global tree presented in Figure 2-15 is driven by a CCC located on the west side of the AFS600 device. It is used to drive all D-flip-flops in the device.

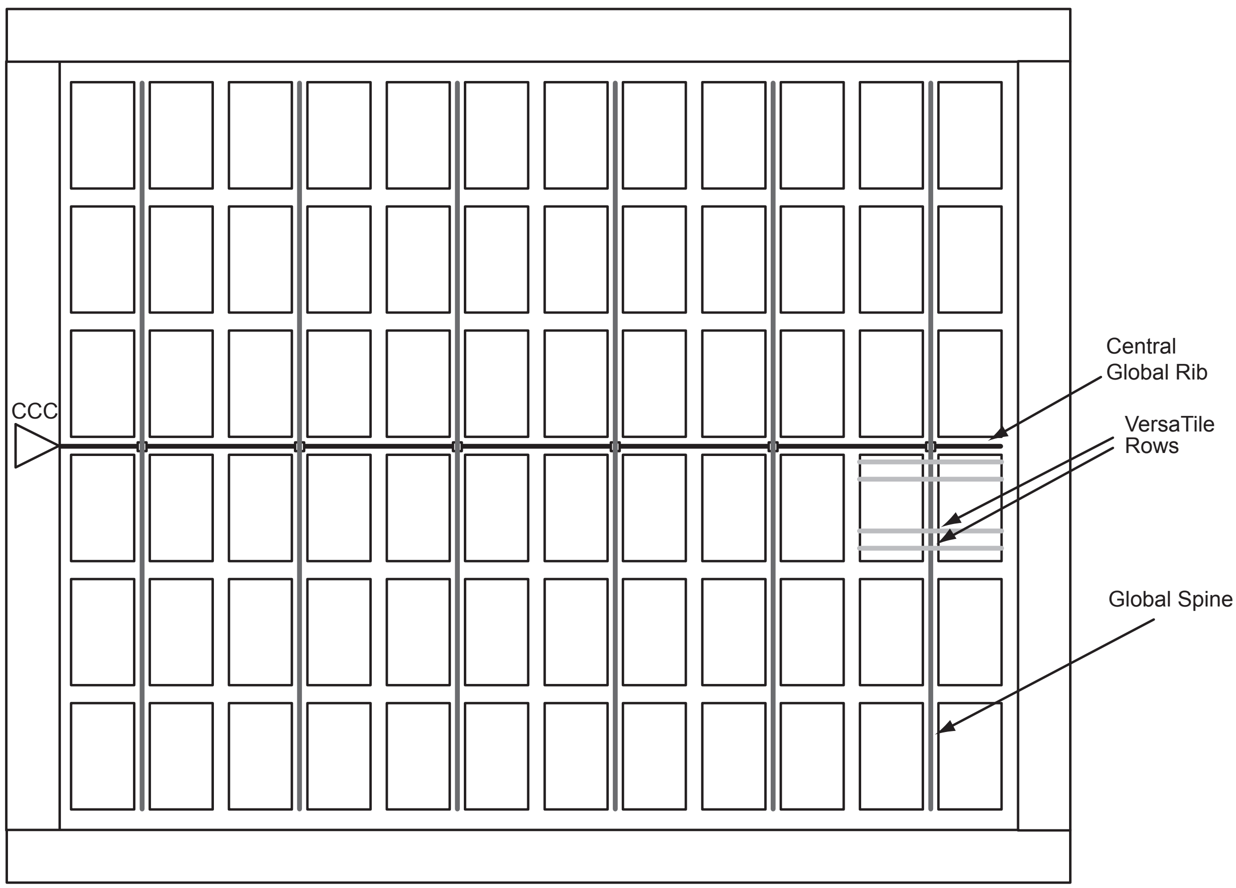


Figure 2-15 • **Example of Global Tree Use in an AFS600 Device for Clock Routing**

Flash Memory Block Characteristics

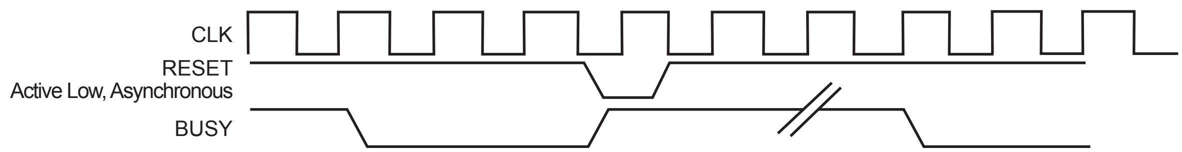


***Figure 2-44* • Reset Timing Diagram**

***Table 2-25* • Flash Memory Block Timing**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{CLK2RD}	Clock-to-Q in 5-cycle read mode of the Read Data	7.99	9.10	10.70	ns
	Clock-to-Q in 6-cycle read mode of the Read Data	5.03	5.73	6.74	ns
$t_{CLK2BUSY}$	Clock-to-Q in 5-cycle read mode of BUSY	4.95	5.63	6.62	ns
	Clock-to-Q in 6-cycle read mode of BUSY	4.45	5.07	5.96	ns
$t_{CLK2STATUS}$	Clock-to-Status in 5-cycle read mode	11.24	12.81	15.06	ns
	Clock-to-Status in 6-cycle read mode	4.48	5.10	6.00	ns
t_{DSUNVM}	Data Input Setup time for the Control Logic	1.92	2.19	2.57	ns
t_{DHNVM}	Data Input Hold time for the Control Logic	0.00	0.00	0.00	ns
t_{ASUNVM}	Address Input Setup time for the Control Logic	2.76	3.14	3.69	ns
t_{AHNVM}	Address Input Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUDWNVM}$	Data Width Setup time for the Control Logic	1.85	2.11	2.48	ns
$t_{HDDWNVM}$	Data Width Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SURENNVM}$	Read Enable Setup time for the Control Logic	3.85	4.39	5.16	ns
$t_{HDRENNVM}$	Read Enable Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUWENNVM}$	Write Enable Setup time for the Control Logic	2.37	2.69	3.17	ns
$t_{HDWENNVM}$	Write Enable Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUPROGNVM}$	Program Setup time for the Control Logic	2.16	2.46	2.89	ns
$t_{HDPROGNVM}$	Program Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUSPAREPAGE}$	SparePage Setup time for the Control Logic	3.74	4.26	5.01	ns
$t_{HDSPAREPAGE}$	SparePage Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUAUXBLK}$	Auxiliary Block Setup Time for the Control Logic	3.74	4.26	5.00	ns
$t_{HDAUXBLK}$	Auxiliary Block Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SURDNEXT}$	ReadNext Setup Time for the Control Logic	2.17	2.47	2.90	ns
$t_{HDRDNEXT}$	ReadNext Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUERASEPG}$	Erase Page Setup Time for the Control Logic	3.76	4.28	5.03	ns
$t_{HDERASEPG}$	Erase Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUUNPROTECTPG}$	Unprotect Page Setup Time for the Control Logic	2.01	2.29	2.69	ns
$t_{HDUNPROTECTPG}$	Unprotect Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUDISCARDPG}$	Discard Page Setup Time for the Control Logic	1.88	2.14	2.52	ns
$t_{HDDISCARDPG}$	Discard Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUOVERWRPRO}$	Overwrite Protect Setup Time for the Control Logic	1.64	1.86	2.19	ns
$t_{HDOVERWRPRO}$	Overwrite Protect Hold Time for the Control Logic	0.00	0.00	0.00	ns

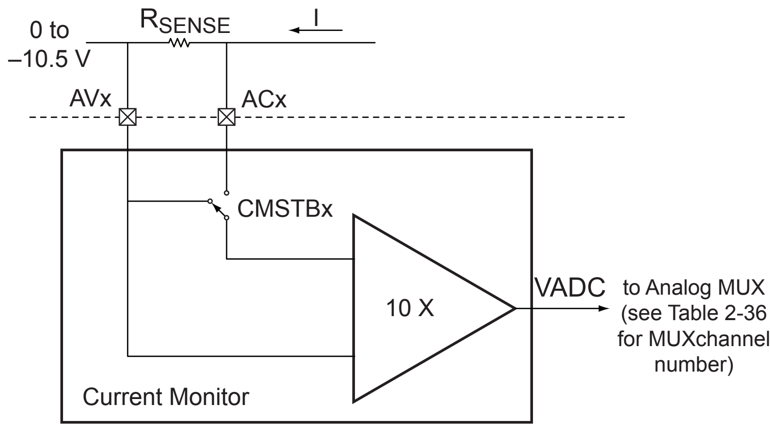


Figure 2-73 • **Negative Current Monitor**

Terminology

Accuracy

The accuracy of Fusion Current Monitor is ±2 mV minimum plus 5% of the differential voltage at the input. The input accuracy can be translated to error at the ADC output by using EQ 4. The 10 V/V gain is the gain of the Current Monitor Circuit, as described in the "Current Monitor" section on page 2-86. For 8-bit mode, $N = 8$, $V_{AREF} = 2.56$ V, zero differential voltage between AV and AC, the Error (E_{ADC}) is equal to 2 LSBs.

$$E_{ADC} = (2mV + 0.05|V_{AV} - V_{AC}|) \times (10V)/V \times \frac{2^N}{V_{AREF}}$$

EQ 4

where

N is the number of bits

V_{AREF} is the Reference voltage

V_{AV} is the voltage at AV pad

V_{AC} is the voltage at AC pad

Terminology

Resolution

Resolution defines the smallest temperature change Fusion Temperature Monitor can resolve. For ADC configured as 8-bit mode, each LSB represents 4°C, and 1°C per LSB for 10-bit mode. With 12-bit mode, the Temperature Monitor can still only resolve 1°C due to Temperature Monitor design.

Offset

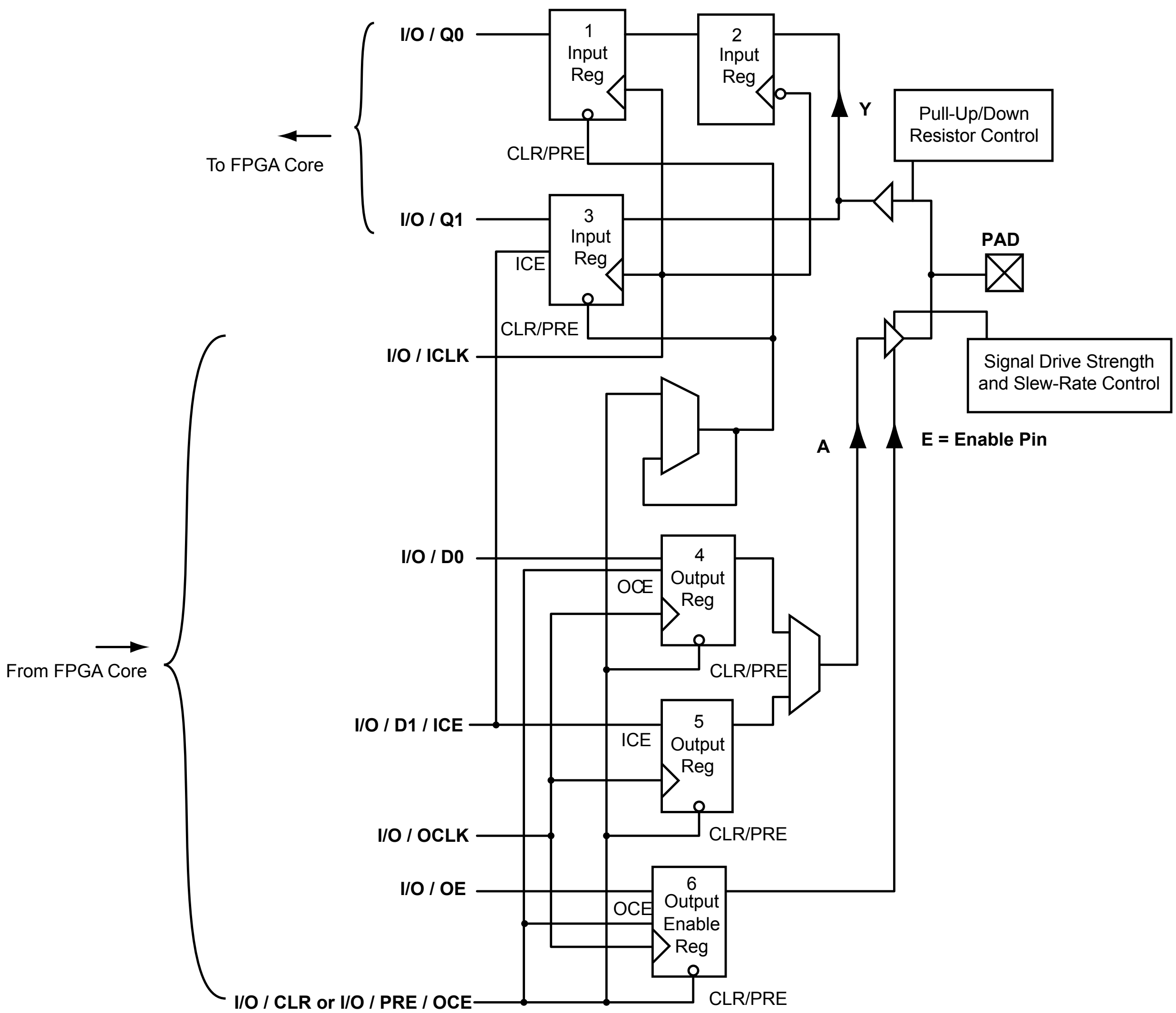
The Fusion Temperature Monitor has a systematic offset (Table 2-49 on page 2-117), excluding error due to board resistance and ideality factor of the external diode. Microsemi provides an IP block (CalibIP) that is required in order to mitigate the systematic temperature offset. For further details on CalibIP, refer to the "*Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the Fusion FPGA Fabric User Guide.*

I/O Registers

Each I/O module contains several input, output, and enable registers. Refer to Figure 2-100 for a simplified representation of the I/O block.

The number of input registers is selected by a set of switches (not shown in Figure 2-100) between registers to implement single or differential data transmission to and from the FPGA core. The Designer software sets these switches for the user.

A common CLR/PRE signal is employed by all I/O registers when I/O register combining is used. Input register 2 does not have a CLR/PRE pin, as this register is used for DDR implementation. The I/O register combining must satisfy some rules.



Note: *Fusion I/Os have registers to support DDR functionality (see the "Double Data Rate (DDR) Support" section on page 2-139 for more information).*

Figure 2-100 **• I/O Block Logical Representation**

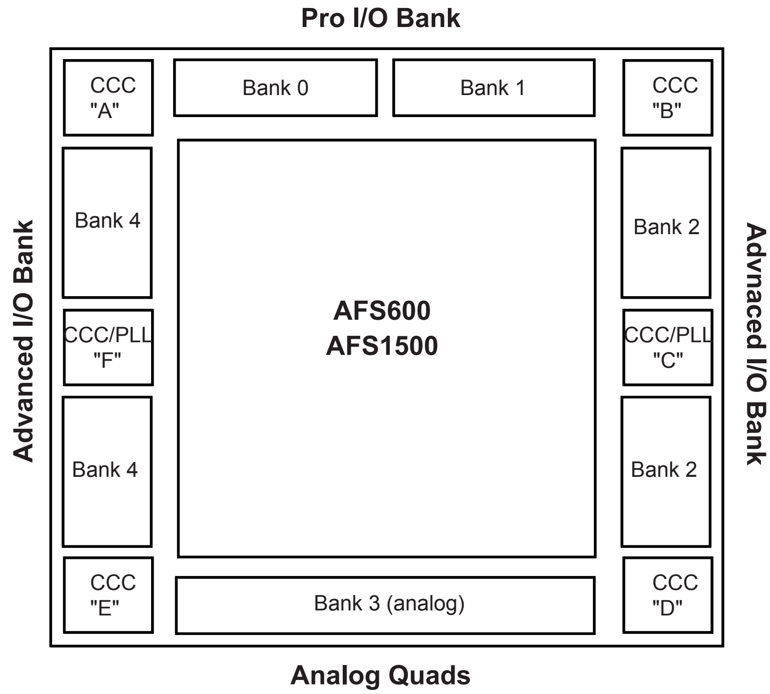


Figure 2-114 **• Naming Conventions of Fusion Devices with Four I/O Banks**

User I/O Characteristics

Timing Model

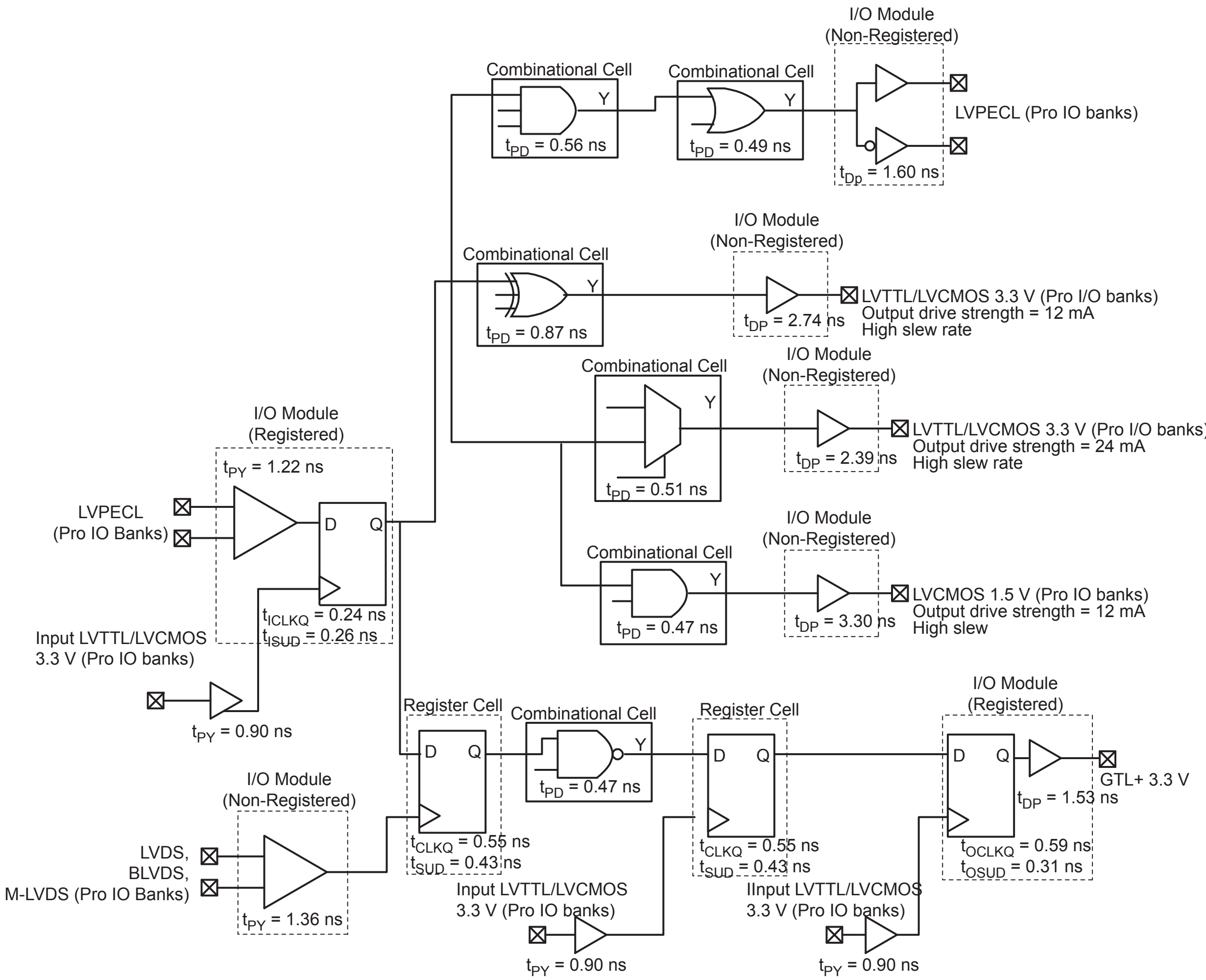


Figure 2-115 **• Timing Model**
Operating Conditions: –2 Speed, Commercial Temperature Range (T_J = 70°C), Worst-Case VCC = 1.425 V

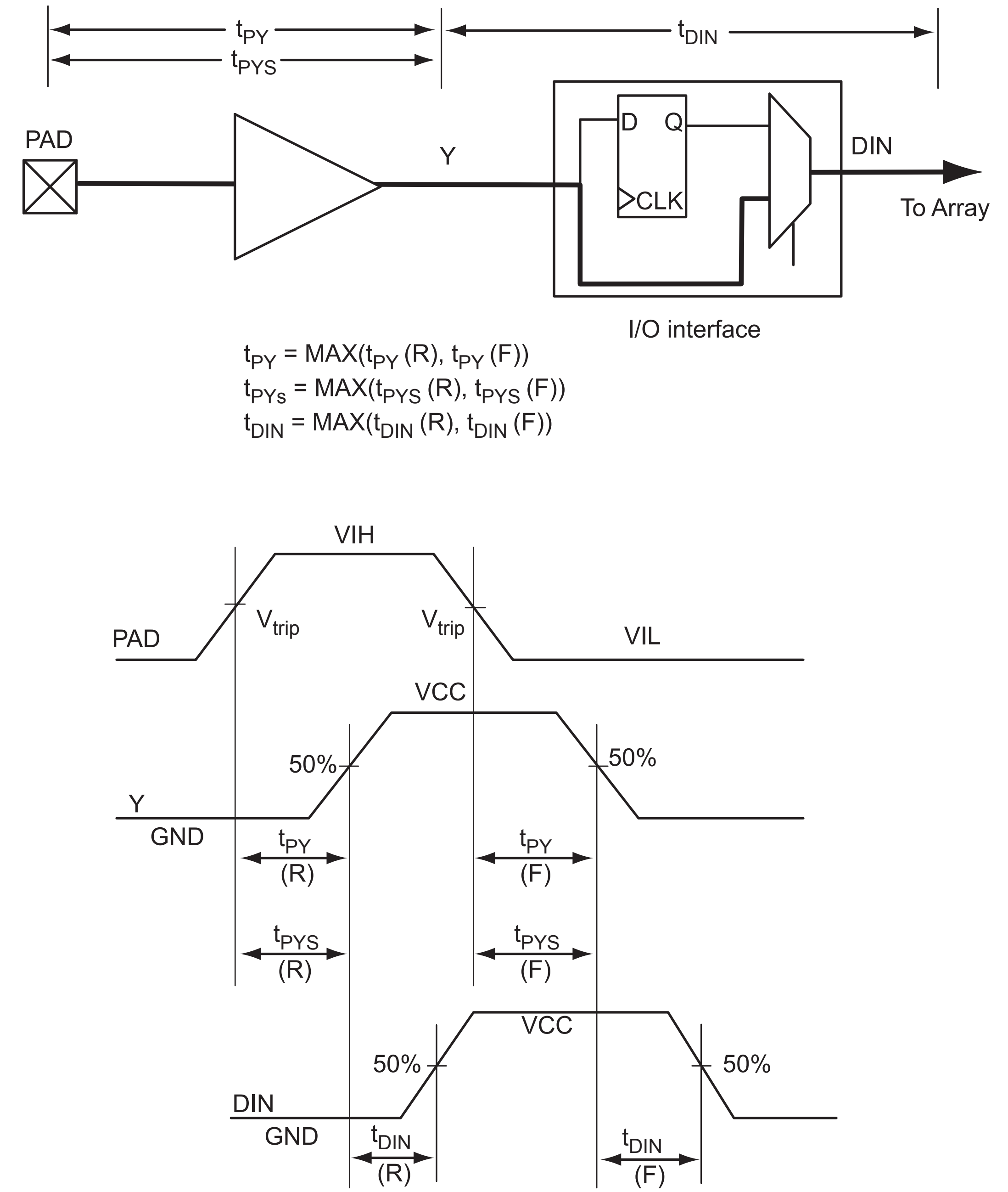


***Figure 2-116* • Input Buffer Timing Model and Delays (example)**

***Table 2-96* • I/O Output Buffer Maximum Resistances [1] (continued)**

Standard	Drive Strength	$R_{PULL-DOWN}$ (ohms) [2]	$R_{PULL-UP}$ (ohms) [3]
Applicable to Standard I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/techdocs/models/ibis.html.*
2. $R_{(PULL-DOWN-MAX)} = VOLspec / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (VCCImax – VOHspec) / IOHspec$

***Table 2-97* • I/O Weak Pull-Up/Pull-Down Resistances**
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

VCCI	$R_{(WEAK\ PULL-UP)}$ [1] (ohms)		$R_{(WEAK\ PULL-DOWN)}$ [2] (ohms)	
	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK\ PULL-UP-MAX)} = (VCCImax – VOHspec) / I_{WEAK\ PULL-UP-MIN}$
2. $R_{(WEAK\ PULL-DOWN-MAX)} = VOLspec / I_{WEAK\ PULL-DOWN-MIN}$

Table 2-121 • 1.8 V LVCMOS High Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Pro I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	12.10	0.04	1.45	1.91	0.43	9.59	12.10	2.78	1.64	11.83	14.34	ns
	–1	0.56	10.30	0.04	1.23	1.62	0.36	8.16	10.30	2.37	1.39	10.06	12.20	ns
	–2	0.49	9.04	0.03	1.08	1.42	0.32	7.16	9.04	2.08	1.22	8.83	10.71	ns
4 mA	Std.	0.66	7.05	0.04	1.45	1.91	0.43	6.20	7.05	3.25	2.86	8.44	9.29	ns
	–1	0.56	6.00	0.04	1.23	1.62	0.36	5.28	6.00	2.76	2.44	7.18	7.90	ns
	–2	0.49	5.27	0.03	1.08	1.42	0.32	4.63	5.27	2.43	2.14	6.30	6.94	ns
8 mA	Std.	0.66	4.52	0.04	1.45	1.91	0.43	4.47	4.52	3.57	3.47	6.70	6.76	ns
	–1	0.56	3.85	0.04	1.23	1.62	0.36	3.80	3.85	3.04	2.95	5.70	5.75	ns
	–2	0.49	3.38	0.03	1.08	1.42	0.32	3.33	3.38	2.66	2.59	5.00	5.05	ns
12 mA	Std.	0.66	4.12	0.04	1.45	1.91	0.43	4.20	3.99	3.63	3.62	6.43	6.23	ns
	–1	0.56	3.51	0.04	1.23	1.62	0.36	3.57	3.40	3.09	3.08	5.47	5.30	ns
	–2	0.49	3.08	0.03	1.08	1.42	0.32	3.14	2.98	2.71	2.71	4.81	4.65	ns
16 mA	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	–1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	–2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-175 • Parameter Definitions and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

Note: *See Figure 2-138 on page 2-214 for more information.

Output Register

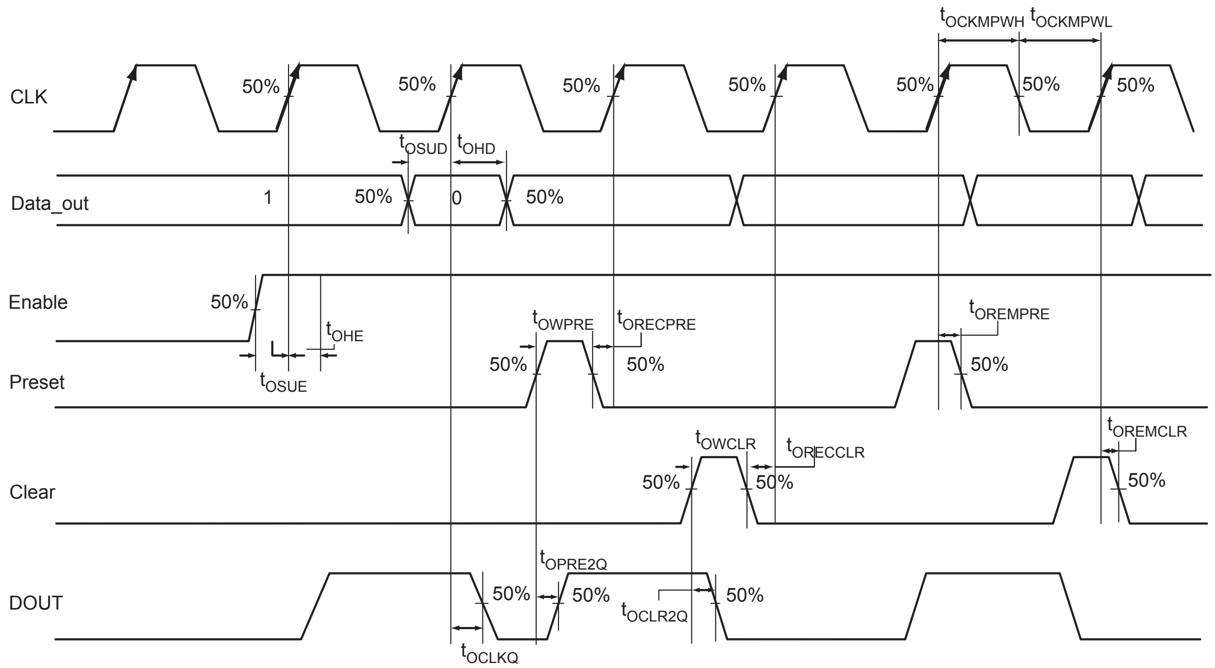


Figure 2-140 • Output Register Timing Diagram

Timing Characteristics

Table 2-177 • Output Data Register Propagation Delays
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.59	0.67	0.79	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.31	0.36	0.42	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.44	0.50	0.59	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.80	0.91	1.07	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.80	0.91	1.07	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.41	0.48	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.37	0.43	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Thermal Characteristics

Introduction

The temperature variable in the Microsemi Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - \theta_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance
θ_{JB} = Junction-to-board thermal resistance
θ_{JC} = Junction-to-case thermal resistance
T_J = Junction temperature
T_A = Ambient temperature
T_B = Board temperature (measured 1.0 mm away from the package edge)
T_C = Case temperature
P = Total power dissipated by the device

Table 3-6 • **Package Thermal Resistance**

Product	θ_{JA}			θ_{JC}	θ_{JB}	Units
	Still Air	1.0 m/s	2.5 m/s			
AFS090-QN108	34.5	30.0	27.7	8.1	16.7	°C/W
AFS090-QN180	33.3	27.6	25.7	9.2	21.2	°C/W
AFS250-QN180	32.2	26.5	24.7	5.7	15.0	°C/W
AFS250-PQ208	42.1	38.4	37	20.5	36.3	°C/W
AFS600-PQ208	23.9	21.3	20.48	6.1	16.5	°C/W
AFS090-FG256	37.7	33.9	32.2	11.5	29.7	°C/W
AFS250-FG256	33.7	30.0	28.3	9.3	24.8	°C/W
AFS600-FG256	28.9	25.2	23.5	6.8	19.9	°C/W
AFS1500-FG256	23.3	19.6	18.0	4.3	14.2	°C/W
AFS600-FG484	21.8	18.2	16.7	7.7	16.8	°C/W
AFS1500-FG484	21.6	16.8	15.2	5.6	14.9	°C/W
AFS1500-FG676	TBD	TBD	TBD	TBD	TBD	°C/W

***Table 3-10* • AFS250 Quiescent Supply Current Characteristics**

Parameter	Description	Conditions	Temp.	Min	Typ	Max	Unit
ICC[1]	1.5 V quiescent current	Operational standby[4], VCC = 1.575 V	T_J = 25°C		4.8	10	mA
			T_J = 85°C		8.2	30	mA
			T_J = 100°C		15	50	mA
		Standby mode[5] or Sleep mode[6], VCC = 0 V			0	0	µA
ICC33[2]	3.3 V analog supplies current	Operational standby[4], VCC33 = 3.63 V	T_J = 25°C		9.8	13	mA
			T_J = 85°C		9.8	14	mA
			T_J = 100°C		10.8	15	mA
		Operational standby, only Analog Quad and –3.3 V output ON, VCC33 = 3.63 V	T_J = 25°C		0.29	2	mA
			T_J = 85°C		0.31	2	mA
			T_J = 100°C		0.45	2	mA
		Standby mode[5], VCC33 = 3.63V	T_J = 25°C		2.9	3.0	mA
			T_J = 85°C		2.9	3.1	mA
			T_J = 100°C		3.5	6	mA
		Sleep mode[6], VCC33 = 3.63 V	T_J = 25°C		19	18	µA
			T_J = 85°C		19	20	µA
			T_J = 100°C		24	25	µA
ICCI[3]	I/O quiescent current	Operational standby[6], VCCIx = 3.63 V	T_J = 25°C		266	437	µA
			T_J = 85°C		266	437	µA
			T_J = 100°C		266	437	µA
IJTAG	JTAG I/O quiescent current	Operational standby[4], VJTAG = 3.63 V	T_J = 25°C		80	100	µA
			T_J = 85°C		80	100	µA
			T_J = 100°C		80	100	µA
		Standby mode[5] or Sleep mode[6], VJTAG = 0 V			0	0	µA

Notes:

1. *ICC is the 1.5 V power supplies, ICC, ICCPLL, ICC15A, ICCNVM.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, and ICCI2.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTA G = VPUMP = 0 V.*

Total Static Power Consumption—P_{STAT}

Number of Quads used: $N_{QUADS} = 4$

Number of NVM blocks available (AFS600): $N_{NVM\text{-}BLOCKS} = 2$

Number of input pins used: $N_{INPUTS} = 30$

Number of output pins used: $N_{OUTPUTS} = 40$

Operating Mode

$P_{STAT} = PDC1 + (N_{NVM\text{-}BLOCKS} * PDC4) + PDC5 + (N_{QUADS} * PDC6) + (N_{INPUTS} * PDC7) + (N_{OUTPUTS} * PDC8)$

$P_{STAT} = 7.50\ mW + (2 * 1.19\ mW) + 8.25\ mW + (4 * 3.30\ mW) + (30 * 0.00) + (40 * 0.00)$

$P_{STAT} = 31.33\ mW$

Standby Mode

$P_{STAT} = PDC2$

$P_{STAT} = 0.03\ mW$

Sleep Mode

$P_{STAT} = PDC3$

$P_{STAT} = 0.03\ mW$

Total Power Consumption—P_{TOTAL}

In operating mode, the total power consumption of the device is 174.39 mW:

$P_{TOTAL} = P_{STAT} + P_{DYN}$

$P_{TOTAL} = 143.06\ mW + 31.33\ mW$

$P_{TOTAL} = 174.39\ mW$

In standby mode, the total power consumption of the device is limited to 0.66 mW:

$P_{TOTAL} = P_{STAT} + P_{DYN}$

$P_{TOTAL} = 0.03\ mW + 0.63\ mW$

$P_{TOTAL} = 0.66\ mW$

In sleep mode, the total power consumption of the device drops as low as 0.03 mW:

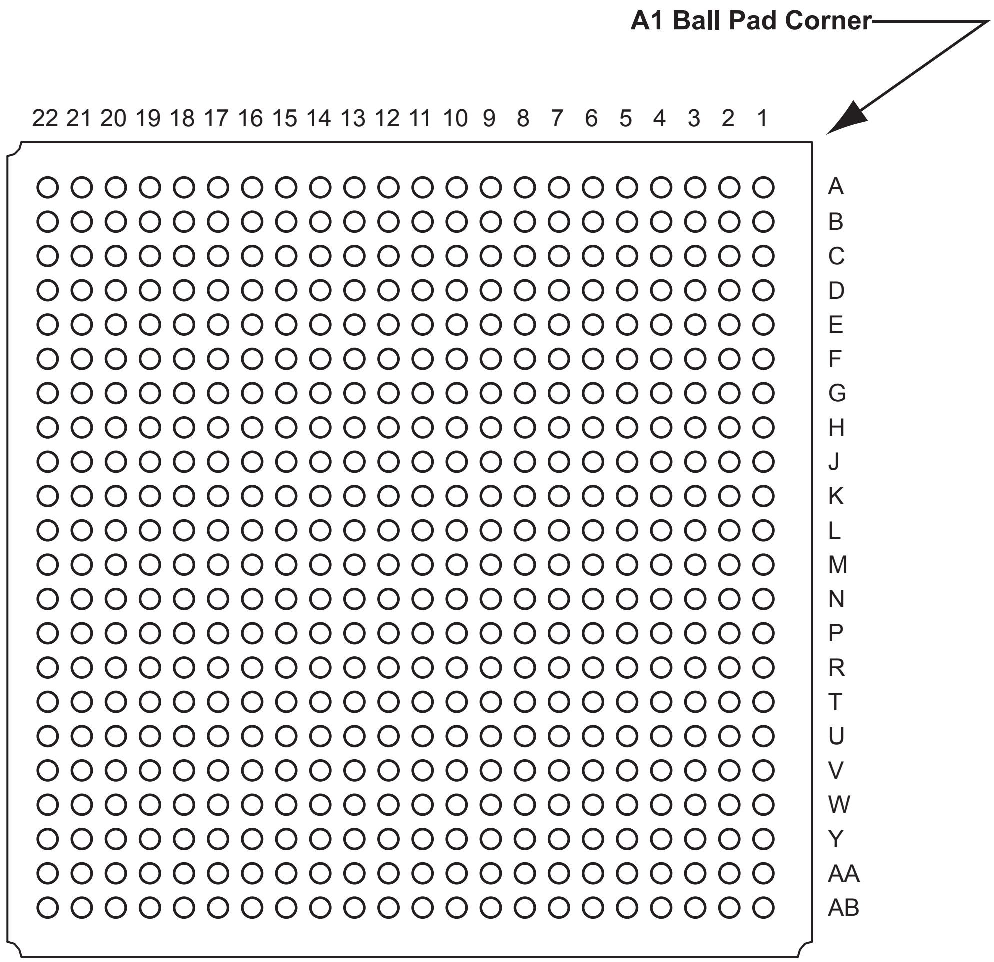
$P_{TOTAL} = P_{STAT} + P_{DYN}$

$P_{TOTAL} = 0.03\ mW$

FG256				
Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function
A1	GND	GND	GND	GND
A2	VCCIB0	VCCIB0	VCCIB0	VCCIB0
A3	GAB0/IO02RSB0V0	GAA0/IO00RSB0V0	GAA0/IO01NDB0V0	GAA0/IO01NDB0V0
A4	GAB1/IO03RSB0V0	GAA1/IO01RSB0V0	GAA1/IO01PDB0V0	GAA1/IO01PDB0V0
A5	GND	GND	GND	GND
A6	IO07RSB0V0	IO11RSB0V0	IO10PDB0V1	IO07PDB0V1
A7	IO10RSB0V0	IO14RSB0V0	IO12PDB0V1	IO13PDB0V2
A8	IO11RSB0V0	IO15RSB0V0	IO12NDB0V1	IO13NDB0V2
A9	IO16RSB0V0	IO24RSB0V0	IO22NDB1V0	IO24NDB1V0
A10	IO17RSB0V0	IO25RSB0V0	IO22PDB1V0	IO24PDB1V0
A11	IO18RSB0V0	IO26RSB0V0	IO24NDB1V1	IO29NDB1V1
A12	GND	GND	GND	GND
A13	GBC0/IO25RSB0V0	GBA0/IO38RSB0V0	GBA0/IO28NDB1V1	GBA0/IO42NDB1V2
A14	GBA0/IO29RSB0V0	IO32RSB0V0	IO29NDB1V1	IO43NDB1V2
A15	VCCIB0	VCCIB0	VCCIB1	VCCIB1
A16	GND	GND	GND	GND
B1	VCOMPLA	VCOMPLA	VCOMPLA	VCOMPLA
B2	VCCPLA	VCCPLA	VCCPLA	VCCPLA
B3	GAA0/IO00RSB0V0	IO07RSB0V0	IO00NDB0V0	IO00NDB0V0
B4	GAA1/IO01RSB0V0	IO06RSB0V0	IO00PDB0V0	IO00PDB0V0
B5	NC	GAB1/IO03RSB0V0	GAB1/IO02PPB0V0	GAB1/IO02PPB0V0
B6	IO06RSB0V0	IO10RSB0V0	IO10NDB0V1	IO07NDB0V1
B7	VCCIB0	VCCIB0	VCCIB0	VCCIB0
B8	IO12RSB0V0	IO16RSB0V0	IO18NDB1V0	IO22NDB1V0
B9	IO13RSB0V0	IO17RSB0V0	IO18PDB1V0	IO22PDB1V0
B10	VCCIB0	VCCIB0	VCCIB1	VCCIB1
B11	IO19RSB0V0	IO27RSB0V0	IO24PDB1V1	IO29PDB1V1
B12	GBB0/IO27RSB0V0	GBC0/IO34RSB0V0	GBC0/IO26NPB1V1	GBC0/IO40NPB1V2
B13	GBC1/IO26RSB0V0	GBA1/IO39RSB0V0	GBA1/IO28PDB1V1	GBA1/IO42PDB1V2
B14	GBA1/IO30RSB0V0	IO33RSB0V0	IO29PDB1V1	IO43PDB1V2
B15	NC	NC	VCCPLB	VCCPLB
B16	NC	NC	VCOMPLB	VCOMPLB
C1	VCCIB3	V**CCI**B3	VCCIB4	VCCIB4
C2	GND	GND	GND	GND
C3	VCCIB3	VCCIB3	VCCIB4	VCCIB4
C4	NC	NC	VCCIB0	VCCIB0
C5	VCCIB0	VCCIB0	VCCIB0	VCCIB0
C6	GAC1/IO05RSB0V0	GAC1/IO05RSB0V0	GAC1/IO03PDB0V0	GAC1/IO03PDB0V0

FG256				
Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function
C7	IO09RSB0V0	IO12RSB0V0	IO06NDB0V0	IO09NDB0V1
C8	IO14RSB0V0	IO22RSB0V0	IO16PDB1V0	IO23PDB1V0
C9	IO15RSB0V0	IO23RSB0V0	IO16NDB1V0	IO23NDB1V0
C10	IO22RSB0V0	IO30RSB0V0	IO25NDB1V1	IO31NDB1V1
C11	IO20RSB0V0	IO31RSB0V0	IO25PDB1V1	IO31PDB1V1
C12	VCCIB0	VCCIB0	VCCIB1	VCCIB1
C13	GBB1/IO28RSB0V0	GBC1/IO35RSB0V0	GBC1/IO26PPB1V1	GBC1/IO40PPB1V2
C14	VCCIB1	VCCIB1	VCCIB2	VCCIB2
C15	GND	GND	GND	GND
C16	VCCIB1	VCCIB1	VCCIB2	VCCIB2
D1	GFC2/IO50NPB3V0	IO75NDB3V0	IO84NDB4V0	IO124NDB4V0
D2	GFA2/IO51NDB3V0	GAB2/IO75PDB3V0	GAB2/IO84PDB4V0	GAB2/IO124PDB4V0
D3	GAC2/IO51PDB3V0	IO76NDB3V0	IO85NDB4V0	IO125NDB4V0
D4	GAA2/IO52PDB3V0	GAA2/IO76PDB3V0	GAA2/IO85PDB4V0	GAA2/IO125PDB4V0
D5	GAB2/IO52NDB3V0	GAB0/IO02RSB0V0	GAB0/IO02NPB0V0	GAB0/IO02NPB0V0
D6	GAC0/IO04RSB0V0	GAC0/IO04RSB0V0	GAC0/IO03NDB0V0	GAC0/IO03NDB0V0
D7	IO08RSB0V0	IO13RSB0V0	IO06PDB0V0	IO09PDB0V1
D8	NC	IO20RSB0V0	IO14NDB0V1	IO15NDB0V2
D9	NC	IO21RSB0V0	IO14PDB0V1	IO15PDB0V2
D10	IO21RSB0V0	IO28RSB0V0	IO23PDB1V1	IO37PDB1V2
D11	IO23RSB0V0	GBB0/IO36RSB0V0	GBB0/IO27NDB1V1	GBB0/IO41NDB1V2
D12	NC	NC	VCCIB1	VCCIB1
D13	GBA2/IO31PDB1V0	GBA2/IO40PDB1V0	GBA2/IO30PDB2V0	GBA2/IO44PDB2V0
D14	GBB2/IO31NDB1V0	IO40NDB1V0	IO30NDB2V0	IO44NDB2V0
D15	GBC2/IO32PDB1V0	GBB2/IO41PDB1V0	GBB2/IO31PDB2V0	GBB2/IO45PDB2V0
D16	GCA2/IO32NDB1V0	IO41NDB1V0	IO31NDB2V0	IO45NDB2V0
E1	GND	GND	GND	GND
E2	GFB0/IO48NPB3V0	IO73NDB3V0	IO81NDB4V0	IO118NDB4V0
E3	GFB2/IO50PPB3V0	IO73PDB3V0	IO81PDB4V0	IO118PDB4V0
E4	VCCIB3	VCCIB3	VCCIB4	VCCIB4
E5	NC	IO74NPB3V0	IO83NPB4V0	IO123NPB4V0
E6	NC	IO08RSB0V0	IO04NPB0V0	IO05NPB0V1
E7	GND	GND	GND	GND
E8	NC	IO18RSB0V0	IO08PDB0V1	IO11PDB0V1
E9	NC	NC	IO20NDB1V0	IO27NDB1V1
E10	GND	GND	GND	GND
E11	IO24RSB0V0	GBB1/IO37RSB0V0	GBB1/IO27PDB1V1	GBB1/IO41PDB1V2
E12	NC	IO50PPB1V0	IO33PSB2V0	IO48PSB2V0

FG484



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/default.aspx.

FG676	
Pin Number	AFS1500 Function
G13	IO22NDB1V0
G14	IO22PDB1V0
G15	GND
G16	IO32PPB1V1
G17	IO36NPB1V2
G18	VCCIB1
G19	GND
G20	IO47NPB2V0
G21	IO49PDB2V0
G22	VCCIB2
G23	IO46NDB2V0
G24	GBC2/IO46PDB2V0
G25	IO48NPB2V0
G26	NC
H1	GND
H2	NC
H3	IO118NDB4V0
H4	IO118PDB4V0
H5	IO119NPB4V0
H6	IO124NDB4V0
H7	GND
H8	VCOMPLA
H9	VCCPLA
H10	VCCIB0
H11	IO12NDB0V1
H12	IO12PDB0V1
H13	VCCIB0
H14	VCCIB1
H15	IO30NDB1V1
H16	IO30PDB1V1
H17	VCCIB1
H18	IO36PPB1V2
H19	IO38NPB1V2
H20	GND
H21	IO49NDB2V0
H22	IO50PDB2V0

FG676	
Pin Number	AFS1500 Function
H23	IO50NDB2V0
H24	IO51PDB2V0
H25	NC
H26	GND
J1	NC
J2	VCCIB4
J3	IO115PDB4V0
J4	GND
J5	IO116NDB4V0
J6	IO116PDB4V0
J7	VCCIB4
J8	IO117PDB4V0
J9	VCCIB4
J10	GND
J11	IO06NDB0V1
J12	IO06PDB0V1
J13	IO16NDB0V2
J14	IO16PDB0V2
J15	IO28NDB1V1
J16	IO28PDB1V1
J17	GND
J18	IO38PPB1V2
J19	IO53PDB2V0
J20	VCCIB2
J21	IO52PDB2V0
J22	IO52NDB2V0
J23	GND
J24	IO51NDB2V0
J25	VCCIB2
J26	NC
K1	NC
K2	NC
K3	IO115NDB4V0
K4	IO113PDB4V0
K5	VCCIB4
K6	IO114NDB4V0

FG676	
Pin Number	AFS1500 Function
K7	IO114PDB4V0
K8	IO117NDB4V0
K9	GND
K10	VCC
K11	VCCIB0
K12	GND
K13	VCCIB0
K14	VCCIB1
K15	GND
K16	VCCIB1
K17	GND
K18	GND
K19	IO53NDB2V0
K20	IO57PDB2V0
K21	GCA2/IO59PDB2V0
K22	VCCIB2
K23	IO54NDB2V0
K24	IO54PDB2V0
K25	NC
K26	NC
L1	GND
L2	NC
L3	IO112PPB4V0
L4	IO113NDB4V0
L5	GFB2/IO109PDB4V0
L6	GFA2/IO110PDB4V0
L7	IO112NPB4V0
L8	IO104PDB4V0
L9	IO111PDB4V0
L10	VCCIB4
L11	GND
L12	VCC
L13	GND
L14	VCC
L15	GND
L16	VCC