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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	119
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs1500-2fgg256i

Embedded Memories

Flash Memory Blocks

The flash memory available in each Fusion device is composed of one to four flash blocks, each 2 Mbits in density. Each block operates independently with a dedicated flash controller and interface. Fusion flash memory blocks combine fast access times (60 ns random access and 10 ns access in Read-Ahead mode) with a configurable 8-, 16-, or 32-bit datapath, enabling high-speed flash operation without wait states. The memory block is organized in pages and sectors. Each page has 128 bytes, with 33 pages comprising one sector and 64 sectors per block. The flash block can support multiple partitions. The only constraint on size is that partition boundaries must coincide with page boundaries. The flexibility and granularity enable many use models and allow added granularity in programming updates.

Fusion devices support two methods of external access to the flash memory blocks. The first method is a serial interface that features a built-in JTAG-compliant port, which allows in-system programmability during user or monitor/test modes. This serial interface supports programming of an AES-encrypted stream. Data protected with security measures can be passed through the JTAG interface, decrypted, and then programmed in the flash block. The second method is a soft parallel interface.

FPGA logic or an on-chip soft microprocessor can access flash memory through the parallel interface. Since the flash parallel interface is implemented in the FPGA fabric, it can potentially be customized to meet special user requirements. For more information, refer to the *CoreCFI Handbook.* The flash memory parallel interface provides configurable byte-wide (×8), word-wide (×16), or dual-word-wide (×32) data-port options. Through the programmable flash parallel interface, the on-chip and off-chip memories can be cascaded for wider or deeper configurations.

The flash memory has built-in security. The user can configure either the entire flash block or the small blocks to protect against unintentional or intrusive attempts to change or destroy the storage contents. Each on-chip flash memory block has a dedicated controller, enabling each block to operate independently.

The flash block logic consists of the following sub-blocks:

- Flash block – Contains all stored data. The flash block contains 64 sectors and each sector contains 33 pages of data.
- Page Buffer – Contains the contents of the current page being modified. A page contains 8 blocks of data.
- Block Buffer – Contains the contents of the last block accessed. A block contains 128 data bits.
- ECC Logic – The flash memory stores error correction information with each block to perform single-bit error correction and double-bit error detection on all data blocks.

User Nonvolatile FlashROM

In addition to the flash blocks, Fusion devices have 1 Kbit of user-accessible, nonvolatile FlashROM on-chip. The FlashROM is organized as 8×128-bit pages. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for communications algorithms protected by security
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IEEE 1532 JTAG programming interface. Pages can be individually programmed (erased and written). On-chip AES decryption can be used selectively over public networks to load data such as security keys stored in the FlashROM for a user design.

The FlashROM can be programmed (erased and written) via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing.

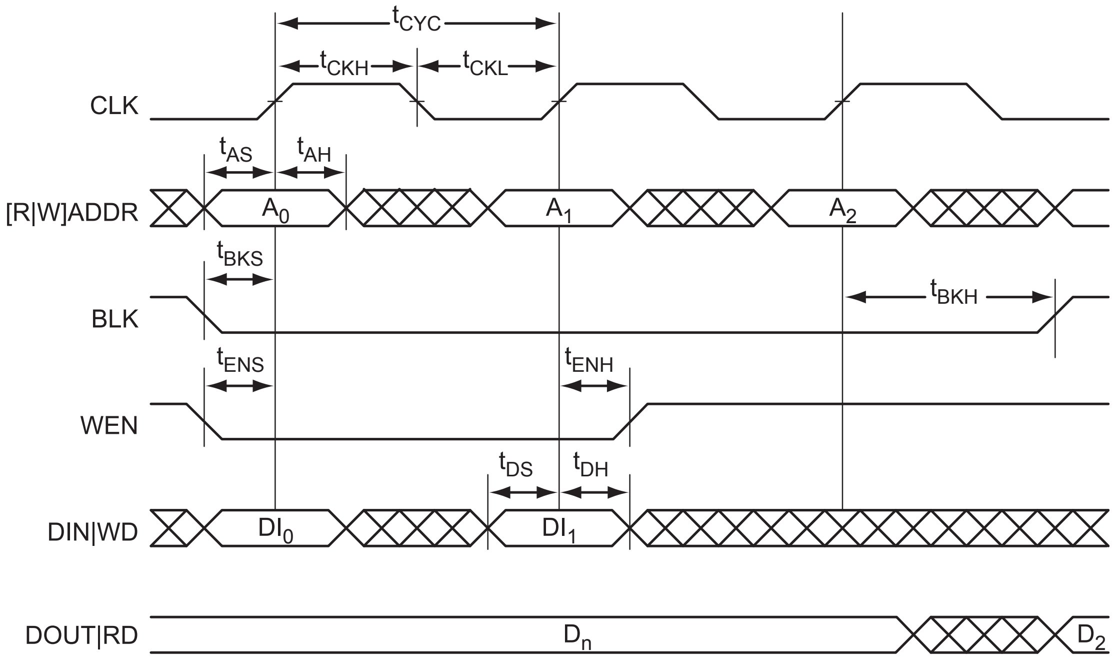

***Figure 2-52* • RAM Write, Output Retained. Applicable to both RAM4K9 and RAM512x18.**

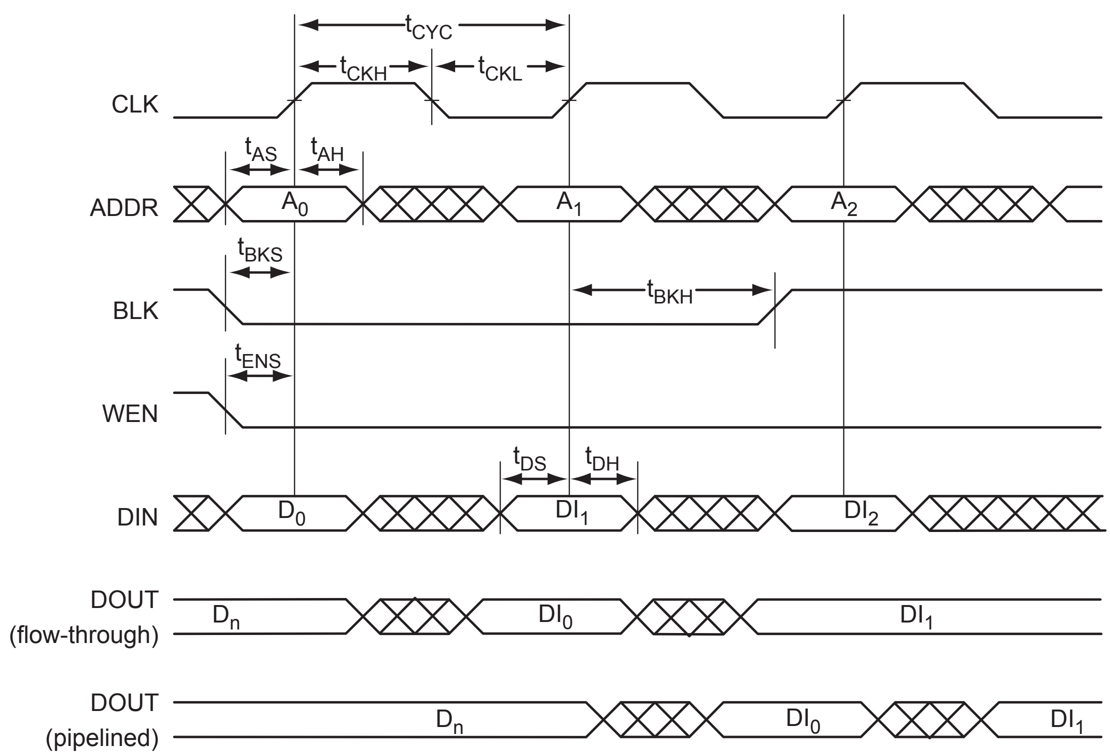

***Figure 2-53* • RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 Only.**

Offset Error

Offset error indicates how well the actual transfer function matches the ideal transfer function at a single point. For an ideal ADC, the first transition occurs at 0.5 LSB above zero. The offset voltage is measured by applying an analog input such that the ADC outputs all zeroes and increases until the first transition occurs (Figure 2-86).

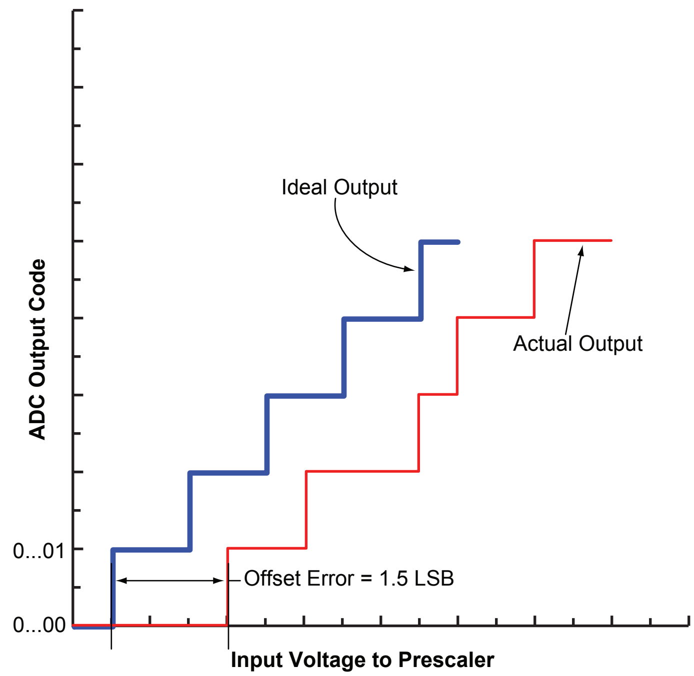

Figure 2-86 • **Offset Error**

Resolution

ADC resolution is the number of bits used to represent an analog input signal. To more accurately replicate the analog signal, resolution needs to be increased.

Sampling Rate

Sampling rate or sample frequency, specified in samples per second (sps), is the rate at which an ADC acquires (samples) the analog input.

SNR – Signal-to-Noise Ratio

SNR is the ratio of the amplitude of the desired signal to the amplitude of the noise signals at a given point in time. For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR (EQ 14) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum ADC noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB[MAX]} = 6.02_{dB} \times N + 1.76_{dB}$$

EQ 14

SINAD – Signal-to-Noise and Distortion

SINAD is the ratio of the rms amplitude to the mean value of the root-sum-square of the all other spectral components, including harmonics, but excluding DC. SINAD is a good indication of the overall dynamic performance of an ADC because it includes all components which make up noise and distortion.

Total Harmonic Distortion

THD measures the distortion content of a signal, and is specified in decibels relative to the carrier (dBc). THD is the ratio of the RMS sum of the selected harmonics of the input signal to the fundamental itself. Only harmonics within the Nyquist limit are included in the measurement.

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

**Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions
Applicable to Pro I/Os**

I/O Standard	Drive Strength	Slew Rate	VIL Min. V	VIL Max. V	VIH Min. V	VIH Max. V	VOL Max. V	VOH Min. V	IOL mA	IOH mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI Specification									
3.3 V PCI-X	Per PCI-X Specification									
3.3 V GTL	20 mA[2]	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
2.5 V GTL	20 mA[2]	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
3.3 V GTL+	35 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35
2.5 V GTL+	33 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33
HSTL (I)	8 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8
HSTL (II)	15 mA[2]	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15
SSTL2 (I)	15 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15
SSTL2 (II)	18 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18
SSTL3 (I)	14 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14
SSTL3 (II)	21 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *Output drive strength is below JEDEC specification.*
3. *Output slew rate can be extracted by the IBIS models.*

**Table 2-87 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions
Applicable to Advanced I/Os**

I/O Standard	Drive Strength	Slew Rate	VIL Min. V	VIL Max. V	VIH Min. V	VIH Max. V	VOL Max. V	VOH Min. V	IOL mA	IOH mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Note: Currents are measured at 85°C junction temperature.

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-90 • **Summary of AC Measuring Points Applicable to All I/O Bank Types**

Standard	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_REF)	Measuring Trip Point (Vtrip)
3.3 V LVTTL / 3.3 V LVCMOS	–	–	1.4 V
2.5 V LVCMOS	–	–	1.2 V
1.8 V LVCMOS	–	–	0.90 V
1.5 V LVCMOS	–	–	0.75 V
3.3 V PCI	–	–	0.285 * VCCI (RR) 0.615 * VCCI (FF))
3.3 V PCI-X	–	–	0.285 * VCCI (RR) 0.615 * VCCI (FF)
3.3 V GTL	0.8 V	1.2 V	VREF
2.5 V GTL	0.8 V	1.2 V	VREF
3.3 V GTL+	1.0 V	1.5 V	VREF
2.5 V GTL+	1.0 V	1.5 V	VREF
HSTL (I)	0.75 V	0.75 V	VREF
HSTL (II)	0.75 V	0.75 V	VREF
SSTL2 (I)	1.25 V	1.25 V	VREF
SSTL2 (II)	1.25 V	1.25 V	VREF
SSTL3 (I)	1.5 V	1.485 V	VREF
SSTL3 (II)	1.5 V	1.485 V	VREF
LVDS	–	–	Cross point
LVPECL	–	–	Cross point

Table 2-91 • **I/O AC Parameter Definitions**

Parameter	Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer with Schmitt trigger disabled
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{PYS}	Pad to Data delay through the Input Buffer with Schmitt trigger enabled
t_{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

***Table 2-98* • I/O Short Currents IOSH/IOSL**

	Drive Strength	IOSH (mA)*	IOSL (mA)*
Applicable to Pro I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
Applicable to Advanced I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181

Note: *T_J = 100°C*

***Table 2-99* • Short Current Event Duration before Failure**

Temperature	Time Before Failure
–40°C	>20 years
0°C	>20 years
25°C	>20 years
70°C	5 years
85°C	2 years
100°C	6 months

***Table 2-100* • Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (typ.) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typ.)
3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

***Table 2-101* • I/O Input Rise Time, Fall Time, and Related I/O Reliability**

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns*	20 years (100°C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis	20 years (100°C)
HSTL/SSTL/GTL	No requirement	10 ns*	10 years (100°C)
LVDS/BLVDS/M-LVDS/LVPECL	No requirement	10 ns*	10 years (100°C)

*Note: * The maximum input rise/fall time is related only to the noise induced into the input buffer trace. If the noise is low, the rise time and fall time of input buffers, when Schmitt trigger is disabled, can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure there is no excessive noise coupling into input signals.*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTL support.

***Table 2-102* • Minimum and Maximum DC Input and Output Levels**

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
Applicable to Pro I/O Banks												
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10
Applicable to Advanced I/O Banks												
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10
Applicable to Standard I/O Banks												
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

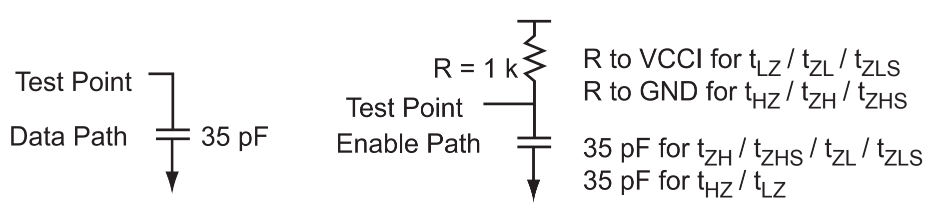

***Figure 2-119* • AC Loading**

Table 2-107 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	7.66	0.04	1.20	0.43	7.80	6.59	2.65	2.61	10.03	8.82	ns
	–1	0.56	6.51	0.04	1.02	0.36	6.63	5.60	2.25	2.22	8.54	7.51	ns
	–2	0.49	5.72	0.03	0.90	0.32	5.82	4.92	1.98	1.95	7.49	6.59	ns
8 mA	Std.	0.66	4.91	0.04	1.20	0.43	5.00	4.07	2.99	3.20	7.23	6.31	ns
	–1	0.56	4.17	0.04	1.02	0.36	4.25	3.46	2.54	2.73	6.15	5.36	ns
	–2	0.49	3.66	0.03	0.90	0.32	3.73	3.04	2.23	2.39	5.40	4.71	ns
12 mA	Std.	0.66	3.53	0.04	1.20	0.43	3.60	2.82	3.21	3.58	5.83	5.06	ns
	–1	0.56	3.00	0.04	1.02	0.36	3.06	2.40	2.73	3.05	4.96	4.30	ns
	–2	0.49	2.64	0.03	0.90	0.32	2.69	2.11	2.40	2.68	4.36	3.78	ns
16 mA	Std.	0.66	3.33	0.04	1.20	0.43	3.39	2.56	3.26	3.68	5.63	4.80	ns
	–1	0.56	2.83	0.04	1.02	0.36	2.89	2.18	2.77	3.13	4.79	4.08	ns
	–2	0.49	2.49	0.03	0.90	0.32	2.53	1.91	2.44	2.75	4.20	3.58	ns
24 mA	Std.	0.66	3.08	0.04	1.20	0.43	3.13	2.12	3.32	4.06	5.37	4.35	ns
	–1	0.56	2.62	0.04	1.02	0.36	2.66	1.80	2.83	3.45	4.57	3.70	ns
	–2	0.49	2.30	0.03	0.90	0.32	2.34	1.58	2.48	3.03	4.01	3.25	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-108 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	9.46	0.04	1.00	0.43	9.64	8.54	2.07	2.04	ns
	–1	0.56	8.05	0.04	0.85	0.36	8.20	7.27	1.76	1.73	ns
	–2	0.49	7.07	0.03	0.75	0.32	7.20	6.38	1.55	1.52	ns
4 mA	Std.	0.66	9.46	0.04	1.00	0.43	9.64	8.54	2.07	2.04	ns
	–1	0.56	8.05	0.04	0.85	0.36	8.20	7.27	1.76	1.73	ns
	–2	0.49	7.07	0.03	0.75	0.32	7.20	6.38	1.55	1.52	ns
6 mA	Std.	0.66	6.57	0.04	1.00	0.43	6.69	5.98	2.40	2.57	ns
	–1	0.56	5.59	0.04	0.85	0.36	5.69	5.09	2.04	2.19	ns
	–2	0.49	4.91	0.03	0.75	0.32	5.00	4.47	1.79	1.92	ns
8 mA	Std.	0.66	6.57	0.04	1.00	0.43	6.69	5.98	2.40	2.57	ns
	–1	0.56	5.59	0.04	0.85	0.36	5.69	5.09	2.04	2.19	ns
	–2	0.49	4.91	0.03	0.75	0.32	5.00	4.47	1.79	1.92	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

***Table 2-121* • 1.8 V LVCMOS High Slew**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Pro I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	12.10	0.04	1.45	1.91	0.43	9.59	12.10	2.78	1.64	11.83	14.34	ns
	–1	0.56	10.30	0.04	1.23	1.62	0.36	8.16	10.30	2.37	1.39	10.06	12.20	ns
	–2	0.49	9.04	0.03	1.08	1.42	0.32	7.16	9.04	2.08	1.22	8.83	10.71	ns
4 mA	Std.	0.66	7.05	0.04	1.45	1.91	0.43	6.20	7.05	3.25	2.86	8.44	9.29	ns
	–1	0.56	6.00	0.04	1.23	1.62	0.36	5.28	6.00	2.76	2.44	7.18	7.90	ns
	–2	0.49	5.27	0.03	1.08	1.42	0.32	4.63	5.27	2.43	2.14	6.30	6.94	ns
8 mA	Std.	0.66	4.52	0.04	1.45	1.91	0.43	4.47	4.52	3.57	3.47	6.70	6.76	ns
	–1	0.56	3.85	0.04	1.23	1.62	0.36	3.80	3.85	3.04	2.95	5.70	5.75	ns
	–2	0.49	3.38	0.03	1.08	1.42	0.32	3.33	3.38	2.66	2.59	5.00	5.05	ns
12 mA	Std.	0.66	4.12	0.04	1.45	1.91	0.43	4.20	3.99	3.63	3.62	6.43	6.23	ns
	–1	0.56	3.51	0.04	1.23	1.62	0.36	3.57	3.40	3.09	3.08	5.47	5.30	ns
	–2	0.49	3.08	0.03	1.08	1.42	0.32	3.14	2.98	2.71	2.71	4.81	4.65	ns
16 mA	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	–1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	–2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

***Table 2-144* • Minimum and Maximum DC Input and Output Levels**

3.3 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	μA[4]	μA[4]
35 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35	181	268	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

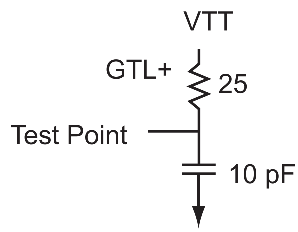

***Figure 2-126* • AC Loading**

***Table 2-145* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

***Table 2-146* • 3.3 V GTL+**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.06	0.04	1.59	0.43	2.09	2.06			4.33	4.29	ns
–1	0.56	1.75	0.04	1.35	0.36	1.78	1.75			3.68	3.65	ns
–2	0.49	1.53	0.03	1.19	0.32	1.56	1.53			3.23	3.20	ns

Note: *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

Example of Power Calculation

This example considers a shift register with 5,000 storage tiles, including a counter and memory that stores analog information. The shift register is clocked at 50 MHz and stores and reads information from a RAM.

The device used is a commercial AFS600 device operating in typical conditions.

The calculation below uses the power calculation methodology previously presented and shows how to determine the dynamic and static power consumption of resources used in the application.

Also included in the example is the calculation of power consumption in operating, standby, and sleep modes to illustrate the benefit of power-saving modes.

Global Clock Contribution—P_{CLOCK}

F_{CLK} = 50 MHz

Number of sequential VersaTiles: $N_{S\text{-}CELL}$ = 5,000

Estimated number of Spines: N_{SPINES} = 5

Estimated number of Rows: N_{ROW} = 313

Operating Mode

$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$

$P_{CLOCK} = (0.0128 + 5 * 0.0019 + 313 * 0.00081 + 5{,}000 * 0.00011) * 50$

P_{CLOCK} = 41.28 mW

Standby Mode and Sleep Mode

P_{CLOCK} = 0 W

Logic—Sequential Cells, Combinational Cells, and Routing Net Contributions—$P_{S\text{-}CELL}$, $P_{C\text{-}CELL}$, and P_{NET}

F_{CLK} = 50 MHz

Number of sequential VersaTiles: $N_{S\text{-}CELL}$ = 5,000

Number of combinatorial VersaTiles: $N_{C\text{-}CELL}$ = 6,000

Estimated toggle rate of VersaTile outputs: α_1 = 0.1 (10%)

Operating Mode

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + (\alpha_1 / 2) * PAC6) * F_{CLK}$

$P_{S\text{-}CELL} = 5{,}000 * (0.00007 + (0.1 / 2) * 0.00029) * 50$

$P_{S\text{-}CELL}$ = 21.13 mW

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * (\alpha_1 / 2) * PAC7 * F_{CLK}$

$P_{C\text{-}CELL} = 6{,}000 * (0.1 / 2) * 0.00029 * 50$

$P_{C\text{-}CELL}$ = 4.35 mW

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * (\alpha_1 / 2) * PAC8 * F_{CLK}$

$P_{NET} = (5{,}000 + 6{,}000) * (0.1 / 2) * 0.0007 * 50$

P_{NET} = 19.25 mW

$P_{LOGIC} = P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET}$

P_{LOGIC} = 21.13 mW + 4.35 mW + 19.25 mW

P_{LOGIC} = 44.73 mW

Standby Mode and Sleep Mode

QN180		
Pin Number	AFS090 Function	AFS250 Function
A1	GNDQ	GNDQ
A2	VCCIB3	VCCIB3
A3	GAB2/IO52NDB3V0	IO74NDB3V0
A4	GFA2/IO51NDB3V0	IO71NDB3V0
A5	GFC2/IO50NDB3V0	IO69NPB3V0
A6	VCCIB3	VCCIB3
A7	GFA1/IO47PPB3V0	GFB1/IO67PPB3V0
A8	GEB0/IO45NDB3V0	NC
A9	XTAL1	XTAL1
A10	GNDOSC	GNDOSC
A11	GEC2/IO43PPB3V0	GEA1/IO61PPB3V0
A12	IO43NPB3V0	GEA0/IO61NPB3V0
A13	NC	VCCIB3
A14	GNDNVM	GNDNVM
A15	PCAP	PCAP
A16	VCC33PMP	VCC33PMP
A17	NC	NC
A18	AV0	AV0
A19	AG0	AG0
A20	ATRTN0	ATRTN0
A21	AG1	AG1
A22	AC1	AC1
A23	AV2	AV2
A24	AT2	AT2
A25	AT3	AT3
A26	AC3	AC3
A27	AV4	AV4
A28	AC4	AC4
A29	AT4	AT4
A30	NC	AG5
A31	NC	AV5
A32	ADCGNDREF	ADCGNDREF
A33	VCC33A	VCC33A
A34	GNDA	GNDA
A35	PTBASE	PTBASE
A36	VCCNVM	VCCNVM

QN180		
Pin Number	AFS090 Function	AFS250 Function
A37	VPUMP	VPUMP
A38	TDI	TDI
A39	TDO	TDO
A40	VJTAG	VJTAG
A41	GDB1/IO39PPB1V0	GDA1/IO54PPB1V0
A42	GDC1/IO38PDB1V0	GDB1/IO53PDB1V0
A43	VCC	VCC
A44	GCB0/IO35NPB1V0	GCB0/IO48NPB1V0
A45	GCC1/IO34PDB1V0	GCC1/IO47PDB1V0
A46	VCCIB1	VCCIB1
A47	GBC2/IO32PPB1V0	GBB2/IO41PPB1V0
A48	VCCIB1	VCCIB1
A49	NC	NC
A50	GBA0/IO29RSB0V0	GBB1/IO37RSB0V0
A51	VCCIB0	VCCIB0
A52	GBB0/IO27RSB0V0	GBC0/IO34RSB0V0
A53	GBC1/IO26RSB0V0	IO33RSB0V0
A54	IO24RSB0V0	IO29RSB0V0
A55	IO21RSB0V0	IO26RSB0V0
A56	VCCIB0	VCCIB0
A57	IO15RSB0V0	IO21RSB0V0
A58	IO10RSB0V0	IO13RSB0V0
A59	IO07RSB0V0	IO10RSB0V0
A60	GAC0/IO04RSB0V0	IO06RSB0V0
A61	GAB1/IO03RSB0V0	GAC1/IO05RSB0V0
A62	VCC	VCC
A63	GAA1/IO01RSB0V0	GAB0/IO02RSB0V0
A64	NC	NC
B1	VCOMPLA	VCOMPLA
B2	GAA2/IO52PDB3V0	GAC2/IO74PDB3V0
B3	GAC2/IO51PDB3V0	GFA2/IO71PDB3V0
B4	GFB2/IO50PDB3V0	GFB2/IO70PSB3V0
B5	VCC	VCC
B6	GFC0/IO49NDB3V0	GFC0/IO68NDB3V0
B7	GEB1/IO45PDB3V0	NC
B8	VCCOSC	VCCOSC

FG256				
Pin Number	**AFS090 Function**	**AFS250 Function**	**AFS600 Function**	**AFS1500 Function**
M15	TRST	TRST	TRST	TRST
M16	GND	GND	GND	GND
N1	GEB2/IO42PDB3V0	GEB2/IO59PDB3V0	GEB2/IO59PDB4V0	GEB2/IO86PDB4V0
N2	GEA2/IO42NDB3V0	IO59NDB3V0	IO59NDB4V0	IO86NDB4V0
N3	NC	GEA2/IO58PPB3V0	GEA2/IO58PPB4V0	GEA2/IO85PPB4V0
N4	VCC33PMP	VCC33PMP	VCC33PMP	VCC33PMP
N5	VCC15A	VCC15A	VCC15A	VCC15A
N6	NC	NC	AG0	AG0
N7	AC1	AC1	AC3	AC3
N8	AG3	AG3	AG5	AG5
N9	AV3	AV3	AV5	AV5
N10	AG4	AG4	AG6	AG6
N11	NC	NC	AC8	AC8
N12	GNDA	GNDA	GNDA	GNDA
N13	VCC33A	VCC33A	VCC33A	VCC33A
N14	VCCNVM	VCCNVM	VCCNVM	VCCNVM
N15	TCK	TCK	TCK	TCK
N16	TDI	TDI	TDI	TDI
P1	VCCNVM	VCCNVM	VCCNVM	VCCNVM
P2	GNDNVM	GNDNVM	GNDNVM	GNDNVM
P3	GNDA	GNDA	GNDA	GNDA
P4	NC	NC	AC0	AC0
P5	NC	NC	AG1	AG1
P6	NC	NC	AV1	AV1
P7	AG0	AG0	AG2	AG2
P8	AG2	AG2	AG4	AG4
P9	GNDA	GNDA	GNDA	GNDA
P10	NC	AC5	AC7	AC7
P11	NC	NC	AV8	AV8
P12	NC	NC	AG8	AG8
P13	NC	NC	AV9	AV9
P14	ADCGNDREF	ADCGNDREF	ADCGNDREF	ADCGNDREF
P15	PTBASE	PTBASE	PTBASE	PTBASE
P16	GNDNVM	GNDNVM	GNDNVM	GNDNVM
R1	VCCIB3	VCCIB3	VCCIB4	VCCIB4
R2	PCAP	PCAP	PCAP	PCAP
R3	NC	NC	AT1	AT1
R4	NC	NC	AT0	AT0

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the Fusion datasheet.

Revision	Changes	Page
Revision 6 (March 2014)	Note added for the discontinuance of QN108 and QN180 packages to the "Package I/Os: Single-/Double-Ended (Analog)" table and the "Temperature Grade Offerings" table (SAR 55113, PDN 1306).	II and IV
	Updated details about page programming time in the "Program Operation" section (SAR 49291).	2-46
	ADC_START changed to ADCSTART in the "ADC Operation" section (SAR 44104).	2-104
Revision 5 (January 2014)	Calibrated offset values (AFS090, AFS250) of the external temperature monitor in Table 2-49 • Analog Channel Specifications have been updated (SAR 51464).	2-117
	Specifications for the internal temperature monitor in Table 2-49 • Analog Channel Specifications have been updated (SAR 50870).	2-117
Revision 4 (January 2013)	The "Product Ordering Codes" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43177).	III
	The note in Table 2-12 • Fusion CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42563).	2-28
	Table 2-49 • Analog Channel Specifications was modified to update the uncalibrated offset values (AFS250) of the external and internal temperature monitors (SAR 43134).	2-117
	In Table 2-57 • Prescaler Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3), changed the column heading from 'Full-Scale Voltage' to 'Full Scale Voltage in 10-Bit Mode', and added and updated Notes as required (SAR 20812).	2-130
	The values for the Speed Grade (-1 and Std.) for FDDRIMAX (Table 2-180 • Input DDR Propagation Delays) and values for the Speed Grade (-2 and Std.) for FDDOMAX (Table 2-182 • Output DDR Propagation Delays) had been inadvertently interchanged. This has been rectified (SAR 38514).	2-220, 2-222
	Added description about what happens if a user connects VAREF to an external 3.3 V on their board to the "VAREF Analog Reference Voltage" section (SAR 35188).	2-225
	Added a note to Table 3-2 • Recommended Operating Conditions1 (SAR 43429): The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.	3-3
	Added the Package Thermal details for AFS600-PQ208 and AFS250-PQ208 to Table 3-6 • Package Thermal Resistance (SAR 37816). Deleted the Die Size column from the table (SAR 43503).	3-7
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 42495). Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 3 (August 2012)	Microblade U1AFS250 and U1AFS1500 devices were added to the product tables.	I – IV
	A sentence pertaining to the analog I/Os was added to the "Specifying I/O States During Programming" section (SAR 34831).	1-9

Revision	Changes	Page
Advance v1.5 (continued)	This bullet was added to the "Integrated A/D Converter (ADC) and Analog I/O" section: ADC Accuracy is Better than 1%	I
	In the "Integrated Analog Blocks and Analog I/Os" section, ±4 LSB was changed to 0.72. The following sentence was deleted: The input range for voltage signals is from –12 V to +12 V with full-scale output values from 0.125 V to 16 V. In addition, 2°C was changed to 3°C: "One analog input in each quad can be connected to an external temperature monitor diode and achieves detection accuracy of ±3ºC." The following sentence was deleted: The input range for voltage signals is from –12 V to +12 V with full-scale output values from 0.125 V to 16 V.	1-4
	The title of the datasheet changed from Actel Programmable System Chips to Actel Fusion Mixed Signal FPGAs. In addition, all instances of programmable system chip were changed to mixed signal FPGA.	N/A
Advance v1.4 (July 2008)	In Table 3-8 · Quiescent Supply Current Characteristics (IDDQ)1, footnote references were updated for I_{DC2} and I_{DC3}. Footnote 3 and 4 were updated and footnote 5 is new.	3-11
Advance v1.3 (July 2008)	The "ADC Description" section was significantly updated. Please review carefully.	2-102
Advance v1.2 (May 2008)	Table 2-25 • Flash Memory Block Timing was significantly updated.	2-55
	The "V_{AREF} Analog Reference Voltage" pin description section was significantly update. Please review it carefully.	2-226
	Table 2-45 • ADC Interface Timing was significantly updated.	2-110
	Table 2-56 • Direct Analog Input Switch Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3) was significantly updated.	2-131
	The following sentence was deleted from the "Voltage Monitor" section: The Analog Quad inputs are tolerant up to 12 V + 10%.	2-86
	The "180-Pin QFN" figure was updated. D1 to D4 are new and the figure was changed to bottom view. The note below the figure is new.	3-3
Advance v1.1 (May 2008)	The following text was incorrect and therefore deleted: **VCC33A** **Analog Power Filter** Analog power pin for the analog power supply low-pass filter. An external 100 pF capacitor should be connected between this pin and ground. There is still a description of V_{CC33A} on page 2-224.	2-204