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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	223
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs1500-2fgg484

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Fusion Device Family Overview

With Fusion, Microsemi also introduces the Analog Quad I/O structure (Figure 1-1). Each quad consists of three analog inputs and one gate driver. Each quad can be configured in various built-in circuit combinations, such as three prescaler circuits, three digital input circuits, a current monitor circuit, or a temperature monitor circuit. Each prescaler has multiple scaling factors programmed by FPGA signals to support a large range of analog inputs with positive or negative polarity. When the current monitor circuit is selected, two adjacent analog inputs measure the voltage drop across a small external sense resistor. For more information, refer to the "Analog System Characteristics" section on page 2-117. Built-in operational amplifiers amplify small voltage signals for accurate current measurement. One analog input in each quad can be connected to an external temperature monitor diode. In addition to the external temperature monitor diode(s), a Fusion device can monitor an internal temperature diode using dedicated channel 31 of the ADCMUX.

Figure 1-1 on page 1-5 illustrates a typical use of the Analog Quad I/O structure. The Analog Quad shown is configured to monitor and control an external power supply. The AV pad measures the source of the power supply. The AC pad measures the voltage drop across an external sense resistor to calculate current. The AG MOSFET gate driver pad turns the external MOSFET on and off. The AT pad measures the load-side voltage level.



Figure 1-1 • Analog Quad



Fusion Device Family Overview

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

The I/Os are controlled by the JTAG Boundary Scan register during programming, except for the analog pins (AC, AT and AV). The Boundary Scan register of the AG pin can be used to enable/disable the gate driver in software v9.0.

- 1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
- 2. From the FlashPro GUI, click **PDB Configuration**. A FlashPoint Programming File Generator window appears.
- Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
- 4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-3).
- Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

1 - I/O is set to drive out logic High

0 – I/O is set to drive out logic Low

Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

Z -Tri-State: I/O is tristated

Port Name	Macro Cell	Pin Number	1/O State (Output Only)
BIST	ADLIB:INBUF	T2	1
BYPASS_IO	ADLIB:INBUF	К1	1
CLK	ADLIB:INBUF	B1	1
ENOUT	ADLIB:INBUF	J16	1
LED	ADLIB:OUTBUF	M3	0
MONITOR[0]	ADLIB:OUTBUF	B5	0
MONITOR[1]	ADLIB:OUTBUF	C7	Z
MONITOR[2]	ADLIB:OUTBUF	D9	Z
MONITOR[3]	ADLIB:OUTBUF	D7	Z
MONITOR[4]	ADLIB:OUTBUF	A11	Z
OEa	ADLIB:INBUF	E4	Z
OEb	ADLIB:INBUF	F1	Z
OSC_EN	ADLIB:INBUF	К3	Z
PAD[10]	ADLIB:BIBUF_LVCMOS33U	M8	Z
PAD[11]	ADLIB:BIBUF_LVCMOS33D	B7	Z
PAD[12]	ADLIB:BIBUF_LVCMOS33U	D11	Z
PAD[13]	ADLIB:BIBUF_LVCMOS33D	C12	Z
PAD[14]	ADLIB:BIBUF LVCMOS33U	B6	7

Figure 1-3 • I/O States During Programming Window

6. Click **OK** to return to the FlashPoint – Programming File Generator window.

I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.



Table 2-7 • AFS250 Global Resource Timing
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	_	·2	-	-1	St	Unite	
	Description	Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Ginta
t _{RCKL}	Input Low Delay for Global Clock	0.89	1.12	1.02	1.27	1.20	1.50	ns
t _{RCKH}	Input High Delay for Global Clock	0.88	1.14	1.00	1.30	1.17	1.53	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock							ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock							ns
t _{RCKSW}	Maximum Skew for Global Clock		0.26		0.30		0.35	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-8 • AFS090 Global Resource Timing

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-	2	-	1	S	Unite	
	Description	Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	0.84	1.07	0.96	1.21	1.13	1.43	ns
t _{RCKH}	Input High Delay for Global Clock	0.83	1.10	0.95	1.25	1.12	1.47	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock							ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock							ns
t _{RCKSW}	Maximum Skew for Global Clock		0.27		0.30		0.36	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Read Operation

Read operations are designed to read data from the FB Array, Page Buffer, Block Buffer, or status registers. Read operations support a normal read and a read-ahead mode (done by asserting READNEXT). Also, the timing for Read operations is dependent on the setting of PIPE.

The following diagrams illustrate representative timing for Non-Pipe Mode (Figure 2-38) and Pipe Mode (Figure 2-39) reads of the flash memory block interface.



Figure 2-38 • Read Waveform (Non-Pipe Mode, 32-bit access)



Figure 2-39 • Read Waveform (Pipe Mode, 32-bit access)



Timing Characteristics

Table 2-35 • FIFO

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{ENS}	REN, WEN Setup time	1.34	1.52	1.79	ns
t _{ENH}	REN, WEN Hold time	0.00	0.00	0.00	ns
t _{BKS}	BLK Setup time	0.19	0.22	0.26	ns
t _{вкн}	BLK Hold time	0.00	0.00	0.00	ns
t _{DS}	Input data (WD) Setup time	0.18	0.21	0.25	ns
t _{DH}	Input data (WD) Hold time	0.00	0.00	0.00	ns
t _{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.17	2.47	2.90	ns
t _{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.94	1.07	1.26	ns
t _{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t _{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t _{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t _{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t _{RSTAF}	RESET Low to Almost-Empty/Full Flag Valid	6.13	6.98	8.20	ns
+	RESET Low to Data out Low on RD (flow-through)	0.92	1.05	1.23	ns
^I RSTBQ	RESET Low to Data out Low on RD (pipelined)	0.92	1.05	1.23	ns
t _{REMRSTB}	RESET Removal	0.29	0.33	0.38	ns
t _{RECRSTB}	RESET Recovery	1.50	1.71	2.01	ns
t _{MPWRSTB}	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t _{CYC}	Clock Cycle time	3.23	3.68	4.32	ns
F _{MAX}	Maximum Frequency for FIFO	310	272	231	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



To initiate a current measurement, the appropriate Current Monitor Strobe (CMSTB) signal on the AB macro must be asserted low for at least t_{CMSLO} in order to discharge the previous measurement. Then CMSTB must be asserted high for at least t_{CMSET} prior to asserting the ADCSTART signal. The CMSTB must remain high until after the SAMPLE signal is de-asserted by the AB macro. Note that the minimum sample time cannot be less than t_{CMSHI} . Figure 2-71 shows the timing diagram of CMSTB in relationship with the ADC control signals.



Figure 2-71 • Timing Diagram for Current Monitor Strobe

Figure 2-72 illustrates positive current monitor operation. The differential voltage between AV and AC goes into the 10× amplifier and is then converted by the ADC. For example, a current of 1.5 A is drawn from a 10 V supply and is measured by the voltage drop across a 0.050 Ω sense resistor, The voltage drop is amplified by ten times by the amplifier and then measured by the ADC. The 1.5 A current creates a differential voltage across the sense resistor of 75 mV. This becomes 750 mV after amplification. Thus, the ADC measures a current of 1.5 A as 750 mV. Using an ADC with 8-bit resolution and VAREF of 2.56 V, the ADC result is decimal 75. EQ 3 shows how to compute the current from the ADC result.

$$||| = (ADC \times V_{AREF}) / (10 \times 2^{N} \times R_{sense})$$

EQ 3

where

I is the current flowing through the sense resistor

ADC is the result from the ADC

VAREF is the Reference voltage

N is the number of bits

Rsense is the resistance of the sense resistor



Fusion uses a remote diode as a temperature sensor. The Fusion Temperature Monitor uses a differential input; the AT pin and ATRTN (AT Return) pin are the differential inputs to the Temperature Monitor. There is one Temperature Monitor in each Quad. A simplified block diagram is shown in Figure 2-77.



Figure 2-77 • Block Diagram for Temperature Monitor Circuit

The Fusion approach to measuring temperature is forcing two different currents through the diode with a ratio of 10:1. The switch that controls the different currents is controlled by the Temperature Monitor Strobe signal, TMSTB. Setting TMSTB to '1' will initiate a Temperature reading. The TMSTB should remain '1' until the ADC finishes sampling the voltage from the Temperature Monitor. The minimum sample time for the Temperature Monitor cannot be less than the minimum strobe high time minus the setup time. Figure 2-78 shows the timing diagram.





Note: When the IEEE 1149.1 Boundary Scan EXTEST instruction is executed, the AG pad drive strength ceases and becomes a 1 µA sink into the Fusion device.



EQ 16 through EQ 18 can be used to calculate the acquisition time required for a given input. The STC signal gives the number of sample periods in ADCCLK for the acquisition time of the desired signal. If the actual acquisition time is higher than the STC value, the settling time error can affect the accuracy of the ADC, because the sampling capacitor is only partially charged within the given sampling cycle. Example acquisition times are given in Table 2-44 and Table 2-45. When controlling the sample time for the ADC along with the use of the active bipolar prescaler, current monitor, or temperature monitor, the minimum sample time(s) for each must be obeyed. EQ 19 can be used to determine the appropriate value of STC.

You can calculate the minimum actual acquisition time by using EQ 16:

EQ 16

EQ 17

For 0.5 LSB gain error, VOUT should be replaced with (VIN –(0.5 × LSB Value)): (VIN – 0.5 × LSB Value) = VIN(1 – $e^{-t/RC}$)

$$1 - e^{-e^{-1}}$$

Solving EQ 17:

EQ 18

where $R = Z_{INAD} + R_{SOURCE}$ and $C = C_{INAD}$. Calculate the value of STC by using EQ 19.

t_{SAMPLE} = (2 + STC) x (1 / ADCCLK) or t_{SAMPLE} = (2 + STC) x (ADC Clock Period)

EQ 19

where ADCCLK = ADC clock frequency in MHz.

where VIN is the ADC reference voltage (VREF)

 t_{SAMPLE} = 0.449 µs from bit resolution in Table 2-44.

ADC Clock frequency = 10 MHz or a 100 ns period.

STC = (t_{SAMPLE} / (1 / 10 MHz)) - 2 = 4.49 - 2 = 2.49.

You must round up to 3 to accommodate the minimum sample time.

Table 2-44 • Acquisition Time Example with VAREF = 2.56 V

	VIN = 2.56V, R = 4K (R _{SOURCE} ~ 0), C = 18 pF										
Resolution	LSB Value (mV)	Min. Sample/Hold Time for 0.5 LSB (μs)									
8	10	0.449									
10	2.5	0.549									
12	0.625	0.649									

|--|

VIN = 3.3V, R = 4K (R _{SOURCE} ~ 0), C = 18 pF										
Resolution	LSB Value (mV)	Min. Sample/Hold time for 0.5 LSB (µs)								
8	12.891	0.449								
10	3.223	0.549								
12	0.806	0.649								

Sample Phase

A conversion is performed in three phases. In the first phase, the analog input voltage is sampled on the input capacitor. This phase is called sample phase. During the sample phase, the output signals BUSY and SAMPLE change from '0' to '1', indicating the ADC is busy and sampling the analog signal. The sample time can be controlled by input signals STC[7:0]. The sample time can be calculated by EQ 20. When controlling the sample time for the ADC along with the use of Prescaler or Current Monitor or Temperature Monitor, the minimum sample time for each must be obeyed.



Intra-Conversion



Note: **t*_{CONV} represents the conversion time of the second conversion. See EQ 23 on page 2-109 for calculation of the conversion time, *t*_{CONV}.

Figure 2-92 • Intra-Conversion Timing Diagram



Injected Conversion

Note: *See EQ 23 on page 2-109 for calculation on the conversion time, t_{CONV}.

Figure 2-93 • Injected Conversion Timing Diagram

User I/O Naming Convention

Due to the comprehensive and flexible nature of Fusion device user I/Os, a naming scheme is used to show the details of the I/O (Figure 2-113 on page 2-158 and Figure 2-114 on page 2-159). The name identifies to which I/O bank it belongs, as well as the pairing and pin polarity for differential I/Os.

I/O Nomenclature = Gmn/IOuxwByVz

Gmn is only used for I/Os that also have CCC access—i.e., global pins.

- G = Global
- m = Global pin location associated with each CCC on the device: A (northwest corner), B (northeast corner), C (east middle), D (southeast corner), E (southwest corner), and F (west middle).
- n = Global input MUX and pin number of the associated Global location m, either A0, A1, A2, B0, B1, B2, C0, C1, or C2. Figure 2-22 on page 2-25 shows the three input pins per clock source MUX at CCC location m.
- u = I/O pair number in the bank, starting at 00 from the northwest I/O bank and proceeding in a clockwise direction.
- x = P (Positive) or N (Negative) for differential pairs, or R (Regular single-ended) for the I/Os that support single-ended and voltage-referenced I/O standards only. U (Positive-LVDS only) or V (Negative-LVDS only) restrict the I/O differential pair from being selected as an LVPECL pair.
- w = D (Differential Pair), P (Pair), or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential (D) pairs, adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

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B = Bank
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- y = Bank number (0–3). The Bank number starts at 0 from the northwest I/O bank and proceeds in a clockwise direction.
- V = Reference voltage
- z = Minibank number



Standard I/O Bank

Figure 2-113 • Naming Conventions of Fusion Devices with Three Digital I/O Banks

Table 2-93 • Summary of I/O Timing Characteristics – Software Default SettingsCommercial Temperature Range Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V,Worst-Case VCCI = I/O Standard DependentApplicable to Advanced I/Os

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ohm)	tpour	top	toin	tey	teout	tzı	tzH	t _{LZ}	tHZ	tzıs	tzHS	Units
3.3 V LVTTL/ 3.3 V LVCMOS	12 mA	High	35 pF	-	0.49	2.64	0.03	0.90	0.32	2.69	2.11	2.40	2.68	4.36	3.78	ns
2.5 V LVCMOS	12 mA	High	35 pF	_	0.49	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns
1.8 V LVCMOS	12 mA	High	35 pF	_	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns
1.5 V LVCMOS	12 mA	High	35 pF	_	0.49	3.05	0.03	1.07	0.32	3.10	2.67	2.95	3.14	4.77	4.34	ns
3.3 V PCI	Per PCI spec	High	10 pF	25 ²	0.49	2.00	0.03	0.65	0.32	2.04	1.46	2.40	2.68	3.71	3.13	ns
3.3 V PCI-X	Per PCI-X spec	High	10 pF	25 ²	0.49	2.00	0.03	0.62	0.32	2.04	1.46	2.40	2.68	3.71	3.13	ns
LVDS	24 mA	High	_	-	0.49	1.37	0.03	1.20	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL	24 mA	High	-	_	0.49	1.34	0.03	1.05	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns

Notes:

1. For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-7 for derating values.

2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-123 on page 2-197 for connectivity. This resistor is not required during normal operation.

Table 2-94 • Summary of I/O Timing Characteristics – Software Default SettingsCommercial Temperature Range Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V,Worst-Case VCCI = I/O Standard DependentApplicable to Standard I/Os

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ohm)	tpour	t _{DP}	t _{DIN}	t _Þ v	teour	tzı	tzH	t _{LZ}	t _{HZ}	Units
3.3 V LVTTL/ 3.3 V LVCMOS	8 mA	High	35 pF	-	0.49	3.29	0.03	0.75	0.32	3.36	2.80	1.79	2.01	ns
2.5 V LVCMOS	8 mA	High	35pF	-	0.49	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns
1.8 V LVCMOS	4 mA	High	35pF	_	0.49	4.74	0.03	0.90	0.32	4.02	4.74	1.80	1.85	ns
1.5 V LVCMOS	2 mA	High	35pF	—	0.49	5.71	0.03	1.06	0.32	4.71	5.71	1.83	1.83	ns

Note: For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-7 for derating values.



Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer. The 3.3 V LVCMOS standard is supported as part of the 3.3 V LVTTL support.

Table 2-102	• Minimum	and Maximum	DC Input	and Output	l evels
10010 2-102	• Willing the second		DO inpui	and Output	. LEVEIJ

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	νон	IOL	ЮН	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
Applicable to P	ro I/O Ba	nks					•				•	
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	-0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	-0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	-0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10
Applicable to A	dvanced	I/O Bank	s									
2 mA	-0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	-0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	-0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	-0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	-0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10
Applicable to S	tandard I	/O Banks										
2 mA	-0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	-0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.



Figure 2-119 • AC Loading

Table 2-114 • 2.5 V LVCMOS Low Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V Applicable to Advanced I/Os

Drive Strength	Speed Grade	toour	top	toin	tev	teour	tzı	t≂⊔	tı z	tu-z	tzı e	tzue	Units
4 mA	Std.	0.66	11.40	0.04	1.31	0.43	11.22	- <u>г</u> н 11.40	2.68	2.20	13.45	13.63	ns
	-1	0.56	9.69	0.04	1.11	0.36	9.54	9.69	2.28	1.88	11.44	11.60	ns
	-2	0.49	8.51	0.03	0.98	0.32	8.38	8.51	2.00	1.65	10.05	10.18	ns
8 mA	Std.	0.66	7.96	0.04	1.31	0.43	8.11	7.81	3.05	2.89	10.34	10.05	ns
	-1	0.56	6.77	0.04	1.11	0.36	6.90	6.65	2.59	2.46	8.80	8.55	ns
	-2	0.49	5.94	0.03	0.98	0.32	6.05	5.84	2.28	2.16	7.72	7.50	ns
12 mA	Std.	0.66	6.18	0.04	1.31	0.43	6.29	5.92	3.30	3.32	8.53	8.15	ns
	-1	0.56	5.26	0.04	1.11	0.36	5.35	5.03	2.81	2.83	7.26	6.94	ns
	-2	0.49	4.61	0.03	0.98	0.32	4.70	4.42	2.47	2.48	6.37	6.09	ns
16 mA	Std.	0.66	6.18	0.04	1.31	0.43	6.29	5.92	3.30	3.32	8.53	8.15	ns
	-1	0.56	5.26	0.04	1.11	0.36	5.35	5.03	2.81	2.83	7.26	6.94	ns
	-2	0.49	4.61	0.03	0.98	0.32	4.70	4.42	2.47	2.48	6.37	6.09	ns
24 mA	Std.	0.66	6.18	0.04	1.31	0.43	6.29	5.92	3.30	3.32	8.53	8.15	ns
	-1	0.56	5.26	0.04	1.11	0.36	5.35	5.03	2.81	2.83	7.26	6.94	ns
	-2	0.49	4.61	0.03	0.98	0.32	4.70	4.42	2.47	2.48	6.37	6.09	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



Symbol	Parameter ²		Commercial	Industrial	Units
Τ _J	Junction temperature		0 to +85	-40 to +100	°C
VCC	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage	Programming mode ³	3.15 to 3.45	3.15 to 3.45	V
		Operation ⁴	0 to 3.6	0 to 3.6	V
VCCPLL	Analog power supply (PLL)		1.425 to 1.575	1.425 to 1.575	V
VCCI	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O	2.375 to 2.625	2.375 to 2.625	V	
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V
VCC33A	+3.3 V power supply	2.97 to 3.63	2.97 to 3.63	V	
VCC33PMP	+3.3 V power supply	2.97 to 3.63	2.97 to 3.63	V	
VAREF	Voltage reference for ADC	2.527 to 2.593	2.527 to 2.593	V	
VCC15A ⁵	Digital power supply for the analog	1.425 to 1.575	1.425 to 1.575	V	
VCCNVM	Embedded flash power supply	1.425 to 1.575	1.425 to 1.575	V	
VCCOSC	Oscillator power supply		2.97 to 3.63	2.97 to 3.63	V
AV, AC ⁶	Unpowered, ADC reset asserted or	unconfigured	-10.5 to 12.0	-10.5 to 11.6	V
	Analog input (+16 V to +2 V presca	ller range)	-0.3 to 12.0	–0.3 to 11.6	V
	Analog input (+1 V to + 0.125 V pre	escaler range)	-0.3 to 3.6	-0.3 to 3.6	V
	Analog input (–16 V to –2 V presca	ler range)	-10.5 to 0.3	-10.5 to 0.3	V
	Analog input (–1 V to –0.125 V pres	scaler range)	-3.6 to 0.3	-3.6 to 0.3	V
	Analog input (direct input to ADC)		-0.3 to 3.6	-0.3 to 3.6	V
	Digital input		-0.3 to 12.0	–0.3 to 11.6	V
AG ⁶	Unpowered, ADC reset asserted or	unconfigured	-10.5 to 12.0	-10.5 to 11.6	V
	Low Current Mode (1 µA, 3 µA, 10	μΑ, 30 μΑ)	-0.3 to 12.0	–0.3 to 11.6	V
	Low Current Mode (–1 µA, –3 µA, -	–10 μA, –30 μA)	-10.5 to 0.3	-10.5 to 0.3	V
	High Current Mode ⁷		-10.5 to 12.0	-10.5 to 11.6	V
AT ⁶	Unpowered, ADC reset asserted or	unconfigured	-0.3 to 15.5	–0.3 to 14.5	V
	Analog input (+16 V, +4 V prescale	r range)	-0.3 to 15.5	–0.3 to 14.5	V
	Analog input (direct input to ADC)		-0.3 to 3.6	-0.3 to 3.6	V
	Digital input		-0.3 to 15.5	-0.3 to 14.5	V

Table 3-2 • Recommended Operating Conditions¹

Notes:

1. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-85 on page 2-157.

- 2. All parameters representing voltages are measured with respect to GND unless otherwise specified.
- 3. The programming temperature range supported is $T_{ambient} = 0^{\circ}C$ to 85°C.
- 4. VPUMP can be left floating during normal operation (not programming mode).
- 5. Violating the V_{CC15A} recommended voltage supply during an embedded flash program cycle can corrupt the page being programmed.
- 6. The input voltage may overshoot by up to 500 mV above the Recommended Maximum (150 mV in Direct mode), provided the duration of the overshoot is less than 50% of the operating lifetime of the device.
- 7. The AG pad should also conform to the limits as specified in Table 2-48 on page 2-114.

Pads	Pad Configuration	Prescaler Range	Input Resistance to Ground
AV, AC	Analog Input (direct input to ADC)	-	2 kΩ (typical)
		-	> 10 MΩ
	Analog Input (positive prescaler)	+16 V to +2 V	1 MΩ (typical)
		+1 V to +0.125 V	> 10 MΩ
	Analog Input (negative prescaler)	–16 V to –2 V	1 MΩ (typical)
		–1 V to –0.125 V	> 10 MΩ
	Digital input	+16 V to +2 V	1 MΩ (typical)
	Current monitor	+16 V to +2 V	1 MΩ (typical)
		–16 V to –2 V	1 MΩ (typical)
AT	Analog Input (direct input to ADC)	-	1 MΩ (typical)
	Analog Input (positive prescaler)	+16 V, +4 V	1 MΩ (typical)
	Digital input	+16 V, +4 V	1 MΩ (typical)
	Temperature monitor	+16 V, +4 V	> 10 MΩ

Table 3-3 • Input Resistance of Analog Pads

Table 3-4 • Overshoot and Undershoot Limits ¹

vccı	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle ²	Maximum Overshoot/ Undershoot ²
2.7 V or less	10%	1.4 V
	5%	1.49 V
3.0 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. Based on reliability requirements at a junction temperature of 85°C.

2. The duration is allowed at one cycle out of six clock cycle. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.



Figure 3-1 • I/O State as a Function of VCCI and VCC Voltage Levels

Calculating Power Dissipation

Quiescent Supply Current

Table 3-8 • AFS1500 Quiescent Supply Current Characteristics

Parameter	Description	Conditions	Temp.	Min.	Тур.	Max.	Unit
ICC ¹	1.5 V quiescent current	Operational standby ⁴ ,	T _J = 25°C		20	40	mA
		VCC = 1.575 V	T _J = 85°C		32	65	mA
			T _J = 100°C		59	120	mA
		Standby mode ⁵ or Sleep mode ⁶ , VCC = 0 V			0	0	μA
ICC33 ²	3.3 V analog supplies	Operational standby ⁴ ,	T _J = 25°C		9.8	13	mA
	current	VCC33 = 3.63 V	T _J = 85°C		10.7	14	mA
			T _J = 100°C		10.8	15	mA
		Operational standby, only Analog Quad and –3.3 V output ON, VCC33 = 3.63 V	T _J = 25°C		0.31	2	mA
			T _J = 85°C		0.35	2	mA
			T _J = 100°C		0.45	2	mA
		Standby mode ⁵ , VCC33 = 3.63 V	T _J = 25°C		2.9	3.6	mA
			T _J = 85°C		2.9	4	mA
			T _J = 100°C		3.3	6	mA
		Sleep mode ⁶ , VCC33 = 3.63 V	T _J = 25°C		17	19	μA
			T _J = 85°C		18	20	μA
			T _J = 100°C		24	25	μA
ICCI ³	I/O quiescent current	Operational standby ⁴ ,	T _J = 25°C		417	649	μA
		Standby mode, and Sleep Mode ^{b} , VCCIx = 3.63 V	T _J = 85°C		417	649	μA
			T _J = 100°C		417	649	μA

Notes:

1. ICC is the 1.5 V power supplies, ICC and ICC15A.

2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.

3. ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.

4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.

5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.

6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.



DC and Power Characteristics

Parameter	Description	Conditions	Temp.	Min.	Тур.	Max.	Unit
IJTAG	JTAG I/O quiescent	Operational standby ⁴ ,	T _J = 25°C		80	100	μA
	current	VJTAG = 3.63 V	T _J = 85°C		80	100	μA
			T _J = 100°C		80	100	μA
		Standby mode ⁵ or Sleep mode ⁶ , VJTAG = 0 V			0	0	μA
IPP	Programming supply	Non-programming mode,	T _J = 25°C		39	80	μA
	current	VPUMP = 3.63 V	T _J = 85°C		40	80	μA
			T _J = 100°C		40	80	μA
		Standby mode ⁵ or Sleep mode ⁶ , VPUMP = 0 V			0	0	μA
ICCNVM	Embedded NVM	Reset asserted, V _{CCNVM} = 1.575 V	T _J = 25°C		50	150	μA
	current		Т _Ј =85°С		50	150	μA
			T _J = 100°C		50	150	μA
ICCPLL	1.5 V PLL quiescent	Operational standby	T _J = 25°C		130	200	μA
	current	, VCCPLL = 1.575 V	T _J = 85°C		130	200	μA
			T _J = 100°C		130	200	μA

Table 3-8 •	AFS1500 Quiescent	Supply Current	Characteristics	(continued)
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Notes:

1. ICC is the 1.5 V power supplies, ICC and ICC15A.

2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.

3. ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.

4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.

5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.

6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.



DC and Power Characteristics

Parameter	Description	Conditions	Temp.	Min	Тур	Мах	Unit
ICCNVM	Embedded NVM current	Reset asserted, VCCNVM = 1.575 V	T _J = 25°C		10	40	μA
			T _J = 85°C		14	40	μA
			T _J = 100°C		14	40	μA
ICCPLL	1.5 V PLL quiescent current	Operational standby, VCCPLL = 1.575 V	T _J = 25°C		65	100	μA
			T _J = 85°C		65	100	μA
			T _J = 100°C		65	100	μA

Table 3-11 • AFS090 Quiescent Supply Current Characteristics (continued)

Notes:

1. ICC is the 1.5 V power supplies, ICC, ICCPLL, ICC15A, ICCNVM.

2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.

- 3. ICCI includes all ICCI0, ICCI1, and ICCI2.
- 4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.

5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.

6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.



Package Pin Assignments

	FG484		FG484			
Pin Number	AFS600 Function	AFS1500 Function	Pin Number	AFS600 Function	AFS1500 Function	
A1	GND	GND	AA14	AG7	AG7	
A2	VCC	NC	AA15	AG8	AG8	
A3	GAA1/IO01PDB0V0	GAA1/IO01PDB0V0	AA16	GNDA	GNDA	
A4	GAB0/IO02NDB0V0	GAB0/IO02NDB0V0	AA17	AG9	AG9	
A5	GAB1/IO02PDB0V0	GAB1/IO02PDB0V0	AA18	VAREF	VAREF	
A6	IO07NDB0V1	IO07NDB0V1	AA19	VCCIB2	VCCIB2	
A7	IO07PDB0V1	IO07PDB0V1	AA20	PTEM	PTEM	
A8	IO10PDB0V1	IO09PDB0V1	AA21	GND	GND	
A9	IO14NDB0V1	IO13NDB0V2	AA22	VCC	NC	
A10	IO14PDB0V1	IO13PDB0V2	AB1	GND	GND	
A11	IO17PDB1V0	IO24PDB1V0	AB2	VCC	NC	
A12	IO18PDB1V0	IO26PDB1V0	AB3	NC	IO94NSB4V0	
A13	IO19NDB1V0	IO27NDB1V1	AB4	GND	GND	
A14	IO19PDB1V0	IO27PDB1V1	AB5	VCC33N	VCC33N	
A15	IO24NDB1V1	IO35NDB1V2	AB6	AT0	AT0	
A16	IO24PDB1V1	IO35PDB1V2	AB7	ATRTN0	ATRTN0	
A17	GBC0/IO26NDB1V1	GBC0/IO40NDB1V2	AB8	AT1	AT1	
A18	GBA0/IO28NDB1V1	GBA0/IO42NDB1V2	AB9	AT2	AT2	
A19	IO29NDB1V1	IO43NDB1V2	AB10	ATRTN1	ATRTN1	
A20	IO29PDB1V1	IO43PDB1V2	AB11	AT3	AT3	
A21	VCC	NC	AB12	AT6	AT6	
A22	GND	GND	AB13	ATRTN3	ATRTN3	
AA1	VCC	NC	AB14	AT7	AT7	
AA2	GND	GND	AB15	AT8	AT8	
AA3	VCCIB4	VCCIB4	AB16	ATRTN4	ATRTN4	
AA4	VCCIB4	VCCIB4	AB17	AT9	AT9	
AA5	PCAP	PCAP	AB18	VCC33A	VCC33A	
AA6	AG0	AG0	AB19	GND	GND	
AA7	GNDA	GNDA	AB20	NC	IO76NPB2V0	
AA8	AG1	AG1	AB21	VCC	NC	
AA9	AG2	AG2	AB22	GND	GND	
AA10	GNDA	GNDA	B1	VCC	NC	
AA11	AG3	AG3	B2	GND	GND	
AA12	AG6	AG6	B3	GAA0/IO01NDB0V0	GAA0/IO01NDB0V0	
AA13	GNDA	GNDA	B4	GND	GND	