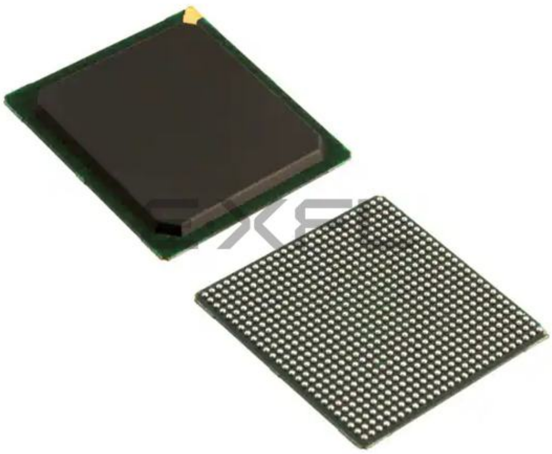

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 276480 |
| Number of I/O | 252 |
| Number of Gates | 1500000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 676-BGA |
| Supplier Device Package | 676-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/afs1500-2fgg676 |

# Fusion Device Architecture Overview

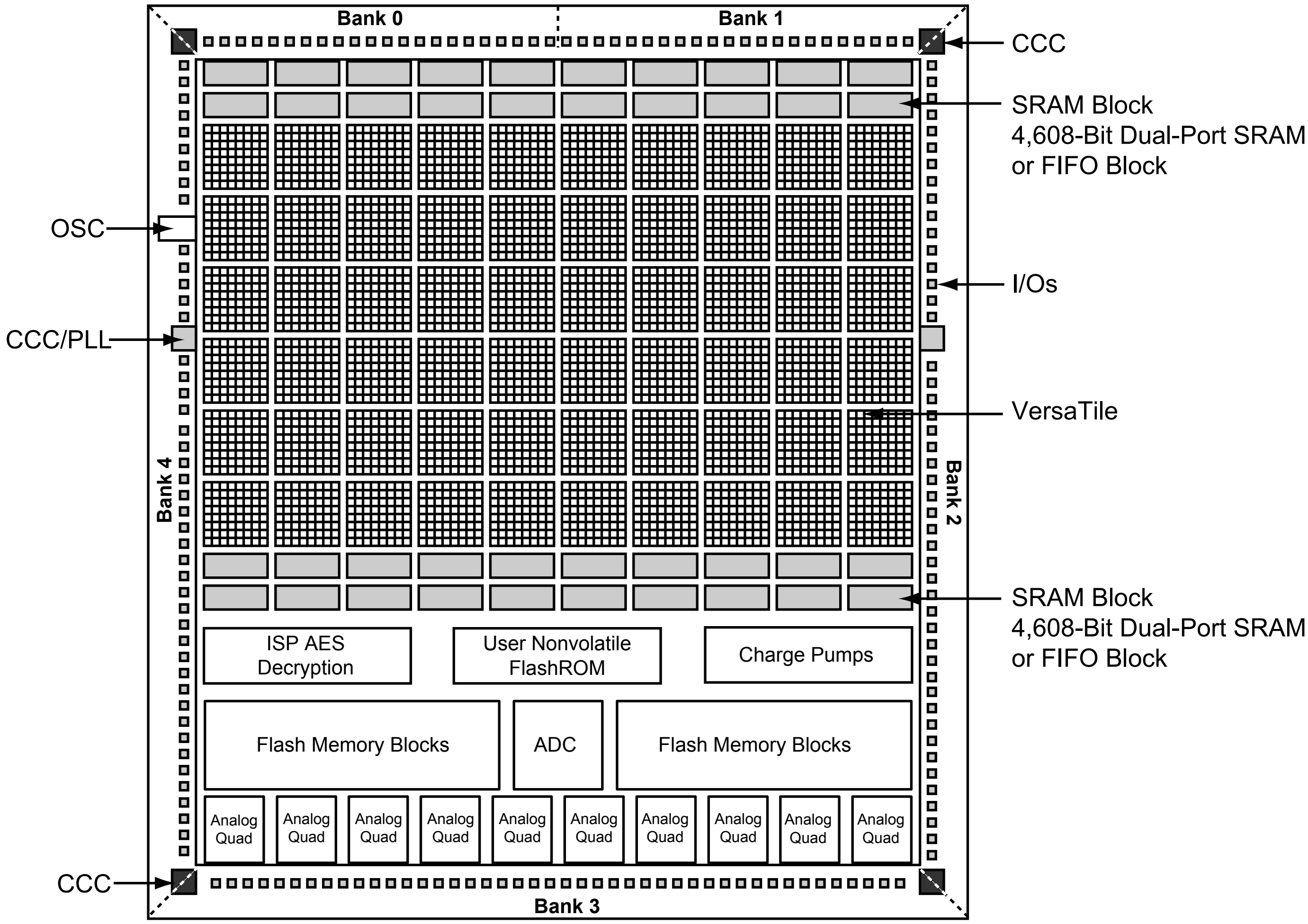



*Figure 1 •* **Fusion Device Architecture Overview (AFS600)**

# Package I/Os: Single-/Double-Ended (Analog)

| **Fusion Devices** | **AFS090** | **AFS250** | **AFS600** | **AFS1500** |
|---|---|---|---|---|
| **ARM Cortex-M1 Devices** | | **M1AFS250** | **M1AFS600** | **M1AFS1500** |
| **Pigeon Point Devices** | | | **P1AFS600** [1] | **P1AFS1500** [1] |
| **MicroBlade Devices** | | **U1AFS250** [2] | **U1AFS600** [2] | **U1AFS1500** [2] |
| QN108 [3] | 37/9 (16) | | | |
| QN180 [3] | 60/16 (20) | 65/15 (24) | | |
| PQ208 [4] | | 93/26 (24) | 95/46 (40) | |
| FG256 | 75/22 (20) | 114/37 (24) | 119/58 (40) | 119/58 (40) |
| FG484 | | | 172/86 (40) | 223/109 (40) |
| FG676 | | | | 252/126 (40) |

*Notes:*
1. *Pigeon Point devices are only offered in FG484 and FG256.*
2. *MicroBlade devices are only offered in FG256.*
3. *Package not available.*
4. *Fusion devices in the same package are pin compatible with the exception of the PQ208 package (AFS250 and AFS600).*

The FlashPoint tool in the Fusion development software solutions, Libero SoC and Designer, has extensive support for flash memory blocks and FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using the Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

### *SRAM and FIFO*

Fusion devices have embedded SRAM blocks along the north and south sides of the device. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be written through a 4-bit port and read as a single bitstream. The SRAM blocks can be initialized from the flash memory blocks or via the device JTAG port (ROM emulation mode), using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal EMPTY and FULL flags. The embedded FIFO control unit contains the counters necessary for the generation of the read and write address pointers. The SRAM/FIFO blocks can be cascaded to create larger configurations.

## Clock Resources

### *PLLs and Clock Conditioning Circuits (CCCs)*

Fusion devices provide designers with very flexible clock conditioning capabilities. Each member of the Fusion family contains six CCCs. In the two larger family members, two of these CCCs also include a PLL; the smaller devices support one PLL.

The inputs of the CCC blocks are accessible from the FPGA core or from one of several inputs with dedicated CCC block connections.

The CCC block has the following key features:

- Wide input frequency range ($f_{IN\_CCC}$) = 1.5 MHz to 350 MHz
- Output frequency range ($f_{OUT\_CCC}$) = 0.75 MHz to 350 MHz
- Clock phase adjustment via programmable and fixed delays from –6.275 ns to +8.75 ns
- Clock skew minimization (PLL)
- Clock frequency synthesis (PLL)
- On-chip analog clocking resources usable as inputs:
  – 100 MHz on-chip RC oscillator
  – Crystal oscillator

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°
- Output duty cycle = 50% ± 1.5%
- Low output jitter. Samples of peak-to-peak period jitter when a single global network is used:
  – 70 ps at 350 MHz
  – 90 ps at 100 MHz
  – 180 ps at 24 MHz
  – Worst case < 2.5% × clock period
- Maximum acquisition time = 150 µs
- Low power consumption of 5 mW

## Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

The I/Os are controlled by the JTAG Boundary Scan register during programming, except for the analog pins (AC, AT and AV). The Boundary Scan register of the AG pin can be used to enable/disable the gate driver in software v9.0.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click **PDB Configuration**. A FlashPoint – Programming File Generator window appears.
3. Click the **Specify I/O States During Programming** button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-3).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tri-State: I/O is tristated

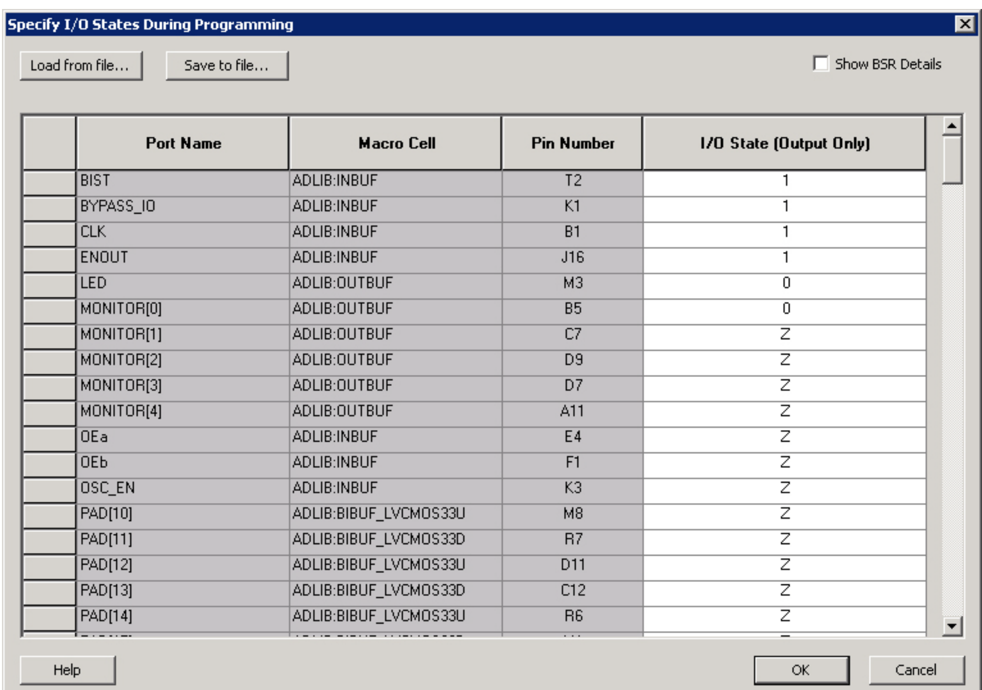



*Figure 1-3 •* **I/O States During Programming Window**

6. Click **OK** to return to the FlashPoint – Programming File Generator window.

I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

### Clock Aggregation

Clock aggregation allows for multi-spine clock domains. A MUX tree provides the necessary flexibility to allow long lines or I/Os to access domains of one, two, or four global spines. Signal access to the clock aggregation system is achieved through long-line resources in the central rib, and also through local resources in the north and south ribs, allowing I/Os to feed directly into the clock system. As Figure 2-14 indicates, this access system is contiguous.

There is no break in the middle of the chip for north and south I/O VersaNet access. This is different from the quadrant clocks, located in these ribs, which only reach the middle of the rib. Refer to the *Using Global Resources in Actel Fusion Devices* application note.

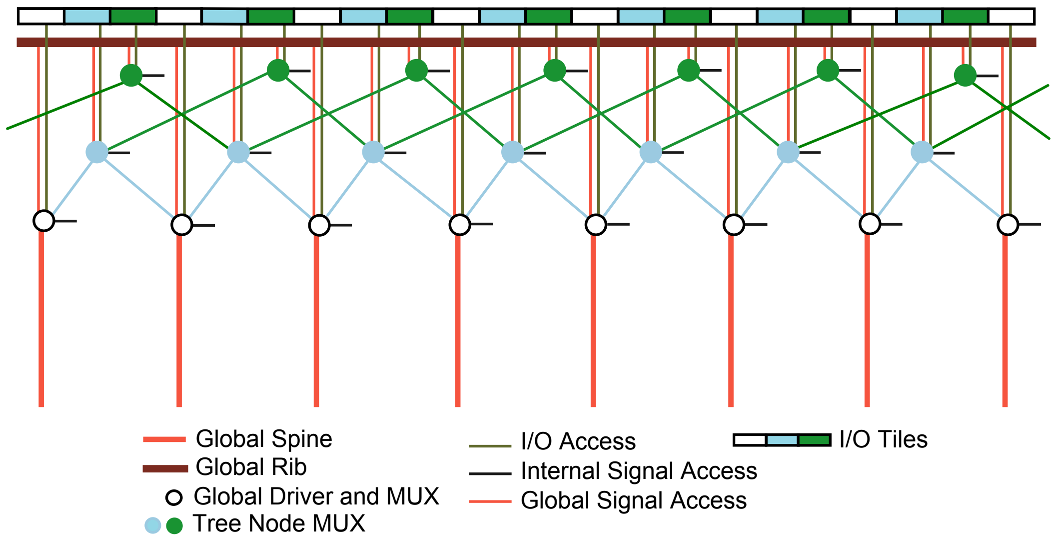



***Figure 2-14 •* Clock Aggregation Tree Architecture**

## VersaNet Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are dependent upon I/O standard, and the clock may be driven and conditioned internally by the CCC module. Table 2-5, Table 2-6, Table 2-7, and Table 2-8 on page 2-17 present minimum and maximum global clock delays within the device Minimum and maximum delays are measured with minimum and maximum loading, respectively.

### Timing Characteristics

**Table 2-5 • AFS1500 Global Resource Timing**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.53 | 1.75 | 1.74 | 1.99 | 2.05 | 2.34 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.53 | 1.79 | 1.75 | 2.04 | 2.05 | 2.40 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | | | | | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | | | | | | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.26 | | 0.29 | | 0.34 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

**Table 2-6 • AFS600 Global Resource Timing**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 1.27 | 1.49 | 1.44 | 1.70 | 1.69 | 2.00 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 1.26 | 1.54 | 1.44 | 1.75 | 1.69 | 2.06 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | | | | | | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | | | | | | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.27 | | 0.31 | | 0.36 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

Conversely, when writing 4-bit values and reading 9-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ little-endian byte order for read and write operations.

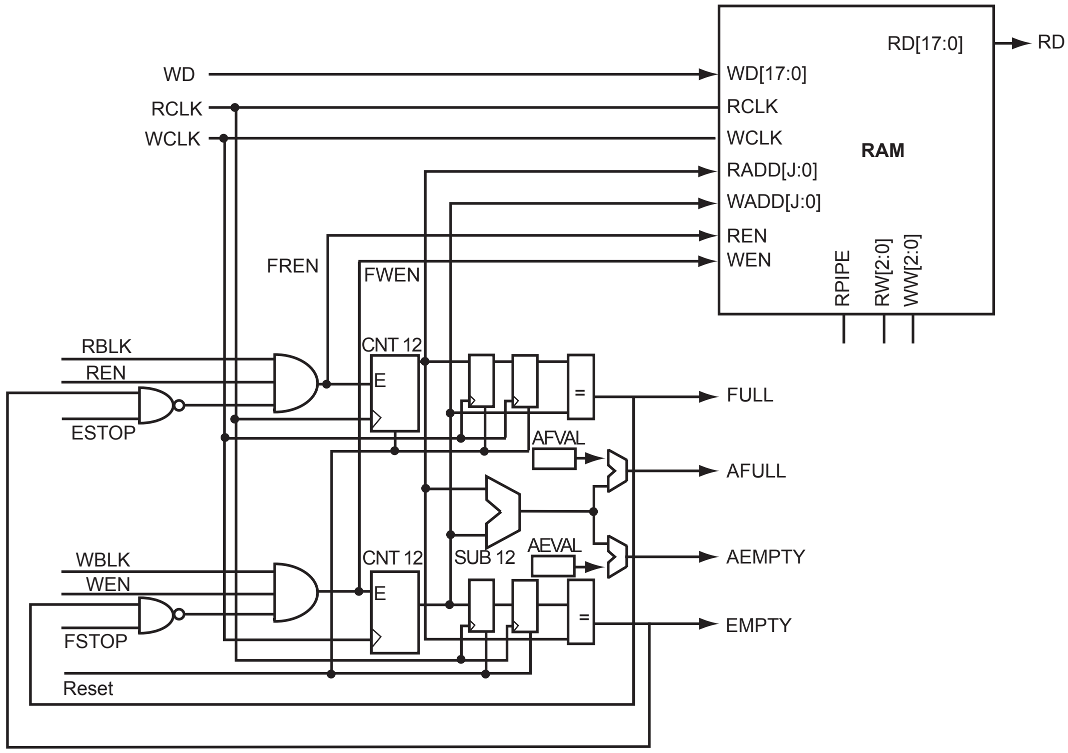



***Figure 2-47* • Fusion RAM Block with Embedded FIFO Controller**

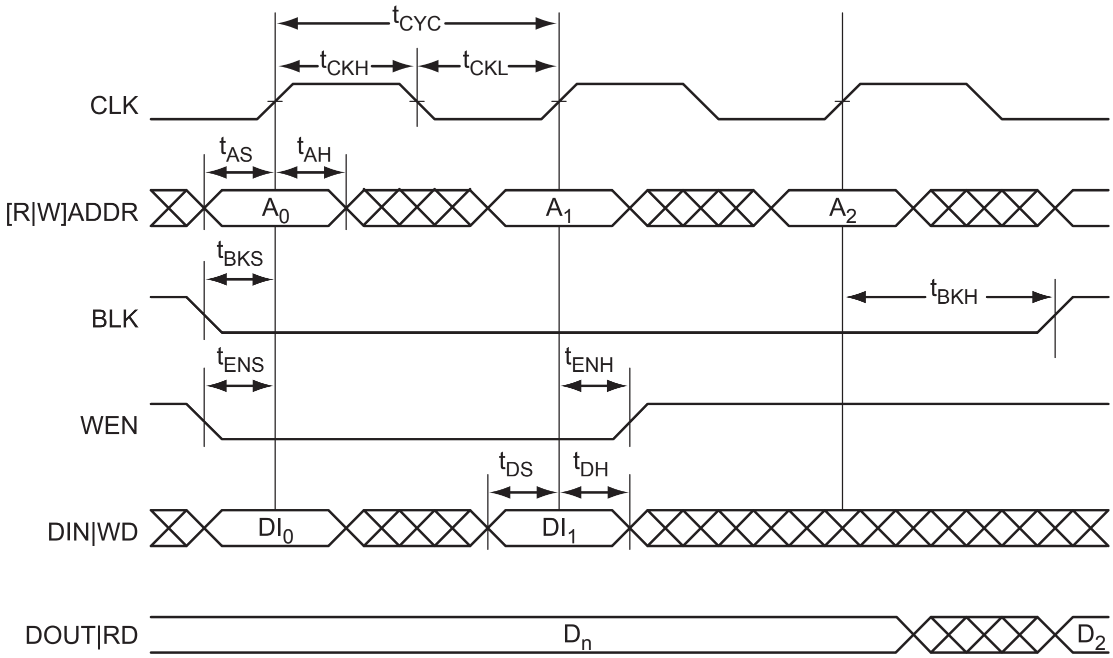



*Figure 2-52* • **RAM Write, Output Retained. Applicable to both RAM4K9 and RAM512x18.**

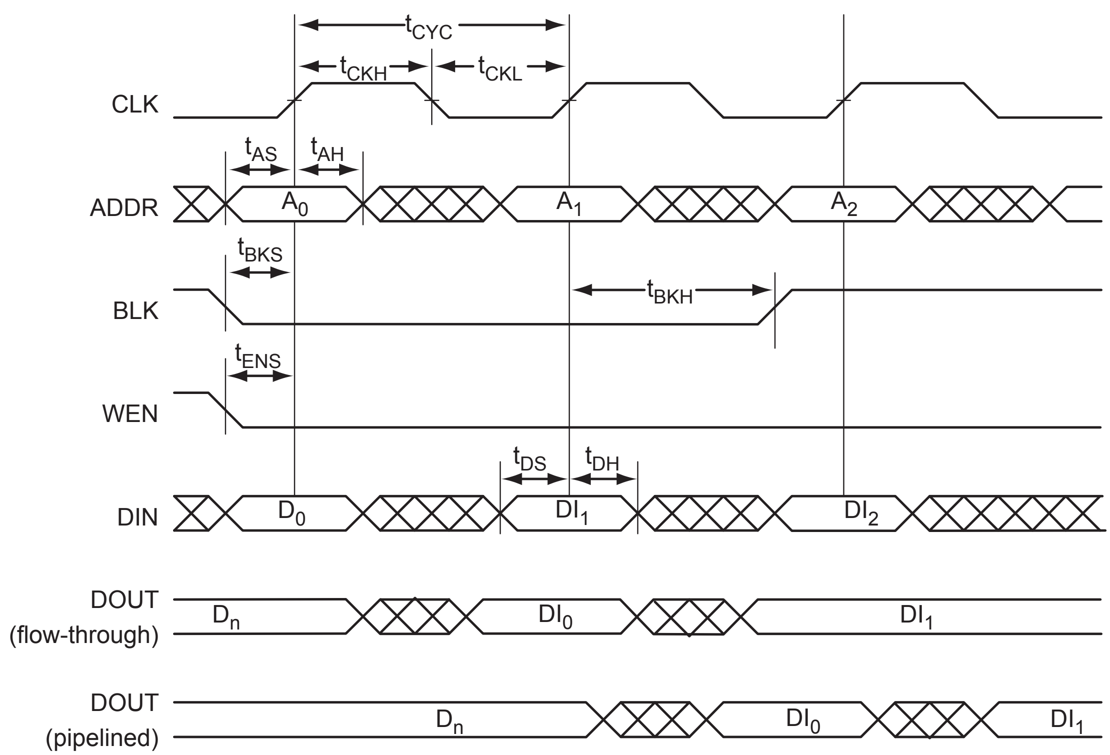



*Figure 2-53* • **RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 Only.**

### Gain Error

The gain error of an ADC indicates how well the slope of an actual transfer function matches the slope of the ideal transfer function. Gain error is usually expressed in LSB or as a percent of full-scale (%FSR). Gain error is the full-scale error minus the offset error (Figure 2-84).

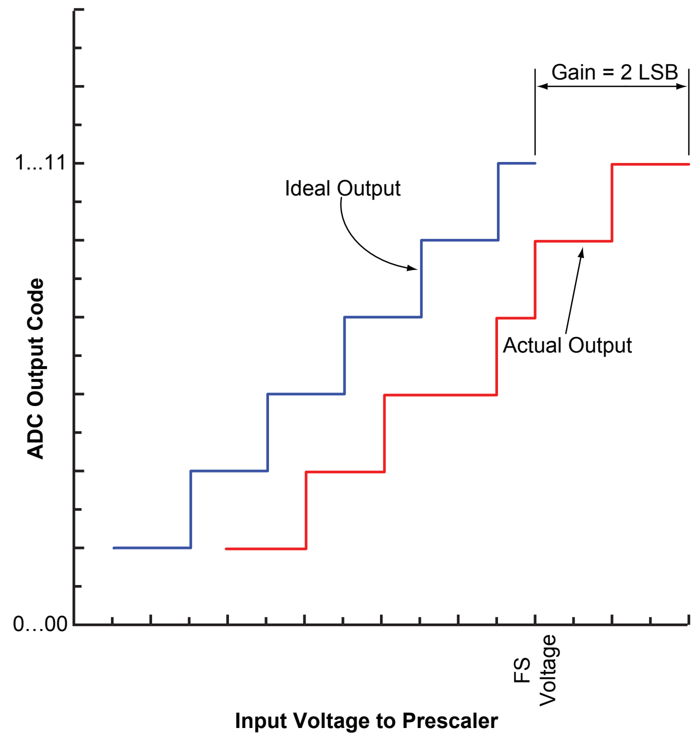



*Figure 2-84* • **Gain Error**

### Gain Error Drift

Gain-error drift is the variation in gain error due to a change in ambient temperature, typically expressed in ppm/°C.

### ADC Input Multiplexer

At the input to the Fusion ADC is a 32:1 multiplexer. Of the 32 input channels, up to 30 are user definable. Two of these channels are hardwired internally. Channel 31 connects to an internal temperature diode so the temperature of the Fusion device itself can be monitored. Channel 0 is wired to the FPGA's 1.5 V VCC supply, enabling the Fusion device to monitor its own power supply. Doing this internally makes it unnecessary to use an analog I/O to support these functions. The balance of the MUX inputs are connected to Analog Quads (see the "Analog Quad" section on page 2-80). Table 2-40 defines which Analog Quad inputs are associated with which specific analog MUX channels. The number of Analog Quads present is device-dependent; refer to the family list in the "Fusion Family" table on page I of this datasheet for the number of quads per device. Regardless of the number of quads populated in a device, the internal connections to both VCC and the internal temperature diode remain on Channels 0 and 31, respectively. To sample the internal temperature monitor, it must be strobed (similar to the AT pads). The TMSTBINT pin on the Analog Block macro is the control for strobing the internal temperature measurement diode.

To determine which channel is selected for conversion, there is a five-pin interface on the Analog Block, CHNUMBER[4:0], defined in Table 2-39.

***Table 2-39* • Channel Selection**

| Channel Number | CHNUMBER[4:0] |
|---|---|
| 0 | 00000 |
| 1 | 00001 |
| 2 | 00010 |
| 3 | 00011 |
| .<br>.<br>. | .<br>.<br>. |
| 30 | 11110 |
| 31 | 11111 |

Table 2-40 shows the correlation between the analog MUX input channels and the analog input pins.

***Table 2-40* • Analog MUX Channels**

| Analog MUX Channel | Signal | Analog Quad Number |
|---|---|---|
| 0 | Vcc_analog | |
| 1 | AV0 | Analog Quad 0 |
| 2 | AC0 | |
| 3 | AT0 | |
| 4 | AV1 | Analog Quad 1 |
| 5 | AC1 | |
| 6 | AT1 | |
| 7 | AV2 | Analog Quad 2 |
| 8 | AC2 | |
| 9 | AT2 | |
| 10 | AV3 | Analog Quad 3 |
| 11 | AC3 | |
| 12 | AT3 | |
| 13 | AV4 | Analog Quad 4 |
| 14 | AC4 | |
| 15 | AT4 | |

EQ 16 through EQ 18 can be used to calculate the acquisition time required for a given input. The STC signal gives the number of sample periods in ADCCLK for the acquisition time of the desired signal. If the actual acquisition time is higher than the STC value, the settling time error can affect the accuracy of the ADC, because the sampling capacitor is only partially charged within the given sampling cycle. Example acquisition times are given in Table 2-44 and Table 2-45. When controlling the sample time for the ADC along with the use of the active bipolar prescaler, current monitor, or temperature monitor, the minimum sample time(s) for each must be obeyed. EQ 19 can be used to determine the appropriate value of STC.

You can calculate the minimum actual acquisition time by using EQ 16:

$$VOUT = VIN(1 - e^{-t/RC})$$

*EQ 16*

For 0.5 LSB gain error, VOUT should be replaced with (VIN –(0.5 × LSB Value)):

$$(VIN - 0.5 \times \text{LSB Value}) = VIN(1 - e^{-t/RC})$$

*EQ 17*

where VIN is the ADC reference voltage (VREF)

Solving EQ 17:

$$t = RC \times \ln(VIN / (0.5 \times \text{LSB Value}))$$

*EQ 18*

where $R = Z_{INAD} + R_{SOURCE}$ and $C = C_{INAD}$.

Calculate the value of STC by using EQ 19.

$$t_{SAMPLE} = (2 + STC) \times (1 / ADCCLK) \text{ or } t_{SAMPLE} = (2 + STC) \times (\text{ADC Clock Period})$$

*EQ 19*

where ADCCLK = ADC clock frequency in MHz.

$t_{SAMPLE}$ = 0.449 µs from bit resolution in Table 2-44.

ADC Clock frequency = 10 MHz or a 100 ns period.

STC = ($t_{SAMPLE}$ / (1 / 10 MHz)) – 2 = 4.49 – 2 = 2.49.

You must round up to 3 to accommodate the minimum sample time.

***Table 2-44* • Acquisition Time Example with VAREF = 2.56 V**

| VIN = 2.56V, R = 4K ($R_{SOURCE}$ ~ 0), C = 18 pF | | |
|---|---|---|
| **Resolution** | **LSB Value (mV)** | **Min. Sample/Hold Time for 0.5 LSB (µs)** |
| 8 | 10 | 0.449 |
| 10 | 2.5 | 0.549 |
| 12 | 0.625 | 0.649 |

***Table 2-45* • Acquisition Time Example with VAREF = 3.3 V**

| VIN = 3.3V, R = 4K ($R_{SOURCE}$ ~ 0), C = 18 pF | | |
|---|---|---|
| **Resolution** | **LSB Value (mV)** | **Min. Sample/Hold time for 0.5 LSB (µs)** |
| 8 | 12.891 | 0.449 |
| 10 | 3.223 | 0.549 |
| 12 | 0.806 | 0.649 |

### *Sample Phase*

A conversion is performed in three phases. In the first phase, the analog input voltage is sampled on the input capacitor. This phase is called sample phase. During the sample phase, the output signals BUSY and SAMPLE change from '0' to '1', indicating the ADC is busy and sampling the analog signal. The sample time can be controlled by input signals STC[7:0]. The sample time can be calculated by EQ 20. When controlling the sample time for the ADC along with the use of Prescaler or Current Monitor or Temperature Monitor, the minimum sample time for each must be obeyed.

# User I/O Characteristics

## Timing Model

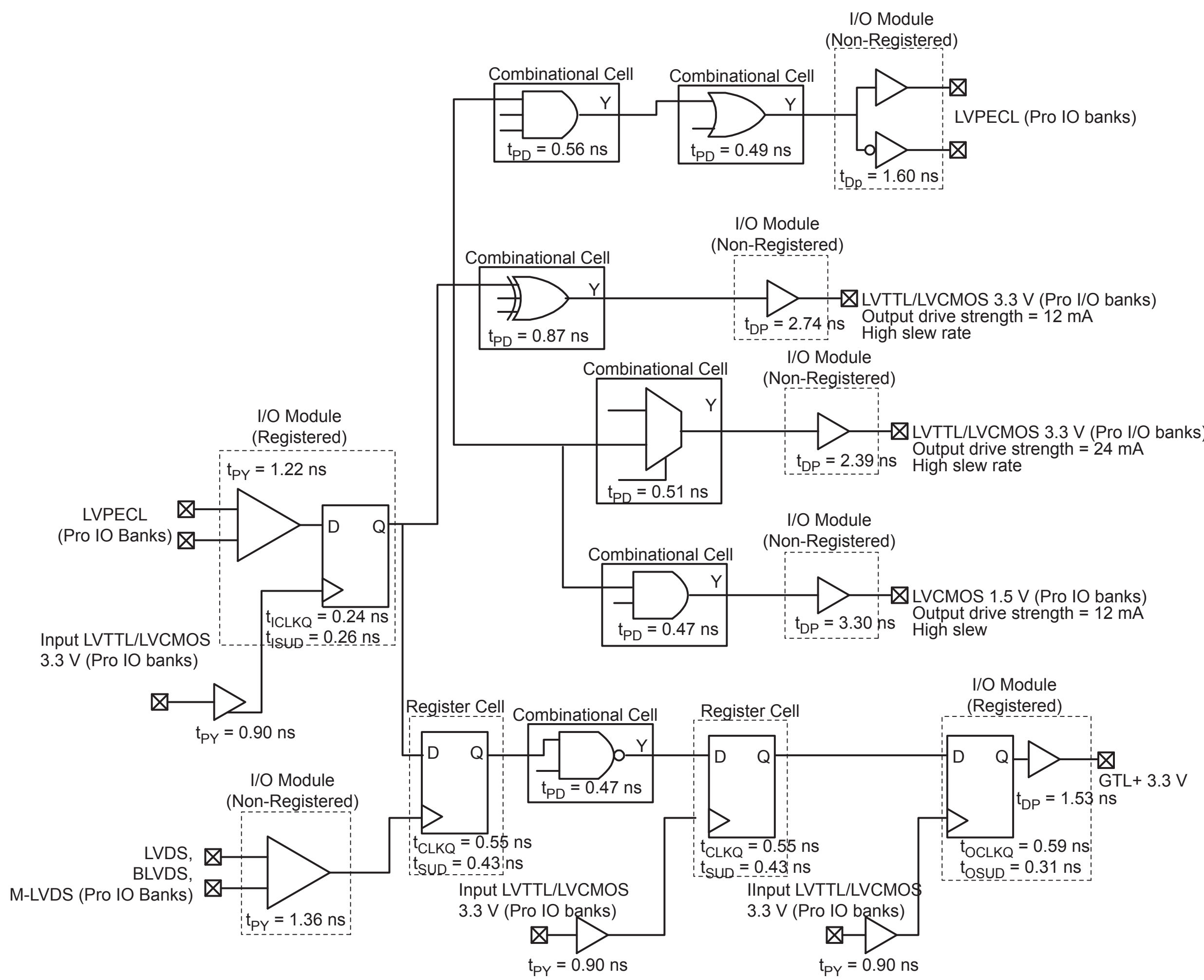



***Figure 2-115* • Timing Model**
**Operating Conditions: –2 Speed, Commercial Temperature Range ($T_J$ = 70°C), Worst-Case VCC = 1.425 V**

**Table 2-107 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Advanced I/Os**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 0.66 | 7.66 | 0.04 | 1.20 | 0.43 | 7.80 | 6.59 | 2.65 | 2.61 | 10.03 | 8.82 | ns |
| | –1 | 0.56 | 6.51 | 0.04 | 1.02 | 0.36 | 6.63 | 5.60 | 2.25 | 2.22 | 8.54 | 7.51 | ns |
| | –2 | 0.49 | 5.72 | 0.03 | 0.90 | 0.32 | 5.82 | 4.92 | 1.98 | 1.95 | 7.49 | 6.59 | ns |
| 8 mA | Std. | 0.66 | 4.91 | 0.04 | 1.20 | 0.43 | 5.00 | 4.07 | 2.99 | 3.20 | 7.23 | 6.31 | ns |
| | –1 | 0.56 | 4.17 | 0.04 | 1.02 | 0.36 | 4.25 | 3.46 | 2.54 | 2.73 | 6.15 | 5.36 | ns |
| | –2 | 0.49 | 3.66 | 0.03 | 0.90 | 0.32 | 3.73 | 3.04 | 2.23 | 2.39 | 5.40 | 4.71 | ns |
| 12 mA | Std. | 0.66 | 3.53 | 0.04 | 1.20 | 0.43 | 3.60 | 2.82 | 3.21 | 3.58 | 5.83 | 5.06 | ns |
| | –1 | 0.56 | 3.00 | 0.04 | 1.02 | 0.36 | 3.06 | 2.40 | 2.73 | 3.05 | 4.96 | 4.30 | ns |
| | –2 | 0.49 | 2.64 | 0.03 | 0.90 | 0.32 | 2.69 | 2.11 | 2.40 | 2.68 | 4.36 | 3.78 | ns |
| 16 mA | Std. | 0.66 | 3.33 | 0.04 | 1.20 | 0.43 | 3.39 | 2.56 | 3.26 | 3.68 | 5.63 | 4.80 | ns |
| | –1 | 0.56 | 2.83 | 0.04 | 1.02 | 0.36 | 2.89 | 2.18 | 2.77 | 3.13 | 4.79 | 4.08 | ns |
| | –2 | 0.49 | 2.49 | 0.03 | 0.90 | 0.32 | 2.53 | 1.91 | 2.44 | 2.75 | 4.20 | 3.58 | ns |
| 24 mA | Std. | 0.66 | 3.08 | 0.04 | 1.20 | 0.43 | 3.13 | 2.12 | 3.32 | 4.06 | 5.37 | 4.35 | ns |
| | –1 | 0.56 | 2.62 | 0.04 | 1.02 | 0.36 | 2.66 | 1.80 | 2.83 | 3.45 | 4.57 | 3.70 | ns |
| | –2 | 0.49 | 2.30 | 0.03 | 0.90 | 0.32 | 2.34 | 1.58 | 2.48 | 3.03 | 4.01 | 3.25 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

**Table 2-108 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Standard I/Os**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 9.46 | 0.04 | 1.00 | 0.43 | 9.64 | 8.54 | 2.07 | 2.04 | ns |
| | –1 | 0.56 | 8.05 | 0.04 | 0.85 | 0.36 | 8.20 | 7.27 | 1.76 | 1.73 | ns |
| | –2 | 0.49 | 7.07 | 0.03 | 0.75 | 0.32 | 7.20 | 6.38 | 1.55 | 1.52 | ns |
| 4 mA | Std. | 0.66 | 9.46 | 0.04 | 1.00 | 0.43 | 9.64 | 8.54 | 2.07 | 2.04 | ns |
| | –1 | 0.56 | 8.05 | 0.04 | 0.85 | 0.36 | 8.20 | 7.27 | 1.76 | 1.73 | ns |
| | –2 | 0.49 | 7.07 | 0.03 | 0.75 | 0.32 | 7.20 | 6.38 | 1.55 | 1.52 | ns |
| 6 mA | Std. | 0.66 | 6.57 | 0.04 | 1.00 | 0.43 | 6.69 | 5.98 | 2.40 | 2.57 | ns |
| | –1 | 0.56 | 5.59 | 0.04 | 0.85 | 0.36 | 5.69 | 5.09 | 2.04 | 2.19 | ns |
| | –2 | 0.49 | 4.91 | 0.03 | 0.75 | 0.32 | 5.00 | 4.47 | 1.79 | 1.92 | ns |
| 8 mA | Std. | 0.66 | 6.57 | 0.04 | 1.00 | 0.43 | 6.69 | 5.98 | 2.40 | 2.57 | ns |
| | –1 | 0.56 | 5.59 | 0.04 | 0.85 | 0.36 | 5.69 | 5.09 | 2.04 | 2.19 | ns |
| | –2 | 0.49 | 4.91 | 0.03 | 0.75 | 0.32 | 5.00 | 4.47 | 1.79 | 1.92 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

***Table 2-122* • 1.8 V LVCMOS Low Slew**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V**
**Applicable to Advanced I/Os**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 15.53 | 0.04 | 1.31 | 0.43 | 14.11 | 15.53 | 2.78 | 1.60 | 16.35 | 17.77 | ns |
| | –1 | 0.56 | 13.21 | 0.04 | 1.11 | 0.36 | 12.01 | 13.21 | 2.36 | 1.36 | 13.91 | 15.11 | ns |
| | –2[2] | 0.49 | 11.60 | 0.03 | 0.98 | 0.32 | 10.54 | 11.60 | 2.07 | 1.19 | 12.21 | 13.27 | ns |
| 4 mA | Std. | 0.66 | 10.48 | 0.04 | 1.31 | 0.43 | 10.41 | 10.48 | 3.23 | 2.73 | 12.65 | 12.71 | ns |
| | –1 | 0.56 | 8.91 | 0.04 | 1.11 | 0.36 | 8.86 | 8.91 | 2.75 | 2.33 | 10.76 | 10.81 | ns |
| | –2 | 0.49 | 7.82 | 0.03 | 0.98 | 0.32 | 7.77 | 7.82 | 2.41 | 2.04 | 9.44 | 9.49 | ns |
| 8 mA | Std. | 0.66 | 8.05 | 0.04 | 1.31 | 0.43 | 8.20 | 7.84 | 3.54 | 3.27 | 10.43 | 10.08 | ns |
| | –1 | 0.56 | 6.85 | 0.04 | 1.11 | 0.36 | 6.97 | 6.67 | 3.01 | 2.78 | 8.88 | 8.57 | ns |
| | –2 | 0.49 | 6.01 | 0.03 | 0.98 | 0.32 | 6.12 | 5.86 | 2.64 | 2.44 | 7.79 | 7.53 | ns |
| 12 mA | Std. | 0.66 | 7.50 | 0.04 | 1.31 | 0.43 | 7.64 | 7.30 | 3.61 | 3.41 | 9.88 | 9.53 | ns |
| | –1 | 0.56 | 6.38 | 0.04 | 1.11 | 0.36 | 6.50 | 6.21 | 3.07 | 2.90 | 8.40 | 8.11 | ns |
| | –2 | 0.49 | 5.60 | 0.03 | 0.98 | 0.32 | 5.71 | 5.45 | 2.69 | 2.55 | 7.38 | 7.12 | ns |
| 16 mA | Std. | 0.66 | 7.29 | 0.04 | 1.31 | 0.43 | 7.23 | 7.29 | 3.71 | 3.95 | 9.47 | 9.53 | ns |
| | –1 | 0.56 | 6.20 | 0.04 | 1.11 | 0.36 | 6.15 | 6.20 | 3.15 | 3.36 | 8.06 | 8.11 | ns |
| | –2 | 0.49 | 5.45 | 0.03 | 0.98 | 0.32 | 5.40 | 5.45 | 2.77 | 2.95 | 7.07 | 7.12 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to* *Table 3-7 on page 3-9.*

## Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

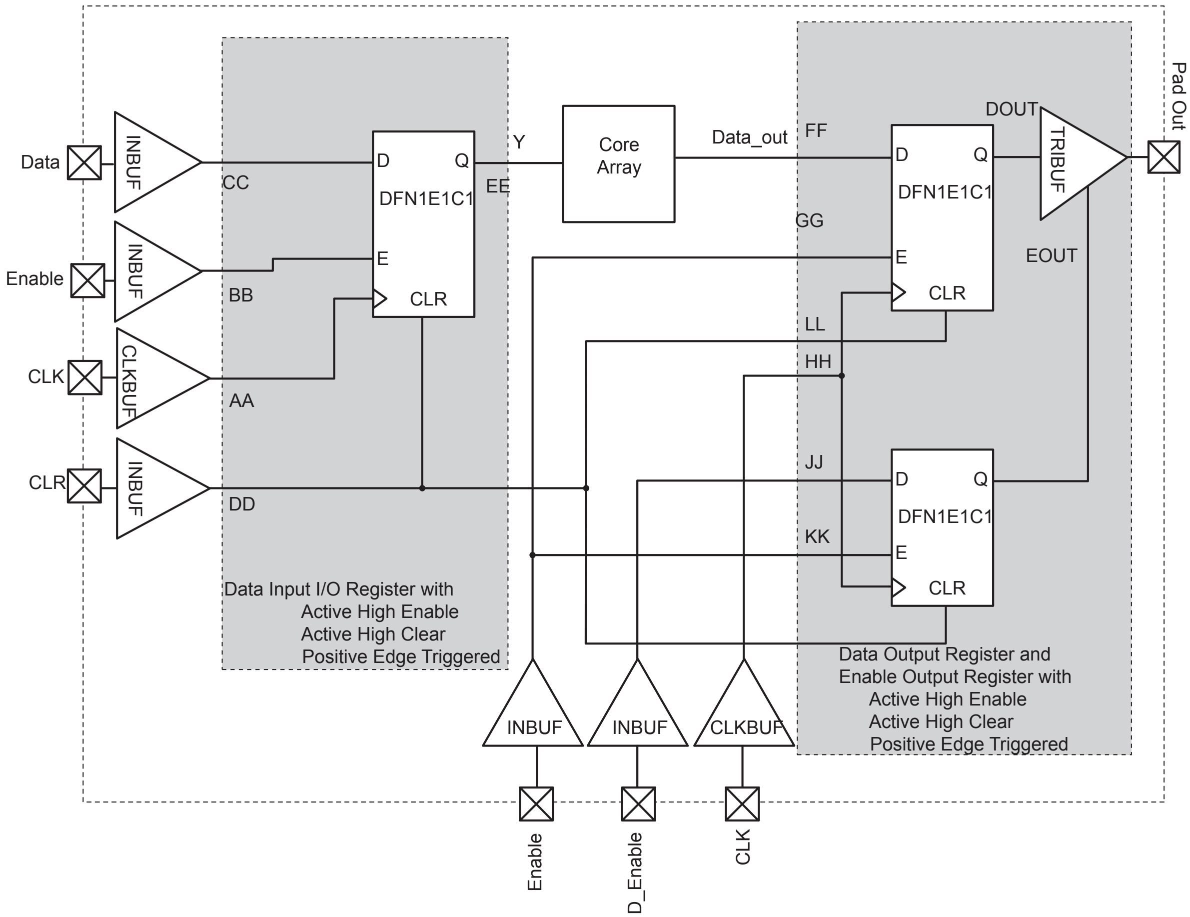



*Figure 2-138* **• Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

**TMS** **Test Mode Select**

The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

**TRST** **Boundary Scan Reset Pin**

The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the TAP is held in reset mode. The resistor values must be chosen from Table 2-183 and must satisfy the parallel resistance value requirement. The values in Table 2-183 correspond to the resistor recommended when a single device is used and to the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

## Special Function Pins

**NC** **No Connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

**DC** **Don't Connect**

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

**NCAP** **Negative Capacitor**

Negative Capacitor is where the negative terminal of the charge pump capacitor is connected. A capacitor, with a 2.2 µF recommended value, is required to connect between PCAP and NCAP.

**PCAP** **Positive Capacitor**

*Positive Capacitor* is where the positive terminal of the charge pump capacitor is connected. A capacitor, with a 2.2 µF recommended value, is required to connect between PCAP and NCAP.

**PUB** **Push Button**

*Push button* is the connection for the external momentary switch used to turn on the 1.5 V voltage regulator and can be floating if not used.

**PTBASE** **Pass Transistor Base**

*Pass Transistor Base* is the control signal of the voltage regulator. This pin should be connected to the base of the external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.

**PTEM** **Pass Transistor Emitter**

*Pass Transistor Emitter* is the feedback input of the voltage regulator.

This pin should be connected to the emitter of the external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.

**XTAL1** **Crystal Oscillator Circuit Input**

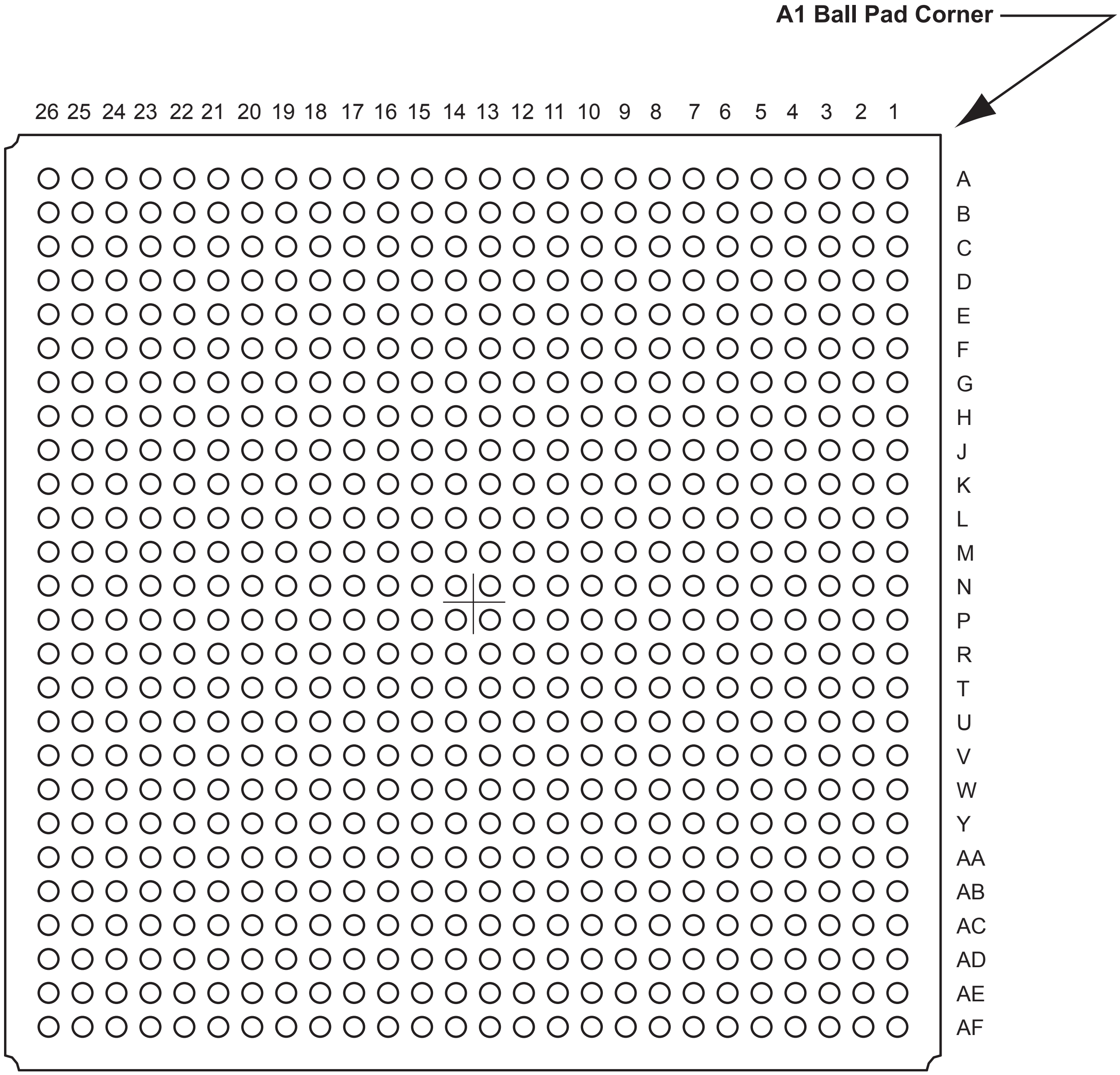
Input to crystal oscillator circuit. Pin for connecting external crystal, ceramic resonator, RC network, or external clock input. When using an external crystal or ceramic oscillator, external capacitors are also recommended (Please refer to the crystal oscillator manufacturer for proper capacitor value).

If using external RC network or clock input, XTAL1 should be used and XTAL2 left unconnected. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.

| QN180 | | |
|---|---|---|
| Pin Number | AFS090 Function | AFS250 Function |
| B9 | XTAL2 | XTAL2 |
| B10 | GEA0/IO44NDB3V0 | GFA0/IO66NDB3V0 |
| B11 | GEB2/IO42PDB3V0 | IO60NDB3V0 |
| B12 | VCC | VCC |
| B13 | VCCNVM | VCCNVM |
| B14 | VCC15A | VCC15A |
| B15 | NCAP | NCAP |
| B16 | VCC33N | VCC33N |
| B17 | GNDAQ | GNDAQ |
| B18 | AC0 | AC0 |
| B19 | AT0 | AT0 |
| B20 | AT1 | AT1 |
| B21 | AV1 | AV1 |
| B22 | AC2 | AC2 |
| B23 | ATRTN1 | ATRTN1 |
| B24 | AG3 | AG3 |
| B25 | AV3 | AV3 |
| B26 | AG4 | AG4 |
| B27 | ATRTN2 | ATRTN2 |
| B28 | NC | AC5 |
| B29 | VCC33A | VCC33A |
| B30 | VAREF | VAREF |
| B31 | PUB | PUB |
| B32 | PTEM | PTEM |
| B33 | GNDNVM | GNDNVM |
| B34 | VCC | VCC |
| B35 | TCK | TCK |
| B36 | TMS | TMS |
| B37 | TRST | TRST |
| B38 | GDB2/IO41PSB1V0 | GDA2/IO55PSB1V0 |
| B39 | GDC0/IO38NDB1V0 | GDB0/IO53NDB1V0 |
| B40 | VCCIB1 | VCCIB1 |
| B41 | GCA1/IO36PDB1V0 | GCA1/IO49PDB1V0 |
| B42 | GCC0/IO34NDB1V0 | GCC0/IO47NDB1V0 |
| B43 | GCB2/IO33PSB1V0 | GBC2/IO42PSB1V0 |
| B44 | VCC | VCC |

| QN180 | | |
|---|---|---|
| Pin Number | AFS090 Function | AFS250 Function |
| B45 | GBA2/IO31PDB1V0 | GBA2/IO40PDB1V0 |
| B46 | GNDQ | GNDQ |
| B47 | GBA1/IO30RSB0V0 | GBA0/IO38RSB0V0 |
| B48 | GBB1/IO28RSB0V0 | GBC1/IO35RSB0V0 |
| B49 | VCC | VCC |
| B50 | GBC0/IO25RSB0V0 | IO31RSB0V0 |
| B51 | IO23RSB0V0 | IO28RSB0V0 |
| B52 | IO20RSB0V0 | IO25RSB0V0 |
| B53 | VCC | VCC |
| B54 | IO11RSB0V0 | IO14RSB0V0 |
| B55 | IO08RSB0V0 | IO11RSB0V0 |
| B56 | GAC1/IO05RSB0V0 | IO08RSB0V0 |
| B57 | VCCIB0 | VCCIB0 |
| B58 | GAB0/IO02RSB0V0 | GAC0/IO04RSB0V0 |
| B59 | GAA0/IO00RSB0V0 | GAA1/IO01RSB0V0 |
| B60 | VCCPLA | VCCPLA |
| C1 | NC | NC |
| C2 | NC | VCCIB3 |
| C3 | GND | GND |
| C4 | NC | GFC2/IO69PPB3V0 |
| C5 | GFC1/IO49PDB3V0 | GFC1/IO68PDB3V0 |
| C6 | GFA0/IO47NPB3V0 | GFB0/IO67NPB3V0 |
| C7 | VCCIB3 | NC |
| C8 | GND | GND |
| C9 | GEA1/IO44PDB3V0 | GFA1/IO66PDB3V0 |
| C10 | GEA2/IO42NDB3V0 | GEC2/IO60PDB3V0 |
| C11 | NC | GEA2/IO58PSB3V0 |
| C12 | NC | NC |
| C13 | GND | GND |
| C14 | NC | NC |
| C15 | NC | NC |
| C16 | GNDA | GNDA |
| C17 | NC | NC |
| C18 | NC | NC |
| C19 | NC | NC |
| C20 | NC | NC |

# FG676




## *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/default.aspx.

| FG676 | |
|---|---|
| Pin Number | AFS1500 Function |
| A1 | NC |
| A2 | GND |
| A3 | NC |
| A4 | NC |
| A5 | GND |
| A6 | NC |
| A7 | NC |
| A8 | GND |
| A9 | IO17NDB0V2 |
| A10 | IO17PDB0V2 |
| A11 | GND |
| A12 | IO18NDB0V2 |
| A13 | IO18PDB0V2 |
| A14 | IO20NDB0V2 |
| A15 | IO20PDB0V2 |
| A16 | GND |
| A17 | IO21PDB0V2 |
| A18 | IO21NDB0V2 |
| A19 | GND |
| A20 | IO39NDB1V2 |
| A21 | IO39PDB1V2 |
| A22 | GND |
| A23 | NC |
| A24 | NC |
| A25 | GND |
| A26 | NC |
| AA1 | NC |
| AA2 | VCCIB4 |
| AA3 | IO93PDB4V0 |
| AA4 | GND |
| AA5 | IO93NDB4V0 |
| AA6 | GEB2/IO86PDB4V0 |
| AA7 | IO86NDB4V0 |
| AA8 | AV0 |
| AA9 | GNDA |
| AA10 | AV1 |

| FG676 | |
|---|---|
| Pin Number | AFS1500 Function |
| AA11 | AV2 |
| AA12 | GNDA |
| AA13 | AV3 |
| AA14 | AV6 |
| AA15 | GNDA |
| AA16 | AV7 |
| AA17 | AV8 |
| AA18 | GNDA |
| AA19 | AV9 |
| AA20 | VCCIB2 |
| AA21 | IO68PPB2V0 |
| AA22 | TCK |
| AA23 | GND |
| AA24 | IO76PPB2V0 |
| AA25 | VCCIB2 |
| AA26 | NC |
| AB1 | GND |
| AB2 | NC |
| AB3 | GEC2/IO87PDB4V0 |
| AB4 | IO87NDB4V0 |
| AB5 | GEA2/IO85PDB4V0 |
| AB6 | IO85NDB4V0 |
| AB7 | NCAP |
| AB8 | AC0 |
| AB9 | VCC33A |
| AB10 | AC1 |
| AB11 | AC2 |
| AB12 | VCC33A |
| AB13 | AC3 |
| AB14 | AC6 |
| AB15 | VCC33A |
| AB16 | AC7 |
| AB17 | AC8 |
| AB18 | VCC33A |
| AB19 | AC9 |
| AB20 | ADCGNDREF |

| FG676 | |
|---|---|
| Pin Number | AFS1500 Function |
| AB21 | PTBASE |
| AB22 | GNDNVM |
| AB23 | VCCNVM |
| AB24 | VPUMP |
| AB25 | NC |
| AB26 | GND |
| AC1 | NC |
| AC2 | NC |
| AC3 | NC |
| AC4 | GND |
| AC5 | VCCIB4 |
| AC6 | VCCIB4 |
| AC7 | PCAP |
| AC8 | AG0 |
| AC9 | GNDA |
| AC10 | AG1 |
| AC11 | AG2 |
| AC12 | GNDA |
| AC13 | AG3 |
| AC14 | AG6 |
| AC15 | GNDA |
| AC16 | AG7 |
| AC17 | AG8 |
| AC18 | GNDA |
| AC19 | AG9 |
| AC20 | VAREF |
| AC21 | VCCIB2 |
| AC22 | PTEM |
| AC23 | GND |
| AC24 | NC |
| AC25 | NC |
| AC26 | NC |
| AD1 | NC |
| AD2 | NC |
| AD3 | GND |
| AD4 | NC |

| Revision | Changes | Page |
|---|---|---|
| Advance v0.8 (continued) | The voltage range in the "VPUMP Programming Supply Voltage" section was updated. The parenthetical reference to "pulled up" was removed from the statement, "VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and 3.6 V." | 2-225 |
| | The "ATRTNx Temperature Monitor Return" section was updated with information about grounding and floating the pin. | 2-226 |
| | The following text was deleted from the "VREF I/O Voltage Reference" section: (all digital I/O). | 2-225 |
| | The "NCAP Negative Capacitor" section and "PCAP Positive Capacitor" section were updated to include information about the type of capacitor that is required to connect the two. | 2-228 |
| | 1 µF was changed to 100 pF in the "XTAL1 Crystal Oscillator Circuit Input". | 2-228 |
| | The "Programming" section was updated to include information about $V_{CCOSC}$. | 2-229 |
| | The VMV pins have now been tied internally with the $V_{CCI}$ pins. | N/A |
| | The AFS090"108-Pin QFN" table was updated. | 3-2 |
| | The AFS090 and AFS250 devices were updated in the "108-Pin QFN" table. | 3-2 |
| | The AFS250 device was updated in the "208-Pin PQFP" table. | 3-8 |
| | The AFS600 device was updated in the "208-Pin PQFP" table. | 3-8 |
| | The AFS090, AFS250, AFS600, and AFS1500 devices were updated in the "256-Pin FBGA" table. | 3-12 |
| | The AFS600 and AFS1500 devices were updated in the "484-Pin FBGA" table. | 3-20 |
| Advance v0.7 (January 2007) | The AFS600 device was updated in the "676-Pin FBGA" table. | 3-28 |
| | The AFS1500 digital I/O count was updated in the "Fusion Family" table. | I |
| | The AFS1500 digital I/O count was updated in the "Package I/Os: Single-/Double-Ended (Analog)" table. | II |
| Advance v0.6 (October 2006) | The second paragraph of the "PLL Macro" section was updated to include information about POWERDOWN. | 2-30 |
| | The description for bit 0 was updated in Table 2-17 · RTC Control/Status Register. | 2-38 |
| | 3.9 was changed to 7.8 in the "Crystal Oscillator (Xtal Osc)" section. | 2-40. |
| | All function descriptions in Table 2-18 · Signals for VRPSM Macro. | 2-42 |
| | In Table 2-19 • Flash Memory Block Pin Names, the RD[31:0] description was updated. | 2-43 |
| | The "RESET" section was updated. | 2-61 |
| | The "RESET" section was updated. | 2-64 |
| | Table 2-35 • FIFO was updated. | 2-79 |
| | The VAREF function description was updated in Table 2-36 • Analog Block Pin Description. | 2-82 |
| | The "Voltage Monitor" section was updated to include information about low power mode and sleep mode. | 2-86 |
| | The text in the "Current Monitor" section was changed from 2 mV to 1 mV. | 2-90 |
| | The "Gate Driver" section was updated to include information about forcing 1 V on the drain. | 2-94 |

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