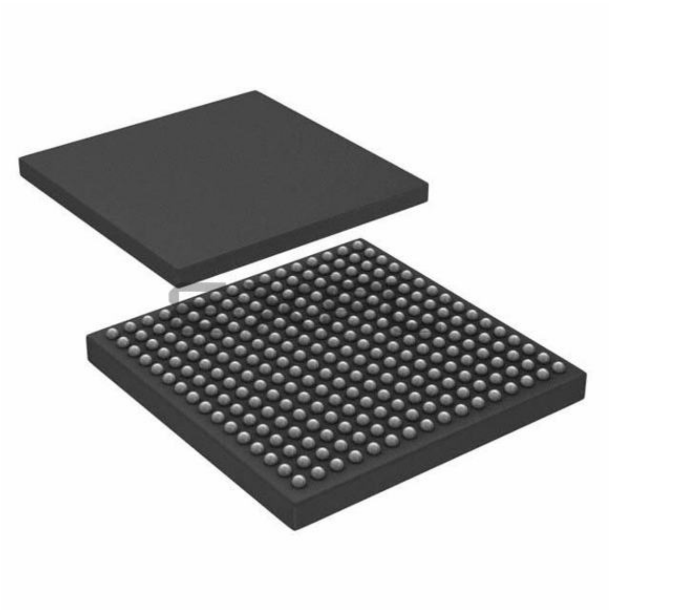

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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 276480 |
| Number of I/O | 119 |
| Number of Gates | 1500000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/afs1500-fg256i |

The FlashPoint tool in the Fusion development software solutions, Libero SoC and Designer, has extensive support for flash memory blocks and FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using the Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

### SRAM and FIFO

Fusion devices have embedded SRAM blocks along the north and south sides of the device. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be written through a 4-bit port and read as a single bitstream. The SRAM blocks can be initialized from the flash memory blocks or via the device JTAG port (ROM emulation mode), using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal EMPTY and FULL flags. The embedded FIFO control unit contains the counters necessary for the generation of the read and write address pointers. The SRAM/FIFO blocks can be cascaded to create larger configurations.

## Clock Resources

### PLLs and Clock Conditioning Circuits (CCCs)

Fusion devices provide designers with very flexible clock conditioning capabilities. Each member of the Fusion family contains six CCCs. In the two larger family members, two of these CCCs also include a PLL; the smaller devices support one PLL.

The inputs of the CCC blocks are accessible from the FPGA core or from one of several inputs with dedicated CCC block connections.

The CCC block has the following key features:

- Wide input frequency range ($f_{IN\_CCC}$) = 1.5 MHz to 350 MHz
- Output frequency range ($f_{OUT\_CCC}$) = 0.75 MHz to 350 MHz
- Clock phase adjustment via programmable and fixed delays from –6.275 ns to +8.75 ns
- Clock skew minimization (PLL)
- Clock frequency synthesis (PLL)
- On-chip analog clocking resources usable as inputs:
  - 100 MHz on-chip RC oscillator
  - Crystal oscillator

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°
- Output duty cycle = 50% ± 1.5%
- Low output jitter. Samples of peak-to-peak period jitter when a single global network is used:
  - 70 ps at 350 MHz
  - 90 ps at 100 MHz
  - 180 ps at 24 MHz
  - Worst case < 2.5% × clock period
- Maximum acquisition time = 150 µs
- Low power consumption of 5 mW

# Real-Time Counter System

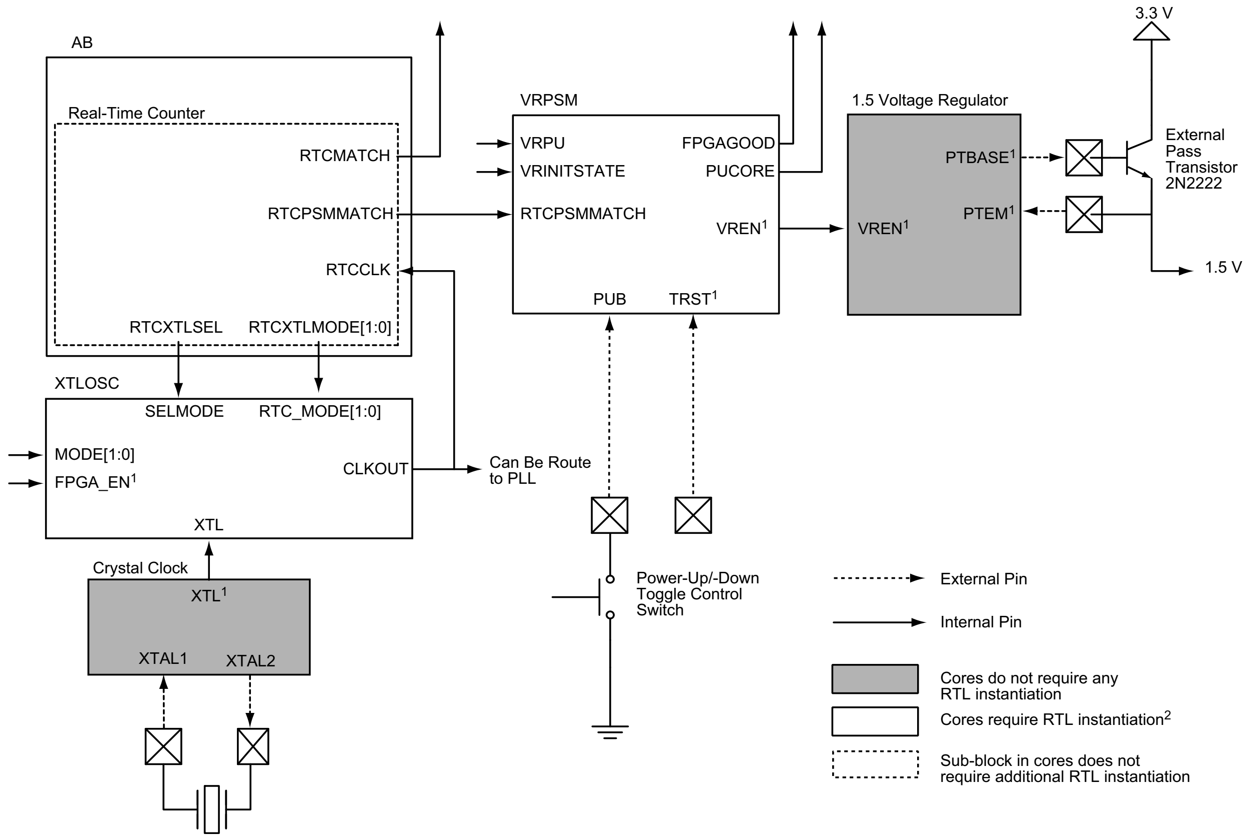
The RTC system enables Fusion devices to support standby and sleep modes of operation to reduce power consumption in many applications.

- Sleep mode, typical 10 µA
- Standby mode (RTC running), typical 3 mA with 20 MHz

The RTC system is composed of five cores:

- RTC sub-block inside Analog Block (AB)
- Voltage Regulator and Power System Monitor (VRPSM)
- Crystal oscillator (XTLOSC); refer to the "Crystal Oscillator" section in the Fusion Clock Resources chapter of the *Fusion FPGA Fabric User Guide* for more detail.
- Crystal clock; does not require instantiation in RTL
- 1.5 V voltage regulator; does not require instantiation in RTL

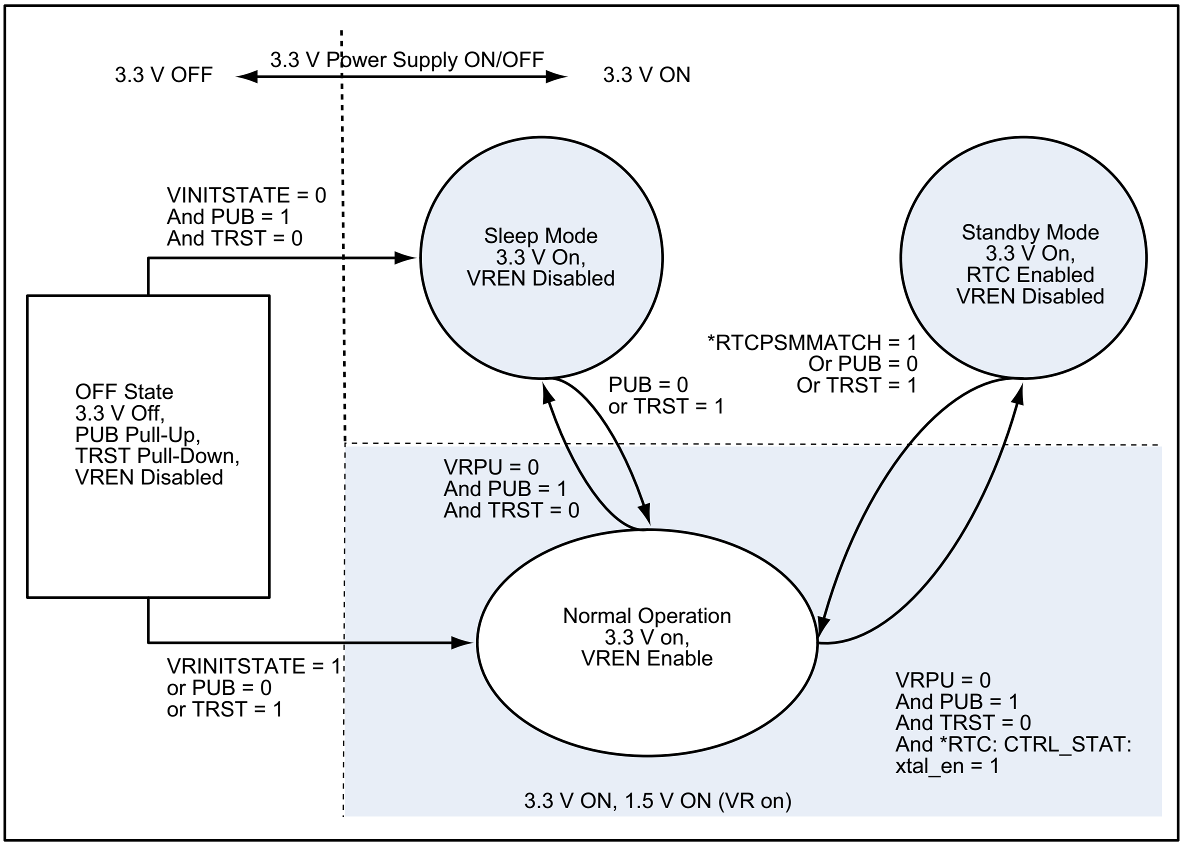
All cores are powered by 3.3 V supplies, so the RTC system is operational without a 1.5 V supply during standby mode. Figure 2-27 shows their connection.




*Notes:*

1. *Signals are hardwired internally and do not exist in the macro core.*
2. *User is only required to instantiate the VRPSM macro if the user wishes to specify PUPO behavior of the voltage regulator to be different from the default, or employ user logic to shut the voltage regulator off.*

***Figure 2-27 •* Real-Time Counter System (not all the signals are shown for the AB macro)**




Note: ** To enter and exit standby mode without any external stimulus on PUB or TRST, the vr_en_mat in the CTRL_STAT register must also be set to 1, so that RTCPSMMATCH will assert when a match occurs; hence the device exits standby mode.*

***Figure 2-31* • State Diagram for All Different Power Modes**

When TRST is 1 or PUB is 0, the 1.5 V voltage regulator is always ON, putting the Fusion device in normal operation at all times. Therefore, when the JTAG port is not in reset, the Fusion device cannot enter sleep mode or standby mode.

To enter standby mode, the Fusion device must first power-up into normal operation. The RTC is enabled through the RTC Control/Status Register described in the "Real-Time Counter (part of AB macro)" section on page 2-33. A match value corresponding to the wake-up time is loaded into the Match Register. The 1.5 V voltage regulator is disabled by setting VRPU to 0 to allow the Fusion device to enter standby mode, when the 1.5 V supply is off but the RTC remains on.

## ADC Description

The Fusion ADC is a 12-bit SAR ADC. It offers a wide variety of features for different use models. Figure 2-80 shows a block diagram of the Fusion ADC.

- Configurable resolution: 8-bit, 10-bit, and 12-bit mode
- DNL: 0.6 LSB for 10-bit mode
- INL: 0.4 LSB for 10-bit mode
- No missing code
- Internal VAREF = 2.56 V
- Maximum Sample Rate = 600 Ksps
- Power-up calibration and dynamic calibration after every sample to compensate for temperature drift over time

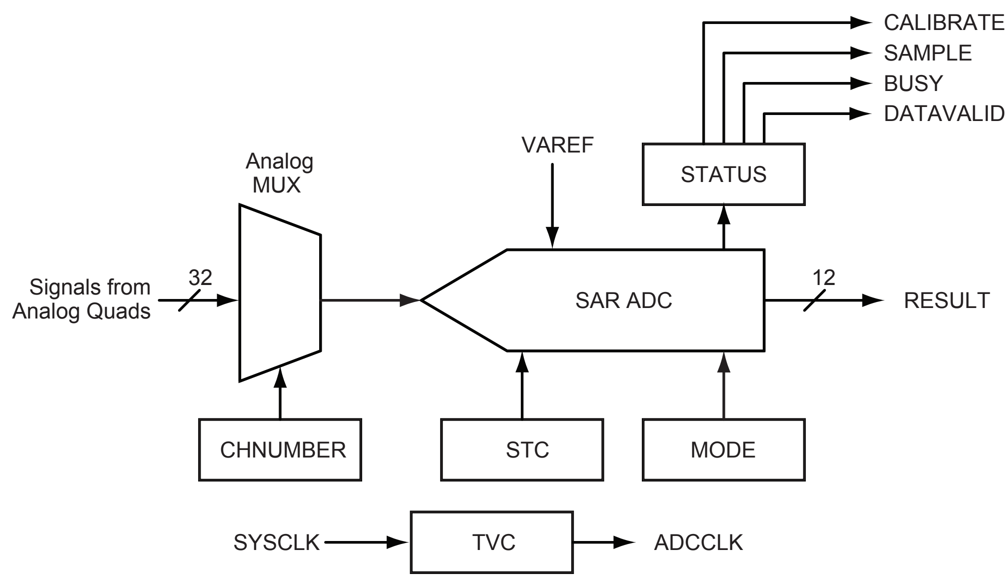



***Figure 2-80*** **• ADC Simplified Block Diagram**

## ADC Theory of Operation

An analog-to-digital converter is used to capture discrete samples of a continuous analog voltage and provide a discrete binary representation of the signal. Analog-to-digital converters are generally characterized in three ways:

- Input voltage range
- Resolution
- Bandwidth or conversion rate

The input voltage range of an ADC is determined by its reference voltage (VREF). Fusion devices include an internal 2.56 V reference, or the user can supply an external reference of up to 3.3 V. The following examples use the internal 2.56 V reference, so the full-scale input range of the ADC is 0 to 2.56 V.

The resolution (LSB) of the ADC is a function of the number of binary bits in the converter. The ADC approximates the value of the input voltage using 2n steps, where n is the number of bits in the converter. Each step therefore represents VREF÷ 2n volts. In the case of the Fusion ADC configured for 12-bit operation, the LSB is 2.56 V / 4096 = 0.625 mV.

Finally, bandwidth is an indication of the maximum number of conversions the ADC can perform each second. The bandwidth of an ADC is constrained by its architecture and several key performance characteristics.

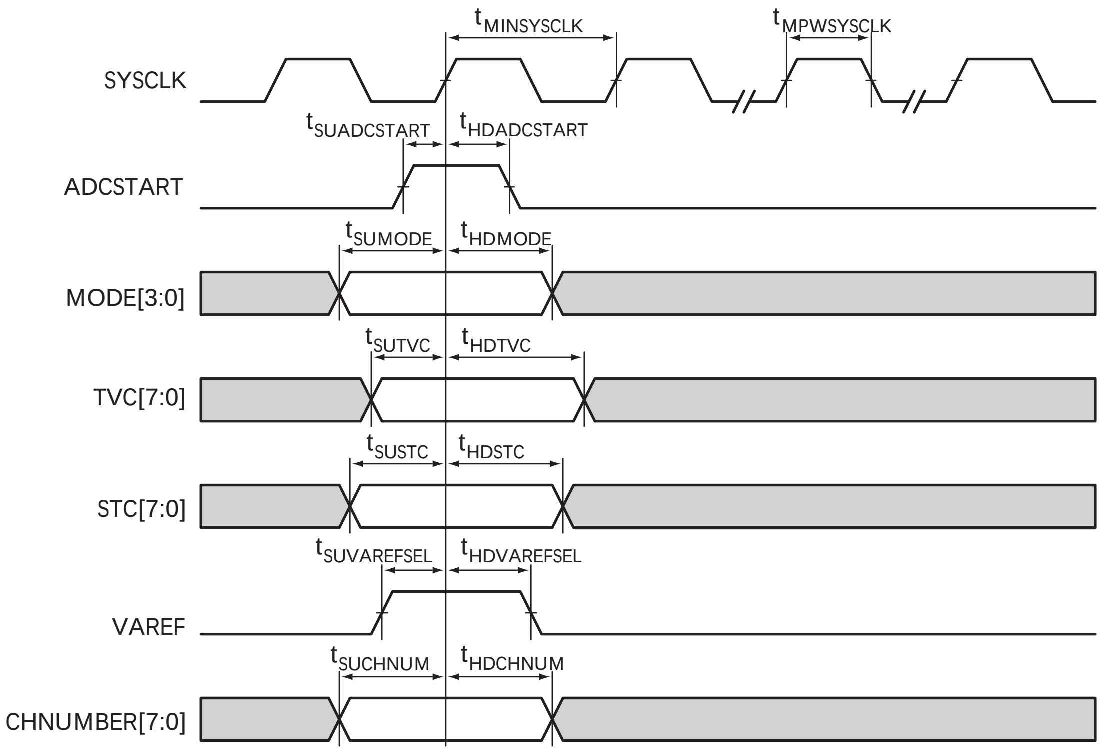
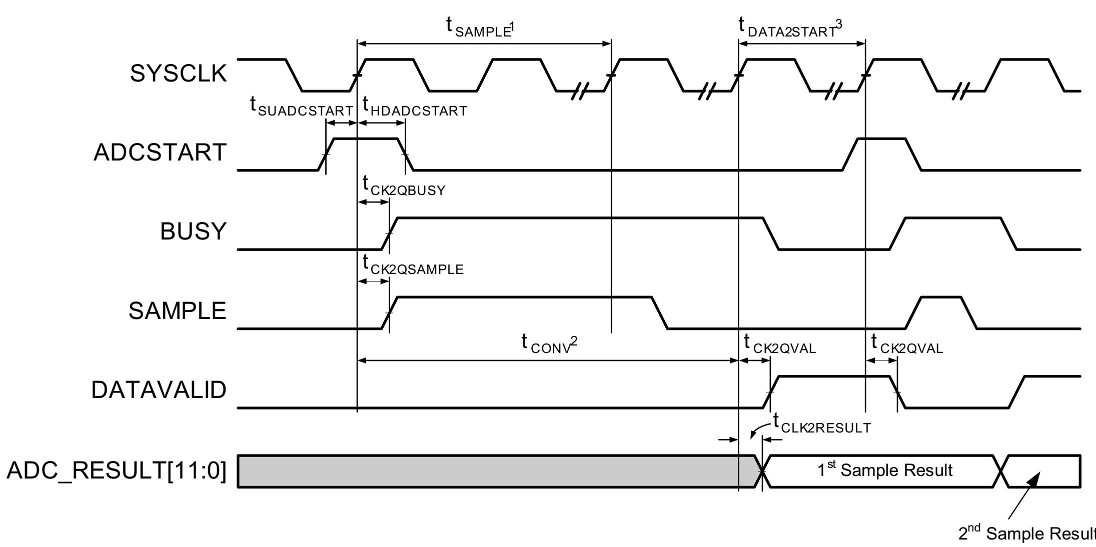



***Figure 2-90*** **• Input Setup Time**

***Standard Conversion***




*Notes:*

1. *Refer to EQ 20 on page 2-109 for the calculation on the sample time,* $t_{SAMPLE}$.
2. *See EQ 23 on page 2-109 for calculation of the conversion time,* $t_{CONV}$.
3. *Minimum time to issue an ADCSTART after DATAVALID is 1 SYSCLK period*

***Figure 2-91*** **• Standard Conversion Status Signal Timing Diagram**

### ADC Interface Timing

**Table 2-48 • ADC Interface Timing**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{SUMODE}$ | Mode Pin Setup Time | 0.56 | 0.64 | 0.75 | ns |
| $t_{HDMODE}$ | Mode Pin Hold Time | 0.26 | 0.29 | 0.34 | ns |
| $t_{SUTVC}$ | Clock Divide Control (TVC) Setup Time | 0.68 | 0.77 | 0.90 | ns |
| $t_{HDTVC}$ | Clock Divide Control (TVC) Hold Time | 0.32 | 0.36 | 0.43 | ns |
| $t_{SUSTC}$ | Sample Time Control (STC) Setup Time | 1.58 | 1.79 | 2.11 | ns |
| $t_{HDSTC}$ | Sample Time Control (STC) Hold Time | 1.27 | 1.45 | 1.71 | ns |
| $t_{SUVAREFSEL}$ | Voltage Reference Select (VAREFSEL) Setup Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{HDVAREFSEL}$ | Voltage Reference Select (VAREFSEL) Hold Time | 0.67 | 0.76 | 0.89 | ns |
| $t_{SUCHNUM}$ | Channel Select (CHNUMBER) Setup Time | 0.90 | 1.03 | 1.21 | ns |
| $t_{HDCHNUM}$ | Channel Select (CHNUMBER) Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUADCSTART}$ | Start of Conversion (ADCSTART) Setup Time | 0.75 | 0.85 | 1.00 | ns |
| $t_{HDADCSTART}$ | Start of Conversion (ADCSTART) Hold Time | 0.43 | 0.49 | 0.57 | ns |
| $t_{CK2QBUSY}$ | Busy Clock-to-Q | 1.33 | 1.51 | 1.78 | ns |
| $t_{CK2QCAL}$ | Power-Up Calibration Clock-to-Q | 0.63 | 0.71 | 0.84 | ns |
| $t_{CK2QVAL}$ | Valid Conversion Result Clock-to-Q | 3.12 | 3.55 | 4.17 | ns |
| $t_{CK2QSAMPLE}$ | Sample Clock-to-Q | 0.22 | 0.25 | 0.30 | ns |
| $t_{CK2QRESULT}$ | Conversion Result Clock-to-Q | 2.53 | 2.89 | 3.39 | ns |
| $t_{CLR2QBUSY}$ | Busy Clear-to-Q | 2.06 | 2.35 | 2.76 | ns |
| $t_{CLR2QCAL}$ | Power-Up Calibration Clear-to-Q | 2.15 | 2.45 | 2.88 | ns |
| $t_{CLR2QVAL}$ | Valid Conversion Result Clear-to-Q | 2.41 | 2.74 | 3.22 | ns |
| $t_{CLR2QSAMPLE}$ | Sample Clear-to-Q | 2.17 | 2.48 | 2.91 | ns |
| $t_{CLR2QRESULT}$ | Conversion result Clear-to-Q | 2.25 | 2.56 | 3.01 | ns |
| $t_{RECCLR}$ | Recovery Time of Clear | 0.00 | 0.00 | 0.00 | ns |
| $t_{REMCLR}$ | Removal Time of Clear | 0.63 | 0.72 | 0.84 | ns |
| $t_{MPWSYSCLK}$ | Clock Minimum Pulse Width for the ADC | 4.00 | 4.00 | 4.00 | ns |
| $t_{FMAXSYSCLK}$ | Clock Maximum Frequency for the ADC | 100.00 | 100.00 | 100.00 | MHz |

**Table 2-50 • ADC Characteristics in Direct Input Mode (continued)**
**Commercial Temperature Range Conditions, $T_J$ = 85°C (unless noted otherwise),**
**Typical: VCC33A = 3.3 V, VCC = 1.5 V**

| Parameter | Description | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Dynamic Performance** | | | | | | |
| SNR | Signal-to-Noise Ratio | 8-bit mode | 48.0 | 49.5 | | dB |
| | | 10-bit mode | 58.0 | 60.0 | | dB |
| | | 12-bit mode | 62.9 | 64.5 | | dB |
| SINAD | Signal-to-Noise Distortion | 8-bit mode | 47.6 | 49.5 | | dB |
| | | 10-bit mode | 57.4 | 59.8 | | dB |
| | | 12-bit mode | 62.0 | 64.2 | | dB |
| THD | Total Harmonic Distortion | 8-bit mode | | –74.4 | –63.0 | dBc |
| | | 10-bit mode | | –78.3 | –63.0 | dBc |
| | | 12-bit mode | | –77.9 | –64.4 | dBc |
| ENOB | Effective Number of Bits | 8-bit mode | 7.6 | 7.9 | | bits |
| | | 10-bit mode | 9.5 | 9.6 | | bits |
| | | 12-bit mode | 10.0 | 10.4 | | bits |
| **Conversion Rate** | | | | | | |
| | Conversion Time | 8-bit mode | 1.7 | | | µs |
| | | 10-bit mode | 1.8 | | | µs |
| | | 12-bit mode | 2 | | | µs |
| | Sample Rate | 8-bit mode | | | 600 | Ksps |
| | | 10-bit mode | | | 550 | Ksps |
| | | 12-bit mode | | | 500 | Ksps |

*Notes:*

1. *Accuracy of the external reference is 2.56 V ± 4.6 mV.*
2. *Data is based on characterization.*
3. *The sample rate is time-shared among active analog inputs.*

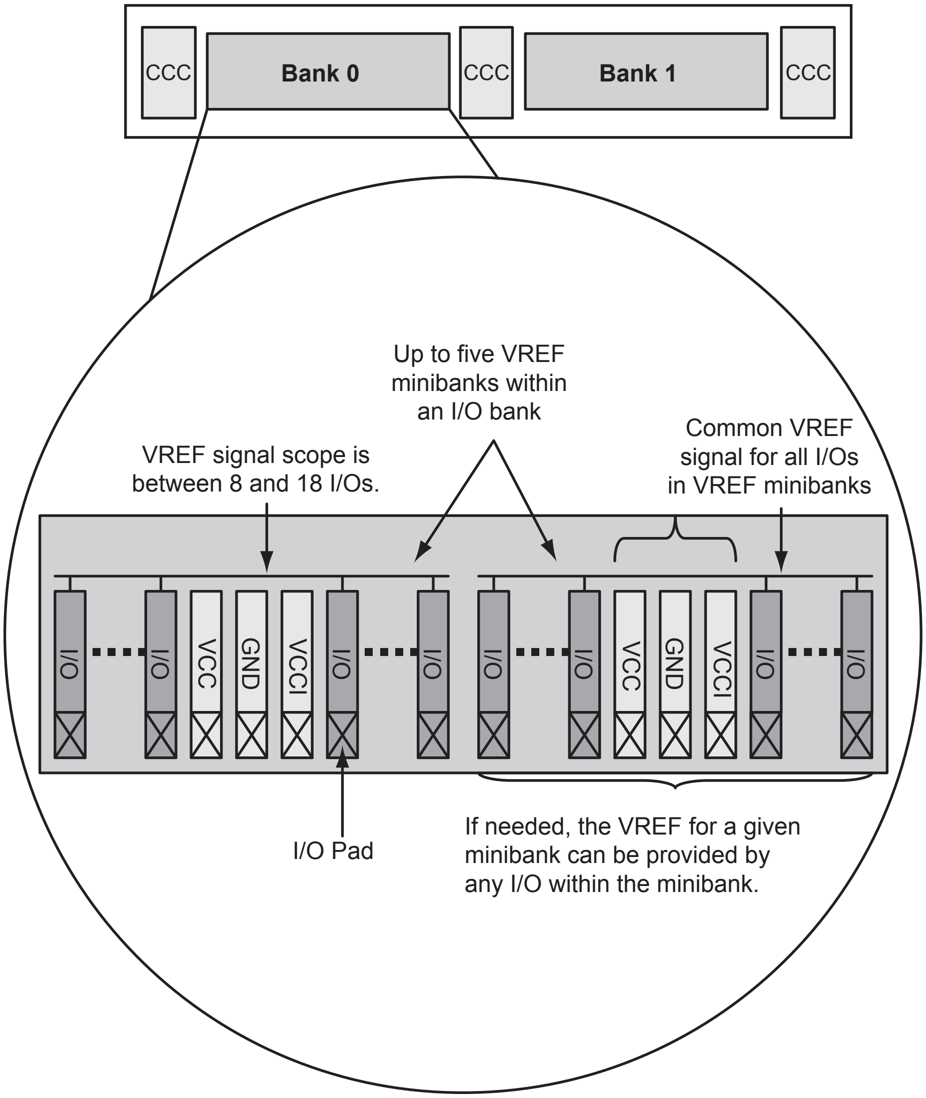



***Figure 2-99* • Fusion Pro I/O Bank Detail Showing VREF Minibanks (north side ofAFS600 and AFS1500)**

***Table 2-67* • I/O Standards Supported by Bank Type**

| I/O Bank | Single-Ended I/O Standards | Differential I/O Standards | Voltage-Referenced | Hot-Swap |
|---|---|---|---|---|
| Standard I/O | LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V | – | – | Yes |
| Advanced I/O | LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V, 3.3 V PCI / 3.3 V PCI-X | LVPECL and LVDS | – | – |
| Pro I/O | LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V, 3.3 V PCI / 3.3 V PCI-X | LVPECL and LVDS | GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II | Yes |

## Overview of I/O Performance

### Summary of I/O DC Input and Output Levels – Default I/O Software Settings

**Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions Applicable to Pro I/Os**

| | | | VIL | | VIH | | VOL | VOH | IOL | IOH |
|---|---|---|---|---|---|---|---|---|---|---|
| I/O Standard | Drive Strength | Slew Rate | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA |
| 3.3 V LVTTL / 3.3 V LVCMOS | 12 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 |
| 2.5 V LVCMOS | 12 mA | High | –0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 12 | 12 |
| 1.8 V LVCMOS | 12 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 12 | 12 |
| 1.5 V LVCMOS | 12 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 |
| 3.3 V PCI | Per PCI Specification | | | | | | | | | |
| 3.3 V PCI-X | Per PCI-X Specification | | | | | | | | | |
| 3.3 V GTL | 20 mA[2] | High | –0.3 | VREF – 0.05 | VREF + 0.05 | 3.6 | 0.4 | – | 20 | 20 |
| 2.5 V GTL | 20 mA[2] | High | –0.3 | VREF – 0.05 | VREF + 0.05 | 3.6 | 0.4 | – | 20 | 20 |
| 3.3 V GTL+ | 35 mA | High | –0.3 | VREF – 0.1 | VREF + 0.1 | 3.6 | 0.6 | – | 35 | 35 |
| 2.5 V GTL+ | 33 mA | High | –0.3 | VREF – 0.1 | VREF + 0.1 | 3.6 | 0.6 | – | 33 | 33 |
| HSTL (I) | 8 mA | High | –0.3 | VREF – 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI – 0.4 | 8 | 8 |
| HSTL (II) | 15 mA[2] | High | –0.3 | VREF – 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI – 0.4 | 15 | 15 |
| SSTL2 (I) | 15 mA | High | –0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | 0.54 | VCCI – 0.62 | 15 | 15 |
| SSTL2 (II) | 18 mA | High | –0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | 0.35 | VCCI – 0.43 | 18 | 18 |
| SSTL3 (I) | 14 mA | High | –0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | 0.7 | VCCI – 1.1 | 14 | 14 |
| SSTL3 (II) | 21 mA | High | –0.3 | VREF – 0.2 | VREF + 0.2 | 3.6 | 0.5 | VCCI – 0.9 | 21 | 21 |

*Notes:*

1. *Currents are measured at 85°C junction temperature.*
2. *Output drive strength is below JEDEC specification.*
3. *Output slew rate can be extracted by the IBIS models.*

**Table 2-87 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions Applicable to Advanced I/Os**

| | | | VIL | | VIH | | VOL | VOH | IOL | IOH |
|---|---|---|---|---|---|---|---|---|---|---|
| I/O Standard | Drive Strength | Slew Rate | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA |
| 3.3 V LVTTL / 3.3 V LVCMOS | 12 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 |
| 2.5 V LVCMOS | 12 mA | High | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 12 | 12 |
| 1.8 V LVCMOS | 12 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 12 | 12 |
| 1.5 V LVCMOS | 12 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 |
| 3.3 V PCI | Per PCI specifications | | | | | | | | | |
| 3.3 V PCI-X | Per PCI-X specifications | | | | | | | | | |

*Note: Currents are measured at 85°C junction temperature.*

## Detailed I/O DC Characteristics

***Table 2-95* • Input Capacitance**

| Symbol | Definition | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | VIN = 0, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on the clock pin | VIN = 0, f = 1.0 MHz | | 8 | pF |

***Table 2-96* • I/O Output Buffer Maximum Resistances [1]**

| Standard | Drive Strength | $R_{PULL-DOWN}$ (ohms) [2] | $R_{PULL-UP}$ (ohms) [3] |
|---|---|---|---|
| **Applicable to Pro I/O Banks** | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 4 mA | 100 | 300 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 17 | 50 |
| | 24 mA | 11 | 33 |
| 2.5 V LVCMOS | 4 mA | 100 | 200 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |
| | 16 mA | 20 | 40 |
| | 24 mA | 11 | 22 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| | 12 mA | 20 | 22 |
| | 16 mA | 20 | 22 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| | 6 mA | 67 | 75 |
| | 8 mA | 33 | 37 |
| | 12 mA | 33 | 37 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 25 | 75 |
| 3.3 V GTL | 20 mA | 11 | – |
| 2.5 V GTL | 20 mA | 14 | – |
| 3.3 V GTL+ | 35 mA | 12 | – |
| 2.5 V GTL+ | 33 mA | 15 | – |

*Notes:*

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/techdocs/models/ibis.html.*
2. $R_{(PULL-DOWN-MAX)} = VOLspec / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (VCCImax – VOHspec) / IOHspec$

*Table 2-99* **• Short Current Event Duration before Failure**

| Temperature | Time Before Failure |
|---|---|
| –40°C | >20 years |
| 0°C | >20 years |
| 25°C | >20 years |
| 70°C | 5 years |
| 85°C | 2 years |
| 100°C | 6 months |

*Table 2-100* **• Schmitt Trigger Input Hysteresis**
**Hysteresis Voltage Value (typ.) for Schmitt Mode Input Buffers**

| Input Buffer Configuration | Hysteresis Value (typ.) |
|---|---|
| 3.3 V LVTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode) | 240 mV |
| 2.5 V LVCMOS (Schmitt trigger mode) | 140 mV |
| 1.8 V LVCMOS (Schmitt trigger mode) | 80 mV |
| 1.5 V LVCMOS (Schmitt trigger mode) | 60 mV |

*Table 2-101* **• I/O Input Rise Time, Fall Time, and Related I/O Reliability**

| Input Buffer | Input Rise/Fall Time (min.) | Input Rise/Fall Time (max.) | Reliability |
|---|---|---|---|
| LVTTL/LVCMOS (Schmitt trigger disabled) | No requirement | 10 ns* | 20 years (100°C) |
| LVTTL/LVCMOS (Schmitt trigger enabled) | No requirement | No requirement, but input noise voltage cannot exceed Schmitt hysteresis | 20 years (100°C) |
| HSTL/SSTL/GTL | No requirement | 10 ns* | 10 years (100°C) |
| LVDS/BLVDS/M-LVDS/LVPECL | No requirement | 10 ns* | 10 years (100°C) |

*Note: * The maximum input rise/fall time is related only to the noise induced into the input buffer trace. If the noise is low, the rise time and fall time of input buffers, when Schmitt trigger is disabled, can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure there is no excessive noise coupling into input signals.*

***Table 2-106* • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Advanced I/Os**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 0.66 | 10.26 | 0.04 | 1.20 | 0.43 | 10.45 | 8.90 | 2.64 | 2.46 | 12.68 | 11.13 | ns |
| | –1 | 0.56 | 8.72 | 0.04 | 1.02 | 0.36 | 8.89 | 7.57 | 2.25 | 2.09 | 10.79 | 9.47 | ns |
| | –2 | 0.49 | 7.66 | 0.03 | 0.90 | 0.32 | 7.80 | 6.64 | 1.98 | 1.83 | 9.47 | 8.31 | ns |
| 8 mA | Std. | 0.66 | 7.27 | 0.04 | 1.20 | 0.43 | 7.41 | 6.28 | 2.98 | 3.04 | 9.65 | 8.52 | ns |
| | –1 | 0.56 | 6.19 | 0.04 | 1.02 | 0.36 | 6.30 | 5.35 | 2.54 | 2.59 | 8.20 | 7.25 | ns |
| | –2 | 0.49 | 5.43 | 0.03 | 0.90 | 0.32 | 5.53 | 4.69 | 2.23 | 2.27 | 7.20 | 6.36 | ns |
| 12 mA | Std. | 0.66 | 5.58 | 0.04 | 1.20 | 0.43 | 5.68 | 4.87 | 3.21 | 3.42 | 7.92 | 7.11 | ns |
| | –1 | 0.56 | 4.75 | 0.04 | 1.02 | 0.36 | 4.84 | 4.14 | 2.73 | 2.91 | 6.74 | 6.05 | ns |
| | –2 | 0.49 | 4.17 | 0.03 | 0.90 | 0.32 | 4.24 | 3.64 | 2.39 | 2.55 | 5.91 | 5.31 | ns |
| 16 mA | Std. | 0.66 | 5.21 | 0.04 | 1.20 | 0.43 | 5.30 | 4.56 | 3.26 | 3.51 | 7.54 | 6.80 | ns |
| | –1 | 0.56 | 4.43 | 0.04 | 1.02 | 0.36 | 4.51 | 3.88 | 2.77 | 2.99 | 6.41 | 5.79 | ns |
| | –2 | 0.49 | 3.89 | 0.03 | 0.90 | 0.32 | 3.96 | 3.41 | 2.43 | 2.62 | 5.63 | 5.08 | ns |
| 24 mA | Std. | 0.66 | 4.85 | 0.04 | 1.20 | 0.43 | 4.94 | 4.54 | 3.32 | 3.88 | 7.18 | 6.78 | ns |
| | –1 | 0.56 | 4.13 | 0.04 | 1.02 | 0.36 | 4.20 | 3.87 | 2.82 | 3.30 | 6.10 | 5.77 | ns |
| | –2 | 0.49 | 3.62 | 0.03 | 0.90 | 0.32 | 3.69 | 3.39 | 2.48 | 2.90 | 5.36 | 5.06 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

**Table 2-130 • 1.5 V LVCMOS Low Slew**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V**
**Applicable to Advanced I/Os**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 12.78 | 0.04 | 1.31 | 0.43 | 12.81 | 12.78 | 3.40 | 2.64 | 15.05 | 15.02 | ns |
| | –1 | 0.56 | 10.87 | 0.04 | 1.11 | 0.36 | 10.90 | 10.87 | 2.89 | 2.25 | 12.80 | 12.78 | ns |
| | –2 | 0.49 | 9.55 | 0.03 | 0.98 | 0.32 | 9.57 | 9.55 | 2.54 | 1.97 | 11.24 | 11.22 | ns |
| 4 mA | Std. | 0.66 | 10.01 | 0.04 | 1.31 | 0.43 | 10.19 | 9.55 | 3.75 | 3.27 | 12.43 | 11.78 | ns |
| | –1 | 0.56 | 8.51 | 0.04 | 1.11 | 0.36 | 8.67 | 8.12 | 3.19 | 2.78 | 10.57 | 10.02 | ns |
| | –2 | 0.49 | 7.47 | 0.03 | 0.98 | 0.32 | 7.61 | 7.13 | 2.80 | 2.44 | 9.28 | 8.80 | ns |
| 8 mA | Std. | 0.66 | 9.33 | 0.04 | 1.31 | 0.43 | 9.51 | 8.89 | 3.83 | 3.43 | 11.74 | 11.13 | ns |
| | –1 | 0.56 | 7.94 | 0.04 | 1.11 | 0.36 | 8.09 | 7.56 | 3.26 | 2.92 | 9.99 | 9.47 | ns |
| | –2 | 0.49 | 6.97 | 0.03 | 0.98 | 0.32 | 7.10 | 6.64 | 2.86 | 2.56 | 8.77 | 8.31 | ns |
| 12 mA | Std. | 0.66 | 8.91 | 0.04 | 1.31 | 0.43 | 9.07 | 8.89 | 3.95 | 4.05 | 11.31 | 11.13 | ns |
| | –1 | 0.56 | 7.58 | 0.04 | 1.11 | 0.36 | 7.72 | 7.57 | 3.36 | 3.44 | 9.62 | 9.47 | ns |
| | –2 | 0.49 | 6.65 | 0.03 | 0.98 | 0.32 | 6.78 | 6.64 | 2.95 | 3.02 | 8.45 | 8.31 | ns |

*Note:* *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

**Table 2-131 • 1.5 V LVCMOS High Slew**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V**
**Applicable to Advanced I/Os**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 8.36 | 0.04 | 1.44 | 0.43 | 6.82 | 8.36 | 3.39 | 2.77 | 9.06 | 10.60 | ns |
| | –1 | 0.56 | 7.11 | 0.04 | 1.22 | 0.36 | 5.80 | 7.11 | 2.88 | 2.35 | 7.71 | 9.02 | ns |
| | –2 | 0.49 | 6.24 | 0.03 | 1.07 | 0.32 | 5.10 | 6.24 | 2.53 | 2.06 | 6.76 | 7.91 | ns |
| 4 mA | Std. | 0.66 | 5.31 | 0.04 | 1.44 | 0.43 | 4.85 | 5.31 | 3.74 | 3.40 | 7.09 | 7.55 | ns |
| | –1 | 0.56 | 4.52 | 0.04 | 1.22 | 0.36 | 4.13 | 4.52 | 3.18 | 2.89 | 6.03 | 6.42 | ns |
| | –2 | 0.49 | 3.97 | 0.03 | 1.07 | 0.32 | 3.62 | 3.97 | 2.79 | 2.54 | 5.29 | 5.64 | ns |
| 8 mA | Std. | 0.66 | 4.67 | 0.04 | 1.44 | 0.43 | 4.55 | 4.67 | 3.82 | 3.56 | 6.78 | 6.90 | ns |
| | –1 | 0.56 | 3.97 | 0.04 | 1.22 | 0.36 | 3.87 | 3.97 | 3.25 | 3.03 | 5.77 | 5.87 | ns |
| | –2 | 0.49 | 3.49 | 0.03 | 1.07 | 0.32 | 3.40 | 3.49 | 2.85 | 2.66 | 5.07 | 5.16 | ns |
| 12 mA | Std. | 0.66 | 4.08 | 0.04 | 1.44 | 0.43 | 4.15 | 3.58 | 3.94 | 4.20 | 6.39 | 5.81 | ns |
| | –1 | 0.56 | 3.47 | 0.04 | 1.22 | 0.36 | 3.53 | 3.04 | 3.36 | 3.58 | 5.44 | 4.95 | ns |
| | –2 | 0.49 | 3.05 | 0.03 | 1.07 | 0.32 | 3.10 | 2.67 | 2.95 | 3.14 | 4.77 | 4.34 | ns |

*Note:* *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

### HSTL Class II

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

***Table 2-153* • Minimum and Maximum DC Input and Output Levels**

| HSTL Class II | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | μA[4] | μA[4] |
| 15 mA[3] | –0.3 | VREF – 0.1 | VREF + 0.1 | 3.6 | 0.4 | VCCI – 0.4 | 15 | 15 | 55 | 66 | 10 | 10 |

*Note:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Output drive strength is below JEDEC specification.*

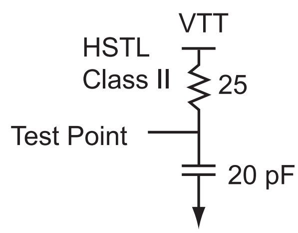



***Figure 2-129* • AC Loading**

***Table 2-154* • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|---|---|
| VREF – 0.1 | VREF + 0.1 | 0.75 | 0.75 | 0.75 | 20 |

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

#### *Timing Characteristics*

***Table 2-155* • HSTL Class II**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V, VREF = 0.75 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 3.02 | 0.04 | 2.12 | 0.43 | 3.08 | 2.71 | | | 5.32 | 4.95 | ns |
| –1 | 0.56 | 2.57 | 0.04 | 1.81 | 0.36 | 2.62 | 2.31 | | | 4.52 | 4.21 | ns |
| –2 | 0.49 | 2.26 | 0.03 | 1.59 | 0.32 | 2.30 | 2.03 | | | 3.97 | 3.70 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

### Input Register

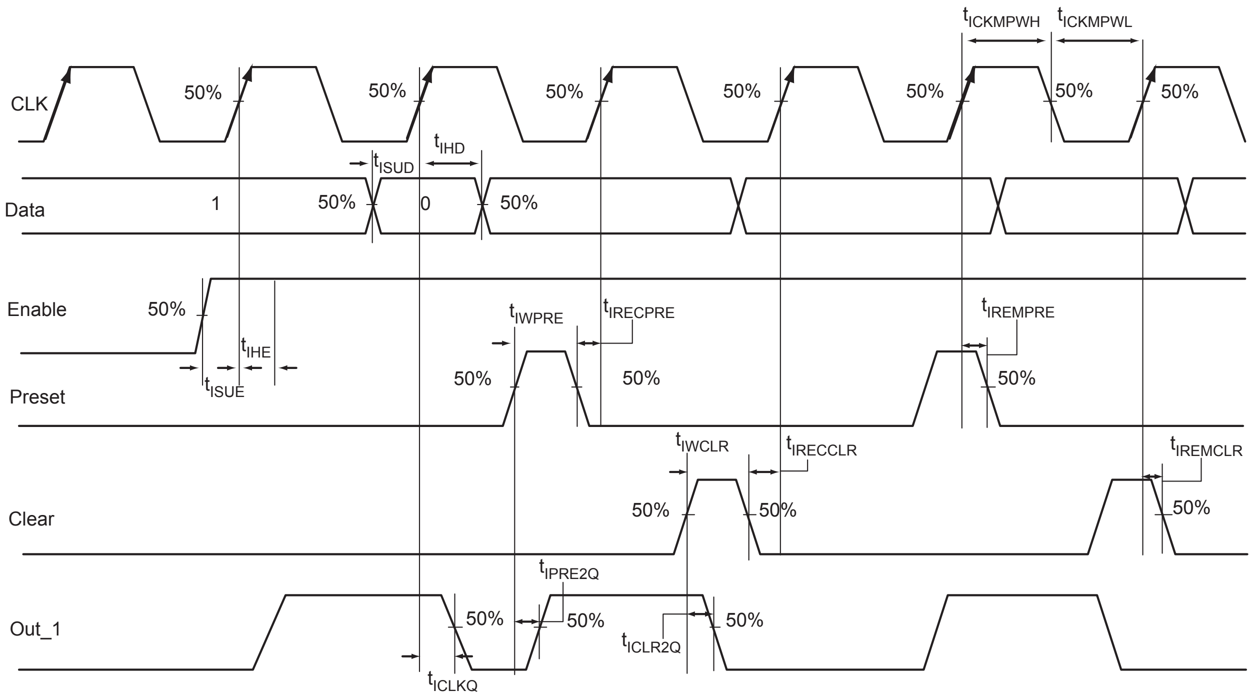



***Figure 2-139*** **• Input Register Timing Diagram**

#### *Timing Characteristics*

***Table 2-176*** **• Input Data Register Propagation Delays**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | 0.24 | 0.27 | 0.32 | ns |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | 0.26 | 0.30 | 0.35 | ns |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ISUE}$ | Enable Setup Time for the Input Data Register | 0.37 | 0.42 | 0.50 | ns |
| $t_{IHE}$ | Enable Hold Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | 0.45 | 0.52 | 0.61 | ns |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | 0.45 | 0.52 | 0.61 | ns |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{IWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{IWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width High for the Input Data Register | 0.36 | 0.41 | 0.48 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width Low for the Input Data Register | 0.32 | 0.37 | 0.43 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

## User-Defined Supply Pins

**VREF I/O Voltage Reference**

Reference voltage for I/O minibanks. Both AFS600 and AFS1500 (north bank only) support Microsemi Pro I/O. These I/O banks support voltage reference standard I/O. The VREF pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated as the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One VREF pin can support the number of I/Os available in its minibank.

**VAREF Analog Reference Voltage**

The Fusion device can be configured to generate a 2.56 V internal reference voltage that can be used by the ADC. While using the internal reference, the reference voltage is output on the VAREF pin for use as a system reference. If a different reference voltage is required, it can be supplied by an external source and applied to this pin. The valid range of values that can be supplied to the ADC is 1.0 V to 3.3 V. When VAREF is internally generated by the Fusion device, a bypass capacitor must be connected from this pin to ground. The value of the bypass capacitor should be between 3.3 μF and 22 μF, which is based on the needs of the individual designs. The choice of the capacitor value has an impact on the settling time it takes the VAREF signal to reach the required specification of 2.56 V to initiate valid conversions by the ADC. If the lower capacitor value is chosen, the settling time required for VAREF to achieve 2.56 V will be shorter than when selecting the larger capacitor value. The above range of capacitor values supports the accuracy specification of the ADC, which is detailed in the datasheet. Designers choosing the smaller capacitor value will not obtain as much margin in the accuracy as that achieved with a larger capacitor value. Depending on the capacitor value selected in the Analog System Builder, a tool in Libero SoC, an automatic delay circuit will be generated using logic tiles available within the FPGA to ensure that VAREF has achieved the 2.56 V value. Microsemi recommends customers use 10 μF as the value of the bypass capacitor. Designers choosing to use an external VAREF need to ensure that a stable and clean VAREF source is supplied to the VAREF pin before initiating conversions by the ADC. Designers should also make sure that the ADCRESET signal is deasserted before initiating valid conversions.[2]

If the user connects VAREF to external 3.3 V on their board, the internal VAREF driving OpAmp tries to bring the pin down to the nominal 2.56 V until the device is programmed and up/functional. Under this scenario, it is recommended to connect an external 3.3 V supply through a ~1 KOhm resistor to limit current, along with placing a 10-100nF capacitor between VAREF and GNDA.

## User Pins

**I/O User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected. Unused I/O pins are configured as inputs with pull-up resistors.

During programming, I/Os become tristated and weakly pulled up to VCCI. With the VCCI and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os get instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

**A*xy* Analog Input/Output**

Analog I/O pin, where *x* is the analog pad type (C = current pad, G = Gate driver pad, T = Temperature pad, V = Voltage pad) and *y* is the Analog Quad number (0 to 9). There is a minimum 1 MΩ to ground on AV, AC, and AT. This pin can be left floating when it is unused.

*2. The ADC is functional with an external reference down to 1V, however to meet the performance parameters highlighted in the datasheet refer to the VAREF specification in Table 3-2 on page 3-3.*

**Table 3-10 • AFS250 Quiescent Supply Current Characteristics (continued)**

| Parameter | Description | Conditions | Temp. | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| IPP | Programming supply current | Non-programming mode, VPUMP = 3.63 V | $T_J$ = 25°C | | 37 | 80 | µA |
| | | | $T_J$ = 85°C | | 37 | 80 | µA |
| | | | $T_J$ = 100°C | | 80 | 100 | µA |
| | | Standby mode[5] or Sleep mode[6], VPUMP = 0 V | | | 0 | 0 | µA |
| ICCNVM | Embedded NVM current | Reset asserted, VCCNVM = 1.575 V | $T_J$ = 25°C | | 10 | 40 | µA |
| | | | $T_J$ = 85°C | | 14 | 40 | µA |
| | | | $T_J$ = 100°C | | 14 | 40 | µA |
| ICCPLL | 1.5 V PLL quiescent current | Operational standby, VCCPLL = 1.575 V | $T_J$ = 25°C | | 65 | 100 | µA |
| | | | $T_J$ = 85°C | | 65 | 100 | µA |
| | | | $T_J$ = 100°C | | 65 | 100 | µA |

*Notes:*

1. *ICC is the 1.5 V power supplies, ICC, ICCPLL, ICC15A, ICCNVM.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, and ICCI2.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTA G = VPUMP = 0 V.*

| PQ208 | | |
|---|---|---|
| **Pin Number** | **AFS250 Function** | **AFS600 Function** |
| 74 | AV2 | AV4 |
| 75 | AC2 | AC4 |
| 76 | AG2 | AG4 |
| 77 | AT2 | AT4 |
| 78 | ATRTN1 | ATRTN2 |
| 79 | AT3 | AT5 |
| 80 | AG3 | AG5 |
| 81 | AC3 | AC5 |
| 82 | AV3 | AV5 |
| 83 | AV4 | AV6 |
| 84 | AC4 | AC6 |
| 85 | AG4 | AG6 |
| 86 | AT4 | AT6 |
| 87 | ATRTN2 | ATRTN3 |
| 88 | AT5 | AT7 |
| 89 | AG5 | AG7 |
| 90 | AC5 | AC7 |
| 91 | AV5 | AV7 |
| 92 | NC | AV8 |
| 93 | NC | AC8 |
| 94 | NC | AG8 |
| 95 | NC | AT8 |
| 96 | NC | ATRTN4 |
| 97 | NC | AT9 |
| 98 | NC | AG9 |
| 99 | NC | AC9 |
| 100 | NC | AV9 |
| 101 | GNDAQ | GNDAQ |
| 102 | VCC33A | VCC33A |
| 103 | ADCGNDREF | ADCGNDREF |
| 104 | VAREF | VAREF |
| 105 | PUB | PUB |
| 106 | VCC33A | VCC33A |
| 107 | GNDA | GNDA |
| 108 | PTEM | PTEM |
| 109 | PTBASE | PTBASE |
| 110 | GNDNVM | GNDNVM |

| PQ208 | | |
|---|---|---|
| **Pin Number** | **AFS250 Function** | **AFS600 Function** |
| 111 | VCCNVM | VCCNVM |
| 112 | VCC | VCC |
| 112 | VCC | VCC |
| 113 | VPUMP | VPUMP |
| 114 | GNDQ | NC |
| 115 | VCCIB1 | TCK |
| 116 | TCK | TDI |
| 117 | TDI | TMS |
| 118 | TMS | TDO |
| 119 | TDO | TRST |
| 120 | TRST | VJTAG |
| 121 | VJTAG | IO57NDB2V0 |
| 122 | IO57NDB1V0 | GDC2/IO57PDB2V0 |
| 123 | GDC2/IO57PDB1V0 | IO56NDB2V0 |
| 124 | IO56NDB1V0 | GDB2/IO56PDB2V0 |
| 125 | GDB2/IO56PDB1V0 | IO55NDB2V0 |
| 126 | VCCIB1 | GDA2/IO55PDB2V0 |
| 127 | GND | GDA0/IO54NDB2V0 |
| 128 | IO55NDB1V0 | GDA1/IO54PDB2V0 |
| 129 | GDA2/IO55PDB1V0 | VCCIB2 |
| 130 | GDA0/IO54NDB1V0 | GND |
| 131 | GDA1/IO54PDB1V0 | VCC |
| 132 | GDB0/IO53NDB1V0 | GCA0/IO45NDB2V0 |
| 133 | GDB1/IO53PDB1V0 | GCA1/IO45PDB2V0 |
| 134 | GDC0/IO52NDB1V0 | GCB0/IO44NDB2V0 |
| 135 | GDC1/IO52PDB1V0 | GCB1/IO44PDB2V0 |
| 136 | IO51NSB1V0 | GCC0/IO43NDB2V0 |
| 137 | VCCIB1 | GCC1/IO43PDB2V0 |
| 138 | GND | IO42NDB2V0 |
| 139 | VCC | IO42PDB2V0 |
| 140 | IO50NDB1V0 | IO41NDB2V0 |
| 141 | IO50PDB1V0 | GCC2/IO41PDB2V0 |
| 142 | GCA0/IO49NDB1V0 | VCCIB2 |
| 143 | GCA1/IO49PDB1V0 | GND |
| 144 | GCB0/IO48NDB1V0 | VCC |
| 145 | GCB1/IO48PDB1V0 | IO40NDB2V0 |
| 146 | GCC0/IO47NDB1V0 | GCB2/IO40PDB2V0 |

| FG256 | | | | |
|---|---|---|---|---|
| **Pin Number** | **AFS090 Function** | **AFS250 Function** | **AFS600 Function** | **AFS1500 Function** |
| H3 | XTAL2 | XTAL2 | XTAL2 | XTAL2 |
| H4 | XTAL1 | XTAL1 | XTAL1 | XTAL1 |
| H5 | GNDOSC | GNDOSC | GNDOSC | GNDOSC |
| H6 | VCCOSC | VCCOSC | VCCOSC | VCCOSC |
| H7 | VCC | VCC | VCC | VCC |
| H8 | GND | GND | GND | GND |
| H9 | VCC | VCC | VCC | VCC |
| H10 | GND | GND | GND | GND |
| H11 | GDC0/IO38NDB1V0 | IO51NDB1V0 | IO47NDB2V0 | IO69NDB2V0 |
| H12 | GDC1/IO38PDB1V0 | IO51PDB1V0 | IO47PDB2V0 | IO69PDB2V0 |
| H13 | GDB1/IO39PDB1V0 | GCA1/IO49PDB1V0 | GCA1/IO45PDB2V0 | GCA1/IO64PDB2V0 |
| H14 | GDB0/IO39NDB1V0 | GCA0/IO49NDB1V0 | GCA0/IO45NDB2V0 | GCA0/IO64NDB2V0 |
| H15 | GCA0/IO36NDB1V0 | GCB0/IO48NDB1V0 | GCB0/IO44NDB2V0 | GCB0/IO63NDB2V0 |
| H16 | GCA1/IO36PDB1V0 | GCB1/IO48PDB1V0 | GCB1/IO44PDB2V0 | GCB1/IO63PDB2V0 |
| J1 | GEA0/IO44NDB3V0 | GFA0/IO66NDB3V0 | GFA0/IO70NDB4V0 | GFA0/IO105NDB4V0 |
| J2 | GEA1/IO44PDB3V0 | GFA1/IO66PDB3V0 | GFA1/IO70PDB4V0 | GFA1/IO105PDB4V0 |
| J3 | IO43NDB3V0 | GFB0/IO67NDB3V0 | GFB0/IO71NDB4V0 | GFB0/IO106NDB4V0 |
| J4 | GEC2/IO43PDB3V0 | GFB1/IO67PDB3V0 | GFB1/IO71PDB4V0 | GFB1/IO106PDB4V0 |
| J5 | NC | GFC0/IO68NDB3V0 | GFC0/IO72NDB4V0 | GFC0/IO107NDB4V0 |
| J6 | NC | GFC1/IO68PDB3V0 | GFC1/IO72PDB4V0 | GFC1/IO107PDB4V0 |
| J7 | GND | GND | GND | GND |
| J8 | VCC | VCC | VCC | VCC |
| J9 | GND | GND | GND | GND |
| J10 | VCC | VCC | VCC | VCC |
| J11 | GDC2/IO41NPB1V0 | IO56NPB1V0 | IO56NPB2V0 | IO83NPB2V0 |
| J12 | NC | GDB0/IO53NPB1V0 | GDB0/IO53NPB2V0 | GDB0/IO80NPB2V0 |
| J13 | NC | GDA1/IO54PDB1V0 | GDA1/IO54PDB2V0 | GDA1/IO81PDB2V0 |
| J14 | GDA0/IO40PDB1V0 | GDC1/IO52PPB1V0 | GDC1/IO52PPB2V0 | GDC1/IO79PPB2V0 |
| J15 | NC | IO50NPB1V0 | IO51NSB2V0 | IO77NSB2V0 |
| J16 | GDA2/IO40NDB1V0 | GDC0/IO52NPB1V0 | GDC0/IO52NPB2V0 | GDC0/IO79NPB2V0 |
| K1 | NC | IO65NPB3V0 | IO67NPB4V0 | IO92NPB4V0 |
| K2 | VCCIB3 | VCCIB3 | VCCIB4 | VCCIB4 |
| K3 | NC | IO65PPB3V0 | IO67PPB4V0 | IO92PPB4V0 |
| K4 | NC | IO64PDB3V0 | IO65PDB4V0 | IO96PDB4V0 |
| K5 | GND | GND | GND | GND |
| K6 | NC | IO64NDB3V0 | IO65NDB4V0 | IO96NDB4V0 |
| K7 | VCC | VCC | VCC | VCC |
| K8 | GND | GND | GND | GND |

| Revision | Changes | Page |
|---|---|---|
| v2.0, Revision 1 (July 2009) | The MicroBlade and Fusion datasheets have been combined. Pigeon Point information is new.<br>CoreMP7 support was removed since it is no longer offered.<br>–F was removed from the datasheet since it is no longer offered.<br>The operating temperature was changed from ambient to junction to better reflect actual conditions of operations.<br>Commercial: 0°C to 85°C<br>Industrial: –40°C to 100°C<br>The version number category was changed from Preliminary to Production, which means the datasheet contains information based on final characterization. The version number changed from Preliminary v1.7 to v2.0. | N/A |
| | The "Integrated Analog Blocks and Analog I/Os" section was updated to include a reference to the "Analog System Characteristics" section in the *Device Architecture* chapter of the datasheet, which includes Table 2-46 • Analog Channel Specifications and specific voltage data. | 1-4 |
| | The phrase "Commercial-Case Conditions" in timing table titles was changed to "Commercial Temperature Range Conditions." | N/A |
| | The "Crystal Oscillator" section was updated significantly. Please review carefully. | 2-20 |
| | The "Real-Time Counter (part of AB macro)" section was updated significantly. Please review carefully. | 2-33 |
| | There was a typo in Table 2-19 • Flash Memory Block Pin Names for the ERASEPAGE description; it was the same as DISCARDPAGE. As a result, the ERASEPAGE description was updated. | 2-40 |
| | The $t_{FMAXCLKNVM}$ parameter was updated in Table 2-25 • Flash Memory Block Timing. | 2-52 |
| | Table 2-31 • RAM4K9 and Table 2-32 • RAM512X18 were updated. | 2-66 |
| | In Table 2-36 • Analog Block Pin Description, the Function description for PWRDWN was changed from "Comparator power-down if 1"<br>to<br>"ADC comparator power-down if 1. When asserted, the ADC will stop functioning, and the digital portion of the analog block will continue operating. This may result in invalid status flags from the analog block. Therefore, Microsemi does not recommend asserting the PWRDWN pin." | 2-78 |
| | Figure 2-75 • Gate Driver Example was updated. | 2-91 |
| | The "ADC Operation" section was updated. Please review carefully. | 2-104 |
| | Figure 2-92 • Intra-Conversion Timing Diagram and Figure 2-93 • Injected Conversion Timing Diagram are new. | 2-113 |
| | The "Typical Performance Characteristics" section is new. | 2-115 |
| | Table 2-49 • Analog Channel Specifications was significantly updated. | 2-117 |
| | Table 2-50 • ADC Characteristics in Direct Input Mode was significantly updated. | 2-120 |
| | In Table 2-52 • Calibrated Analog Channel Accuracy 1,2,3, note 2 was updated. | 2-123 |
| | In Table 2-53 • Analog Channel Accuracy: Monitoring Standard Positive Voltages, note 1 was updated. | 2-124 |
| | In Table 2-54 • ACM Address Decode Table for Analog Quad, bit 89 was removed. | 2-126 |