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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

EXF

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	276480
Number of I/O	223
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs1500-fgg484i

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# **Fusion Device Architecture Overview**



Figure 1 • Fusion Device Architecture Overview (AFS600)

# Package I/Os: Single-/Double-Ended (Analog)

Fusion Devices	AFS090	AFS250	AFS600	AFS1500
ARM Cortex-M1 Devices		M1AFS250	M1AFS600	M1AFS1500
Pigeon Point Devices			P1AFS600 <sup>1</sup>	P1AFS1500 <sup>1</sup>
MicroBlade Devices		U1AFS250 <sup>2</sup>	U1AFS600 <sup>2</sup>	U1AFS1500 <sup>2</sup>
QN108 <sup>3</sup>	37/9 (16)			
QN180 <sup>3</sup>	60/16 (20)	65/15 (24)		
PQ208 <sup>4</sup>		93/26 (24)	95/46 (40)	
FG256	75/22 (20)	114/37 (24)	119/58 (40)	119/58 (40)
FG484			172/86 (40)	223/109 (40)
FG676				252/126 (40)
Notes:	•	1		•

1. Pigeon Point devices are only offered in FG484 and FG256.

2. MicroBlade devices are only offered in FG256.

3. Package not available.

4. Fusion devices in the same package are pin compatible with the exception of the PQ208 package (AFS250 and AFS600).



# Table 2-7 • AFS250 Global Resource Timing<br/>Commercial Temperature Range Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	_	·2	-	-1	St	Unite	
	Description	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Units
t <sub>RCKL</sub>	Input Low Delay for Global Clock	0.89	1.12	1.02	1.27	1.20	1.50	ns
t <sub>RCKH</sub>	Input High Delay for Global Clock	0.88	1.14	1.00	1.30	1.17	1.53	ns
t <sub>RCKMPWH</sub>	Minimum Pulse Width High for Global Clock							ns
t <sub>RCKMPWL</sub>	Minimum Pulse Width Low for Global Clock							ns
t <sub>RCKSW</sub>	Maximum Skew for Global Clock		0.26		0.30		0.35	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

## Table 2-8 • AFS090 Global Resource Timing

Commercial Temperature Range Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-	2	-	1	S	td.	Unite
	Description	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Units
t <sub>RCKL</sub>	Input Low Delay for Global Clock	0.84	1.07	0.96	1.21	1.13	1.43	ns
t <sub>RCKH</sub>	Input High Delay for Global Clock	0.83	1.10	0.95	1.25	1.12	1.47	ns
t <sub>RCKMPWH</sub>	Minimum Pulse Width High for Global Clock							ns
t <sub>RCKMPWL</sub>	Minimum Pulse Width Low for Global Clock							ns
t <sub>RCKSW</sub>	Maximum Skew for Global Clock		0.27		0.30		0.36	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

### Read Next Operation

The Read Next operation is a feature by which the next block relative to the block in the Block Buffer is read from the FB Array while performing reads from the Block Buffer. The goal is to minimize wait states during consecutive sequential Read operations.

The Read Next operation is performed in a predetermined manner because it does look-ahead reads. The general look-ahead function is as follows:

- Within a page, the next block fetched will be the next in linear address.
- When reading the last data block of a page, it will fetch the first block of the next page.
- When reading spare pages, it will read the first block of the next sector's spare page.
- Reads of the last sector will wrap around to sector 0.
- · Reads of Auxiliary blocks will read the next linear page's Auxiliary block.

When an address on the ADDR input does not agree with the predetermined look-ahead address, there is a time penalty for this access. The FB will be busy finishing the current look-ahead read before it can start the next read. The worst case is a total of nine BUSY cycles before data is delivered.

The Non-Pipe Mode and Pipe Mode waveforms for Read Next operations are illustrated in Figure 2-40 and Figure 2-41.



Figure 2-40 • Read Next Waveform (Non-Pipe Mode, 32-bit access)



*Figure 2-41* • Read Next WaveForm (Pipe Mode, 32-bit access)



RAM512X18 exhibits slightly different behavior from RAM4K9, as it has dedicated read and write ports.

#### WW and RW

These signals enable the RAM to be configured in one of the two allowable aspect ratios (Table 2-30).

#### Table 2-30 • Aspect Ratio Settings for WW[1:0]

WW[1:0]	RW[1:0]	D×W
01	01	512×9
10	10	256×18
00, 11	00, 11	Reserved

#### WD and RD

These are the input and output data signals, and they are 18 bits wide. When a 512×9 aspect ratio is used for write, WD[17:9] are unused and must be grounded. If this aspect ratio is used for read, then RD[17:9] are undefined.

#### WADDR and RADDR

These are read and write addresses, and they are nine bits wide. When the 256×18 aspect ratio is used for write or read, WADDR[8] or RADDR[8] are unused and must be grounded.

#### WCLK and RCLK

These signals are the write and read clocks, respectively. They are both active high.

#### WEN and REN

These signals are the write and read enables, respectively. They are both active low by default. These signals can be configured as active high.

#### RESET

This active low signal resets the output to zero, disables reads and/or writes from the SRAM block, and clears the data hold registers when asserted. It does not reset the contents of the memory.

#### PIPE

This signal is used to specify pipelined read on the output. A Low on PIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A High indicates a pipelined read, and data appears on the output in the next clock cycle.

#### Clocking

The dual-port SRAM blocks are only clocked on the rising edge. SmartGen allows falling-edge-triggered clocks by adding inverters to the netlist, hence achieving dual-port SRAM blocks that are clocked on either edge (rising or falling). For dual-port SRAM, each port can be clocked on either edge or by separate clocks, by port.

Fusion devices support inversion (bubble pushing) throughout the FPGA architecture, including the clock input to the SRAM modules. Inversions added to the SRAM clock pin on the design schematic or in the HDL code will be automatically accounted for during design compile without incurring additional delay in the clock path.

The two-port SRAM can be clocked on the rising edge or falling edge of WCLK and RCLK.

If negative-edge RAM and FIFO clocking is selected for memory macros, clock edge inversion management (bubble pushing) is automatically used within the Fusion development tools, without performance penalty.



The AEMPTY flag is asserted when the difference between the write address and the read address is less than a predefined value. In the example above, a value of 200 for AEVAL means that the AEMPTY flag will be asserted when a read causes the difference between the write address and the read address to drop to 200. It will stay asserted until that difference rises above 200. Note that the FIFO can be configured with different read and write widths; in this case, the AFVAL setting is based on the number of write data entries and the AEVAL setting is based on the number of software and 256×18, only 4,096 bits can be addressed by the 12 bits of AFVAL and AEVAL. The number of words must be multiplied by 8 and 16, instead of 9 and 18. The SmartGen tool automatically uses the proper values. To avoid halfwords being written or read, which could happen if different read and write aspect ratios are specified, the FIFO will assert FULL or EMPTY as soon as at least a minimum of one word cannot be written or read. For example, if a two-bit word is written and a four-bit word is being read, the FIFO will remain in the empty state when the first word is written. This occurs even if the FIFO is not completely empty, because in this case, a complete word cannot be read. The same is applicable in the full state. If a four-bit word is written and a two-bit word is read, the FIFO is full and one word is read. The FULL flag will remain asserted because a complete word cannot be written at this point.



# Terminology

#### Resolution

Resolution defines the smallest temperature change Fusion Temperature Monitor can resolve. For ADC configured as 8-bit mode, each LSB represents 4°C, and 1°C per LSB for 10-bit mode. With 12-bit mode, the Temperature Monitor can still only resolve 1°C due to Temperature Monitor design.

#### Offset

The Fusion Temperature Monitor has a systematic offset (Table 2-49 on page 2-117), excluding error due to board resistance and ideality factor of the external diode. Microsemi provides an IP block (CalibIP) that is required in order to mitigate the systematic temperature offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the Fusion FPGA Fabric User Guide.

There are several popular ADC architectures, each with advantages and limitations.

The analog-to-digital converter in Fusion devices is a switched-capacitor Successive Approximation Register (SAR) ADC. It supports 8-, 10-, and 12-bit modes of operation with a cumulative sample rate up to 600 k samples per second (ksps). Built-in bandgap circuitry offers 1% internal voltage reference accuracy or an external reference voltage can be used.

As shown in Figure 2-81, a SAR ADC contains N capacitors with binary-weighted values.



Figure 2-81 • Example SAR ADC Architecture

To begin a conversion, all of the capacitors are quickly discharged. Then VIN is applied to all the capacitors for a period of time (acquisition time) during which the capacitors are charged to a value very close to VIN. Then all of the capacitors are switched to ground, and thus –VIN is applied across the comparator. Now the conversion process begins. First, C is switched to VREF Because of the binary weighting of the capacitors, the voltage at the input of the comparator is then shown by EQ 11.

Voltage at input of comparator = -VIN + VREF / 2

EQ 11

If VIN is greater than VREF / 2, the output of the comparator is 1; otherwise, the comparator output is 0. A register is clocked to retain this value as the MSB of the result. Next, if the MSB is 0, C is switched back to ground; otherwise, it remains connected to VREF, and C / 2 is connected to VREF. The result at the comparator input is now either –VIN + VREF / 4 or –VIN + 3 VREF / 4 (depending on the state of the MSB), and the comparator output now indicates the value of the next most significant bit. This bit is likewise registered, and the process continues for each subsequent bit until a conversion is complete. The conversion process requires some acquisition time plus N + 1 ADC clock cycles to complete.



Intra-Conversion



*Note:* \**t*<sub>CONV</sub> represents the conversion time of the second conversion. See EQ 23 on page 2-109 for calculation of the conversion time, *t*<sub>CONV</sub>.

Figure 2-92 • Intra-Conversion Timing Diagram



Injected Conversion

Note: \*See EQ 23 on page 2-109 for calculation on the conversion time, t<sub>CONV</sub>.

Figure 2-93 • Injected Conversion Timing Diagram



#### Table 2-98 • I/O Short Currents IOSH/IOSL (continued)

	Drive Strength	IOSH (mA)*	IOSL (mA)*		
2.5 V LVCMOS	2 mA	16	18		
	4 mA	16	18		
	6 mA	32	37		
	8 mA	32	37		
	12 mA	65	74		
	16 mA	83	87		
	24 mA	169	124		
1.8 V LVCMOS	2 mA	9	11		
	4 mA	17	22		
	6 mA	35	44		
	8 mA	45	51		
	12 mA	91	74		
	16 mA	91	74		
1.5 V LVCMOS	2 mA	13	16		
	4 mA	25	33		
	6 mA	32	39		
	8 mA	66	55		
	12 mA	66	55		
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109		
Applicable to Standard I/O Banks					
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27		
	4 mA	25	27		
	6 mA	51	54		
	8 mA	51	54		
2.5 V LVCMOS	2 mA	16	18		
	4 mA	16	18		
	6 mA	32	37		
	8 mA	32	37		
1.8 V LVCMOS	2 mA	9	11		
	4 mA	17	22		
1.5 V LVCMOS	2 mA	13	16		

*Note:*  $^{*}T_{J} = 100^{\circ}C$ 

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 36 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.



#### Table 2-105 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew

Commercial Temperature Range Conditions:  $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Pro I/Os

Drive	Speed						<sup>τ</sup> ΕΟU							11
Strength	Grade	TDOUT	τ <sub>DP</sub>	τ <sub>DIN</sub>	τ <sub>ΡΥ</sub>	τ <sub>PYS</sub>	Т	۲ZL	τzΗ	ιLZ	τ <sub>HZ</sub>	τ <sub>ZLS</sub>	τ <sub>zhs</sub>	Units
4 mA	Std.	0.66	7.88	0.04	1.20	1.57	0.43	8.03	6.70	2.69	2.59	10.26	8.94	ns
	-1	0.56	6.71	0.04	1.02	1.33	0.36	6.83	5.70	2.29	2.20	8.73	7.60	ns
	-2	0.49	5.89	0.03	0.90	1.17	0.32	6.00	5.01	2.01	1.93	7.67	6.67	ns
8 mA	Std.	0.66	5.08	0.04	1.20	1.57	0.43	5.17	4.14	3.05	3.21	7.41	6.38	ns
	-1	0.56	4.32	0.04	1.02	1.33	0.36	4.40	3.52	2.59	2.73	6.30	5.43	ns
	-2	0.49	3.79	0.03	0.90	1.17	0.32	3.86	3.09	2.28	2.40	5.53	4.76	ns
12 mA	Std.	0.66	3.67	0.04	1.20	1.57	0.43	3.74	2.87	3.28	3.61	5.97	5.11	ns
	-1	0.56	3.12	0.04	1.02	1.33	0.36	3.18	2.44	2.79	3.07	5.08	4.34	ns
	-2	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81	ns
16 mA	Std.	0.66	3.46	0.04	1.20	1.57	0.43	3.53	2.61	3.33	3.72	5.76	4.84	ns
	-1	0.56	2.95	0.04	1.02	1.33	0.36	3.00	2.22	2.83	3.17	4.90	4.12	ns
	-2	0.49	2.59	0.03	0.90	1.17	0.32	2.63	1.95	2.49	2.78	4.30	3.62	ns
24 mA	Std.	0.66	3.21	0.04	1.20	1.57	0.43	3.27	2.16	3.39	4.13	5.50	4.39	ns
	-1	0.56	2.73	0.04	1.02	1.33	0.36	2.78	1.83	2.88	3.51	4.68	3.74	ns
	-2	0.49	2.39	0.03	0.90	1.17	0.32	2.44	1.61	2.53	3.08	4.11	3.28	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



#### Table 2-115 • 2.5 V LVCMOS High Slew

Commercial Temperature Range Conditions:  $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V Applicable to Advanced I/Os

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>zH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>zLS</sub>	t <sub>zHS</sub>	Units
4 mA	Std.	0.66	8.66	0.04	1.31	0.43	7.83	8.66	2.68	2.30	10.07	10.90	ns
	-1	0.56	7.37	0.04	1.11	0.36	6.66	7.37	2.28	1.96	8.56	9.27	ns
	-2	0.49	6.47	0.03	0.98	0.32	5.85	6.47	2.00	1.72	7.52	8.14	ns
8 mA	Std.	0.66	5.17	0.04	1.31	0.43	5.04	5.17	3.05	3.00	7.27	7.40	ns
	-1	0.56	4.39	0.04	1.11	0.36	4.28	4.39	2.59	2.55	6.19	6.30	ns
	-2	0.49	3.86	0.03	0.98	0.32	3.76	3.86	2.28	2.24	5.43	5.53	ns
12 mA	Std.	0.66	3.56	0.04	1.31	0.43	3.63	3.43	3.30	3.44	5.86	5.67	ns
	-1	0.56	3.03	0.04	1.11	0.36	3.08	2.92	2.81	2.92	4.99	4.82	ns
	-2	0.49	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns
16 mA	Std.	0.66	3.35	0.04	1.31	0.43	3.41	3.06	3.36	3.55	5.65	5.30	ns
	-1	0.56	2.85	0.04	1.11	0.36	2.90	2.60	2.86	3.02	4.81	4.51	ns
	-2	0.49	2.50	0.03	0.98	0.32	2.55	2.29	2.51	2.65	4.22	3.96	ns
24 mA	Std.	0.66	3.56	0.04	1.31	0.43	3.63	3.43	3.30	3.44	5.86	5.67	ns
	-1	0.56	3.03	0.04	1.11	0.36	3.08	2.92	2.81	2.92	4.99	4.82	ns
	-2	0.49	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

#### Table 2-116 • 2.5 V LVCMOS Low Slew

Commercial Temperature Range Conditions:  $T_J$  = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V Applicable to Standard I/Os

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>zH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	Units
2 mA	Std.	0.66	11.00	0.04	1.29	0.43	10.37	11.00	2.03	1.83	ns
	-1	0.56	9.35	0.04	1.10	0.36	8.83	9.35	1.73	1.56	ns
	-2	0.49	8.21	0.03	0.96	0.32	7.75	8.21	1.52	1.37	ns
4 mA	Std.	0.66	11.00	0.04	1.29	0.43	10.37	11.00	2.03	1.83	ns
	-1	0.56	9.35	0.04	1.10	0.36	8.83	9.35	1.73	1.56	ns
	-2	0.49	8.21	0.03	0.96	0.32	7.75	8.21	1.52	1.37	ns
6 mA	Std.	0.66	7.50	0.04	1.29	0.43	7.36	7.50	2.39	2.46	ns
	-1	0.56	6.38	0.04	1.10	0.36	6.26	6.38	2.03	2.10	ns
	-2	0.49	5.60	0.03	0.96	0.32	5.49	5.60	1.78	1.84	ns
8 mA	Std.	0.66	7.50	0.04	1.29	0.43	7.36	7.50	2.39	2.46	ns
	-1	0.56	6.38	0.04	1.10	0.36	6.26	6.38	2.03	2.10	ns
	-2	0.49	5.60	0.03	0.96	0.32	5.49	5.60	1.78	1.84	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



#### 1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for generalpurpose 1.8 V applications. It uses a 1.8 V input buffer and push-pull output buffer.

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
Applicable to Pro I/O Banks												
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	2	2	11	9	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	4	4	22	17	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	6	6	44	35	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	8	8	51	45	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	12	12	74	91	10	10
16 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	16	16	74	91	10	10
Applicable	to Advar	nced I/O Banl	(S									
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	2	2	11	9	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	4	4	22	17	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	6	6	44	35	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	8	8	51	45	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	12	12	74	91	10	10
16 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	16	16	74	91	10	10
Applicable	to Stand	ard I/O Banks	5			•						
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	2	2	11	9	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI-0.45	4	4	22	17	10	10

#### Table 2-118 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.



### Figure 2-121 • AC Loading

#### Table 2-119 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input Low (V)	Measuring Point* (V)	VREF (typ.) (V)	C <sub>LOAD</sub> (pF)		
0	1.8	0.9	_	35		

Note: \*Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.



#### 1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for generalpurpose 1.5 V applications. It uses a 1.5 V input buffer and push-pull output buffer.

1.5 V LVCMOS		VIL	VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
Applicable	to Pro I	/O Banks								1		
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	6	6	39	32	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	8	8	55	66	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12	55	66	10	10
Applicable	to Adva	inced I/O Ban	iks						-	-		
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	6	6	39	32	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	8	8	55	66	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12	55	66	10	10
Applicable	to Pro I	/O Banks							-	-		
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. I<sub>IH</sub> is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.



Figure 2-122 • AC Loading

#### Table 2-127 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C <sub>LOAD</sub> (pF)
0	1.5	0.75	-	35

Note: \*Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.



#### SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-156 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class I	I VIL		VIH VOL		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL¹	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
15 mA	-0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15	87	83	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.



#### Figure 2-130 • AC Loading

Table 2-157	•	AC Waveforms.	Measuring Po	ints, and Car	pacitive Loads
		Ao marononino,	mououring i o	millo, and ou	

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C <sub>LOAD</sub> (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

Note: \*Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

#### Timing Characteristics

Table 2-158 • SSTL 2 Class I

```
Commercial Temperature Range Conditions: T_J = 70^{\circ}C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V
```

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>zH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>zLS</sub>	t <sub>zHS</sub>	Units
Std.	0.66	2.13	0.04	1.33	0.43	2.17	1.85			4.40	4.08	ns
-1	0.56	1.81	0.04	1.14	0.36	1.84	1.57			3.74	3.47	ns
-2	0.49	1.59	0.03	1.00	0.32	1.62	1.38			3.29	3.05	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



# 3 – DC and Power Characteristics

# **General Specifications**

# **Operating Conditions**

Stresses beyond those listed in Table 3-1 may cause permanent damage to the device.

Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating ranges specified in Table 3-2 on page 3-3.

Symbol	Parameter	Commercial	Industrial	Units
VCC	DC core supply voltage	-0.3 to 1.65	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	-0.3 to 3.75	-0.3 to 3.75	V
VPUMP	Programming voltage	-0.3 to 3.75	-0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	-0.3 to 1.65	-0.3 to 1.65	V
VCCI	DC I/O output buffer supply voltage	-0.3 to 3.75	-0.3 to 3.75	V
VI	I/O input voltage <sup>1</sup>	-0.3 V to 3.6 V (when enabled) -0.3 V to (VCCI + 1 voltage is lower (when disabled)	<ul><li>I/O hot insertion mode is</li><li>V) or 3.6 V, whichever</li><li>I/O hot-insertion mode is</li></ul>	V
VCC33A	+3.3 V power supply	–0.3 to 3.75 <sup>2</sup>	–0.3 to 3.75 <sup>2</sup>	V
VCC33PMP	+3.3 V power supply	-0.3 to 3.75 <sup>2</sup>	-0.3 to 3.75 <sup>2</sup>	V
VAREF	Voltage reference for ADC	-0.3 to 3.75	-0.3 to 3.75	V
VCC15A	Digital power supply for the analog system	-0.3 to 1.65	–0.3 to 1.65	V
VCCNVM	Embedded flash power supply	-0.3 to 1.65	-0.3 to 1.65	V
VCCOSC	Oscillator power supply	-0.3 to 3.75	-0.3 to 3.75	V

#### Table 3-1 • Absolute Maximum Ratings

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-4 on page 3-4.

2. Analog data not valid beyond 3.65 V.

3. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.

4. For flash programming and retention maximum limits, refer to Table 3-5 on page 3-5. For recommended operating limits refer to Table 3-2 on page 3-3.



#### Table 3-12 • Summary of I/O Input Buffer Power (per pin)—Default I/O Software Settings (continued)

	VCCI (V)	Static Power PDC7 (mW) <sup>1</sup>	Dynamic Power PAC9 (µW/MHz) <sup>2</sup>
Applicable to Advanced I/O Banks			
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	_	16.69
2.5 V LVCMOS	2.5	_	5.12
1.8 V LVCMOS	1.8	_	2.13
1.5 V LVCMOS (JESD8-11)	1.5	_	1.45
3.3 V PCI	3.3	_	18.11
3.3 V PCI-X	3.3	_	18.11
Differential			
LVDS	2.5	2.26	1.20
LVPECL	3.3	5.72	1.87
Applicable to Standard I/O Banks			
3.3 V LVTTL/LVCMOS	3.3	-	16.79
2.5 V LVCMOS	2.5	_	5.19
1.8 V LVCMOS	1.8	_	2.18
1.5 V LVCMOS (JESD8-11)	1.5	_	1.52

Notes:

1. PDC7 is the static power (where applicable) measured on VCCI.

2. PAC9 is the total dynamic power measured on VCC and VCCI.

### PLL/CCC Contribution—P<sub>PLL</sub>

PLL is not used in this application.

 $P_{PLL} = 0 W$ 

## Nonvolatile Memory—P<sub>NVM</sub>

Nonvolatile memory is not used in this application.

 $P_{NVM} = 0 W$ 

# Crystal Oscillator—P<sub>XTL-OSC</sub>

The application utilizes standby mode. The crystal oscillator is assumed to be active.

#### **Operating Mode**

P<sub>XTL-OSC</sub> = PAC18

 $P_{XTL-OSC} = 0.63 \text{ mW}$ 

#### Standby Mode

P<sub>XTL-OSC</sub> = PAC18

P<sub>XTL-OSC</sub> = 0.63 mW

#### Sleep Mode

 $P_{XTL-OSC} = 0 W$ 

## RC Oscillator—P<sub>RC-OSC</sub>

#### **Operating Mode**

P<sub>RC-OSC</sub> = PAC19

 $P_{RC-OSC} = 3.30 \text{ mW}$ 

#### Standby Mode and Sleep Mode

 $P_{RC-OSC} = 0 W$ 

#### Analog System—P<sub>AB</sub>

Number of Quads used: N<sub>QUADS</sub> = 4

#### **Operating Mode**

P<sub>AB</sub> = PAC20

 $P_{AB}$  = 3.00 mW

#### Standby Mode and Sleep Mode

 $P_{AB} = 0 W$ 

#### Total Dynamic Power Consumption—P<sub>DYN</sub>

#### **Operating Mode**

P<sub>DYN</sub> = P<sub>CLOCK</sub> + P<sub>S-CELL</sub> + P<sub>C-CELL</sub> + P<sub>NET</sub> + P<sub>INPUTS</sub> + P<sub>OUTPUTS</sub> + P<sub>MEMORY</sub> + P<sub>PLL</sub> + P<sub>NVM</sub>+ P<sub>XTL-OSC</sub> + P<sub>RC-OSC</sub> + P<sub>AB</sub> P<sub>DYN</sub> = 41.28 mW + 21.1 mW + 4.35 mW + 19.25 mW + 1.30 mW + 47.47 mW + 1.38 mW + 0 + 0 + 0 + 0.63 mW + 3.30 mW + 3.00 mW

P<sub>DYN</sub> = 143.06 mW

#### Standby Mode

 $P_{DYN} = P_{XTL-OSC}$  $P_{DYN} = 0.63 \text{ mW}$ 

#### Sleep Mode

 $P_{DYN} = 0 W$ 



# **QN180**



Note: The die attach paddle center of the package is tied to ground (GND).

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/default.aspx.



Package Pin Assignments

	FG484		FG484					
Pin Number	AFS600 Function	AFS1500 Function	Pin Number	AFS600 Function	AFS1500 Function			
E9	NC	IO08PDB0V1	F22	IO35PDB2V0	IO51PDB2V0			
E10	GND	GND	G1	IO77PDB4V0	IO115PDB4V0			
E11	IO15NDB1V0	IO22NDB1V0	G2	GND	GND			
E12	IO15PDB1V0	IO22PDB1V0	G3	IO78NDB4V0	IO116NDB4V0			
E13	GND	GND	G4	IO78PDB4V0	IO116PDB4V0			
E14	NC	IO32PPB1V1	G5	VCCIB4	VCCIB4			
E15	NC	IO36NPB1V2	G6	NC	IO117PDB4V0			
E16	VCCIB1	VCCIB1	G7	VCCIB4	VCCIB4			
E17	GND	GND	G8	GND	GND			
E18	NC	IO47NPB2V0	G9	IO04NDB0V0	IO06NDB0V1			
E19	IO33PDB2V0	IO49PDB2V0	G10	IO04PDB0V0	IO06PDB0V1			
E20	VCCIB2	VCCIB2	G11	IO12NDB0V1	IO16NDB0V2			
E21	IO32NDB2V0	IO46NDB2V0	G12	IO12PDB0V1	IO16PDB0V2			
E22	GBC2/IO32PDB2V0	GBC2/IO46PDB2V0	G13	NC	IO28NDB1V1			
F1	IO80NDB4V0	IO118NDB4V0	G14	NC	IO28PDB1V1			
F2	IO80PDB4V0	IO118PDB4V0	G15	GND	GND			
F3	NC	IO119NSB4V0	G16	NC	IO38PPB1V2			
F4	IO84NDB4V0	IO124NDB4V0	G17	NC	IO53PDB2V0			
F5	GND	GND	G18	VCCIB2	VCCIB2			
F6	VCOMPLA	VCOMPLA	G19	IO36PDB2V0	IO52PDB2V0			
F7	VCCPLA	VCCPLA	G20	IO36NDB2V0	IO52NDB2V0			
F8	VCCIB0	VCCIB0	G21	GND	GND			
F9	IO08NDB0V1	IO12NDB0V1	G22	IO35NDB2V0	IO51NDB2V0			
F10	IO08PDB0V1	IO12PDB0V1	H1	IO77NDB4V0	IO115NDB4V0			
F11	VCCIB0	VCCIB0	H2	IO76PDB4V0	IO113PDB4V0			
F12	VCCIB1	VCCIB1	H3	VCCIB4	VCCIB4			
F13	IO22NDB1V0	IO30NDB1V1	H4	IO79NDB4V0	IO114NDB4V0			
F14	IO22PDB1V0	IO30PDB1V1	H5	IO79PDB4V0	IO114PDB4V0			
F15	VCCIB1	VCCIB1	H6	NC	IO117NDB4V0			
F16	NC	IO36PPB1V2	H7	GND	GND			
F17	NC	IO38NPB1V2	H8	VCC	VCC			
F18	GND	GND	H9	VCCIB0	VCCIB0			
F19	IO33NDB2V0	IO49NDB2V0	H10	GND	GND			
F20	IO34PDB2V0	IO50PDB2V0	H11	VCCIB0	VCCIB0			
F21	IO34NDB2V0	IO50NDB2V0	H12	VCCIB1	VCCIB1			

	FG484		FG484					
Pin Number	AFS600 Function	AFS1500 Function	Pin Number	AFS600 Function	AFS1500 Function			
H13	GND	GND	K4	IO75NDB4V0	IO110NDB4V0			
H14	VCCIB1	VCCIB1	K5	GND	GND			
H15	GND	GND	K6	NC	IO104NDB4V0			
H16	GND	GND	K7	NC	IO111NDB4V0			
H17	NC	IO53NDB2V0	K8	GND	GND			
H18	IO38PDB2V0	IO57PDB2V0	K9	VCC	VCC			
H19	GCA2/IO39PDB2V0	GCA2/IO59PDB2V0	K10	GND	GND			
H20	VCCIB2	VCCIB2	K11	VCC	VCC			
H21	IO37NDB2V0	IO54NDB2V0	K12	GND	GND			
H22	IO37PDB2V0	IO54PDB2V0	K13	VCC	VCC			
J1	NC	IO112PPB4V0	K14	GND	GND			
J2	IO76NDB4V0	IO113NDB4V0	K15	GND	GND			
J3	GFB2/IO74PDB4V0	GFB2/IO109PDB4V0	K16	IO40NDB2V0	IO60NDB2V0			
J4	GFA2/IO75PDB4V0	GFA2/IO110PDB4V0	K17	NC	IO58PDB2V0			
J5	NC	IO112NPB4V0	K18	GND	GND			
J6	NC	IO104PDB4V0	K19	NC	IO68NPB2V0			
J7	NC	IO111PDB4V0	K20	IO41NDB2V0	IO61NDB2V0			
J8	VCCIB4	VCCIB4	K21	GND	GND			
J9	GND	GND	K22	IO42NDB2V0	IO56NDB2V0			
J10	VCC	VCC	L1	IO73NDB4V0	IO108NDB4V0			
J11	GND	GND	L2	VCCOSC	VCCOSC			
J12	VCC	VCC	L3	VCCIB4	VCCIB4			
J13	GND	GND	L4	XTAL2	XTAL2			
J14	VCC	VCC	L5	GFC1/IO72PDB4V0	GFC1/IO107PDB4V0			
J15	VCCIB2	VCCIB2	L6	VCCIB4	VCCIB4			
J16	GCB2/IO40PDB2V0	GCB2/IO60PDB2V0	L7	GFB1/IO71PDB4V0	GFB1/IO106PDB4V0			
J17	NC	IO58NDB2V0	L8	VCCIB4	VCCIB4			
J18	IO38NDB2V0	IO57NDB2V0	L9	GND	GND			
J19	IO39NDB2V0	IO59NDB2V0	L10	VCC	VCC			
J20	GCC2/IO41PDB2V0	GCC2/IO61PDB2V0	L11	GND	GND			
J21	NC	IO55PSB2V0	L12	VCC	VCC			
J22	IO42PDB2V0	IO56PDB2V0	L13	GND	GND			
K1	GFC2/IO73PDB4V0	GFC2/IO108PDB4V0	L14	VCC	VCC			
K2	GND	GND	L15	VCCIB2	VCCIB2			
K3	IO74NDB4V0	IO109NDB4V0	L16	IO48PDB2V0	IO70PDB2V0			