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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	114
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs250-1fg256

VersaNet Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are dependent upon I/O standard, and the clock may be driven and conditioned internally by the CCC module. Table 2-5, Table 2-6, Table 2-7, and Table 2-8 on page 2-17 present minimum and maximum global clock delays within the device Minimum and maximum delays are measured with minimum and maximum loading, respectively.

Timing Characteristics

Table 2-5 • AFS1500 Global Resource Timing
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.53	1.75	1.74	1.99	2.05	2.34	ns
t_{RCKH}	Input High Delay for Global Clock	1.53	1.79	1.75	2.04	2.05	2.40	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock							ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock							ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

Table 2-6 • AFS600 Global Resource Timing
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.27	1.49	1.44	1.70	1.69	2.00	ns
t_{RCKH}	Input High Delay for Global Clock	1.26	1.54	1.44	1.75	1.69	2.06	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock							ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock							ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27		0.31		0.36	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

Flash Memory Block Characteristics

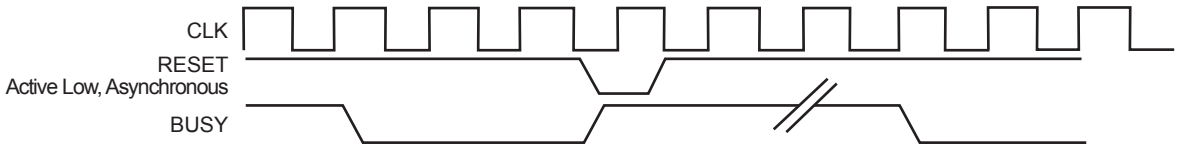

Figure 2-44 • **Reset Timing Diagram**

Table 2-25 • **Flash Memory Block Timing**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{CLK2RD}	Clock-to-Q in 5-cycle read mode of the Read Data	7.99	9.10	10.70	ns
	Clock-to-Q in 6-cycle read mode of the Read Data	5.03	5.73	6.74	ns
$t_{CLK2BUSY}$	Clock-to-Q in 5-cycle read mode of BUSY	4.95	5.63	6.62	ns
	Clock-to-Q in 6-cycle read mode of BUSY	4.45	5.07	5.96	ns
$t_{CLK2STATUS}$	Clock-to-Status in 5-cycle read mode	11.24	12.81	15.06	ns
	Clock-to-Status in 6-cycle read mode	4.48	5.10	6.00	ns
t_{DSUNVM}	Data Input Setup time for the Control Logic	1.92	2.19	2.57	ns
t_{DHNVM}	Data Input Hold time for the Control Logic	0.00	0.00	0.00	ns
t_{ASUNVM}	Address Input Setup time for the Control Logic	2.76	3.14	3.69	ns
t_{AHNVM}	Address Input Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUDWNVM}$	Data Width Setup time for the Control Logic	1.85	2.11	2.48	ns
$t_{HDDWNVM}$	Data Width Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SURENNVM}$	Read Enable Setup time for the Control Logic	3.85	4.39	5.16	ns
$t_{HDRENNVM}$	Read Enable Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUWENNVM}$	Write Enable Setup time for the Control Logic	2.37	2.69	3.17	ns
$t_{HDWENNVM}$	Write Enable Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUPROGNVM}$	Program Setup time for the Control Logic	2.16	2.46	2.89	ns
$t_{HDPROGNVM}$	Program Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUSPAREPAGE}$	SparePage Setup time for the Control Logic	3.74	4.26	5.01	ns
$t_{HDSPAREPAGE}$	SparePage Hold time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUAUXBLK}$	Auxiliary Block Setup Time for the Control Logic	3.74	4.26	5.00	ns
$t_{HDAUXBLK}$	Auxiliary Block Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SURDNEXT}$	ReadNext Setup Time for the Control Logic	2.17	2.47	2.90	ns
$t_{HDRDNEXT}$	ReadNext Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUERASEPG}$	Erase Page Setup Time for the Control Logic	3.76	4.28	5.03	ns
$t_{HDERASEPG}$	Erase Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUUNPROTECTPG}$	Unprotect Page Setup Time for the Control Logic	2.01	2.29	2.69	ns
$t_{HDUNPROTECTPG}$	Unprotect Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUDISCARDPG}$	Discard Page Setup Time for the Control Logic	1.88	2.14	2.52	ns
$t_{HDDISCARDPG}$	Discard Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
$t_{SUOVERWRPRO}$	Overwrite Protect Setup Time for the Control Logic	1.64	1.86	2.19	ns
$t_{HDOVERWRPRO}$	Overwrite Protect Hold Time for the Control Logic	0.00	0.00	0.00	ns

The AEMPTY flag is asserted when the difference between the write address and the read address is less than a predefined value. In the example above, a value of 200 for AEVAL means that the AEMPTY flag will be asserted when a read causes the difference between the write address and the read address to drop to 200. It will stay asserted until that difference rises above 200. Note that the FIFO can be configured with different read and write widths; in this case, the AFVAL setting is based on the number of write data entries and the AEVAL setting is based on the number of read data entries. For aspect ratios of 512×9 and 256×18, only 4,096 bits can be addressed by the 12 bits of AFVAL and AEVAL. The number of words must be multiplied by 8 and 16, instead of 9 and 18. The SmartGen tool automatically uses the proper values. To avoid halfwords being written or read, which could happen if different read and write aspect ratios are specified, the FIFO will assert FULL or EMPTY as soon as at least a minimum of one word cannot be written or read. For example, if a two-bit word is written and a four-bit word is being read, the FIFO will remain in the empty state when the first word is written. This occurs even if the FIFO is not completely empty, because in this case, a complete word cannot be read. The same is applicable in the full state. If a four-bit word is written and a two-bit word is read, the FIFO is full and one word is read. The FULL flag will remain asserted because a complete word cannot be written at this point.

Voltage Monitor

The Fusion Analog Quad offers a robust set of voltage-monitoring capabilities unique in the FPGA industry. The Analog Quad comprises three analog input pads— Analog Voltage (AV), Analog Current (AC), and Analog Temperature (AT)—and a single gate driver output pad, Analog Gate (AG). There are many common characteristics among the analog input pads. Each analog input can be configured to connect directly to the input MUX of the ADC. When configured in this manner (Figure 2-66), there will be no prescaling of the input signal. Care must be taken in this mode not to drive the ADC into saturation by applying an input voltage greater than the reference voltage. The internal reference voltage of the ADC is 2.56 V. Optionally, an external reference can be supplied by the user. The external reference can be a maximum of 3.3 V DC.

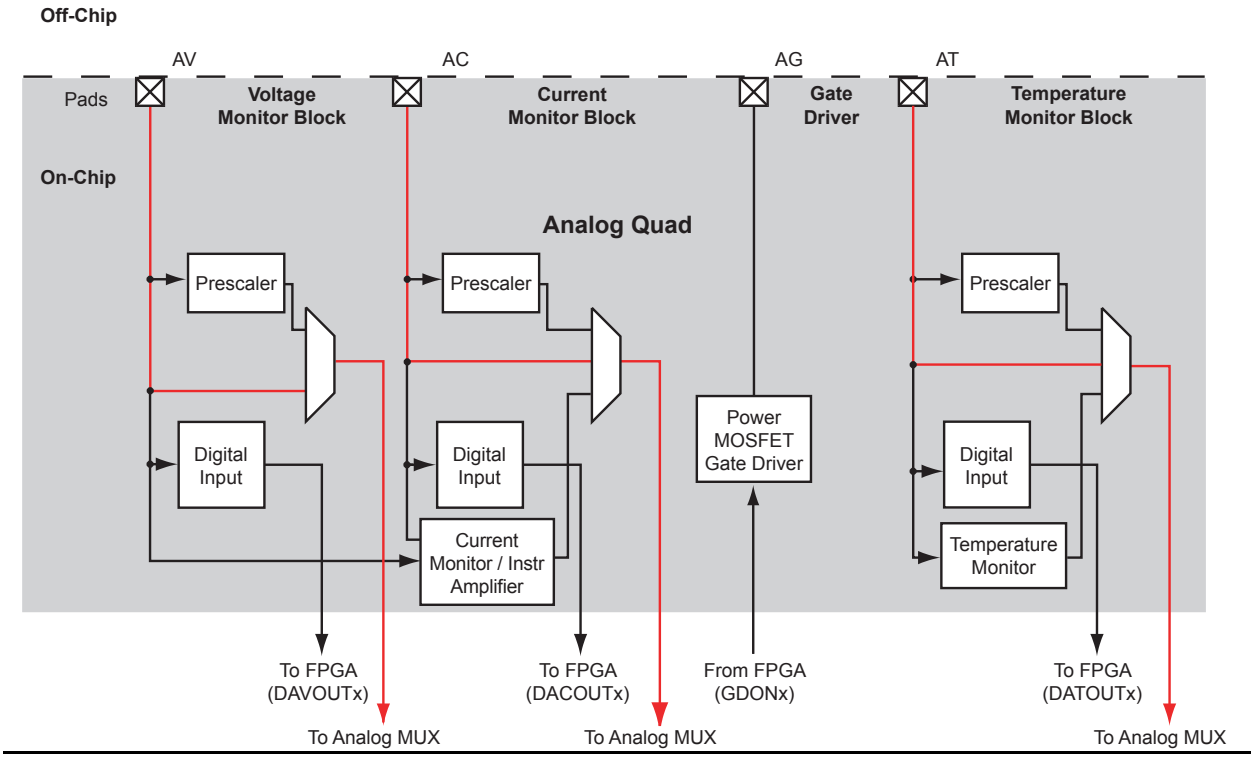

Figure 2-66 • **Analog Quad Direct Connect**

The Analog Quad offers a wide variety of prescaling options to enable the ADC to resolve the input signals. Figure 2-67 shows the path through the Analog Quad for a signal that is to be prescaled prior to conversion. The ADC internal reference voltage and the prescaler factors were selected to make both prescaling and postscaling of the signals easy binary calculations (refer to Table 2-57 on page 2-130 for details). When an analog input pad is configured with a prescaler, there will be a 1 MΩ resistor to ground. This occurs even when the device is in power-down mode. In low power standby or sleep mode (VCC is OFF, VCC33A is ON, VCCI is ON) or when the resource is not used, analog inputs are pulled down to ground through a 1 MΩ resistor. The gate driver output is floating (or tristated), and there is no extra current on VCC33A.

These scaling factors hold true whether the particular pad is configured to accept a positive or negative voltage. Note that whereas the AV and AC pads support the same prescaling factors, the AT pad supports a reduced set of prescaling factors and supports positive voltages only.

Fusion uses a remote diode as a temperature sensor. The Fusion Temperature Monitor uses a differential input; the AT pin and ATRTN (AT Return) pin are the differential inputs to the Temperature Monitor. There is one Temperature Monitor in each Quad. A simplified block diagram is shown in Figure 2-77.

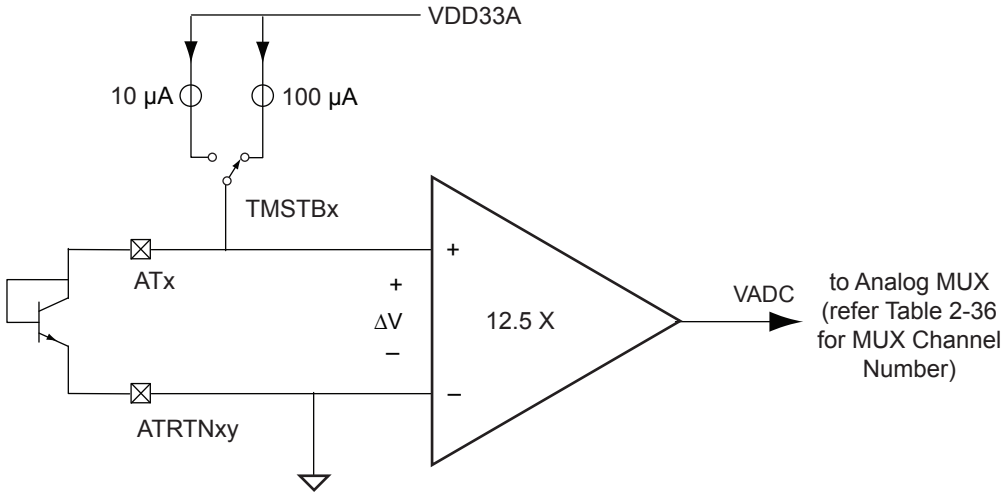

Figure 2-77 • **Block Diagram for Temperature Monitor Circuit**

The Fusion approach to measuring temperature is forcing two different currents through the diode with a ratio of 10:1. The switch that controls the different currents is controlled by the Temperature Monitor Strobe signal, TMSTB. Setting TMSTB to '1' will initiate a Temperature reading. The TMSTB should remain '1' until the ADC finishes sampling the voltage from the Temperature Monitor. The minimum sample time for the Temperature Monitor cannot be less than the minimum strobe high time minus the setup time. Figure 2-78 shows the timing diagram.

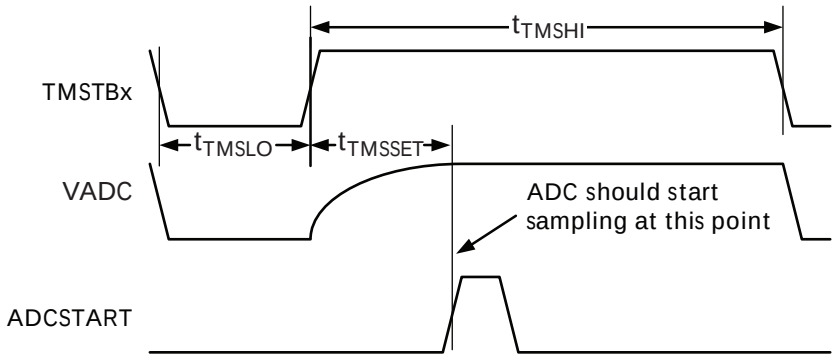

Figure 2-78 • **Timing Diagram for the Temperature Monitor Strobe Signal**

Note: When the IEEE 1149.1 Boundary Scan EXTEST instruction is executed, the AG pad drive strength ceases and becomes a 1 µA sink into the Fusion device.

ADC Terminology

Conversion Time

Conversion time is the interval between the release of the hold state (imposed by the input circuitry of a track-and-hold) and the instant at which the voltage on the sampling capacitor settles to within one LSB of a new input value.

DNL – Differential Non-Linearity

For an ideal ADC, the analog-input levels that trigger any two successive output codes should differ by one LSB (DNL = 0). Any deviation from one LSB in defined as DNL (Figure 2-83).

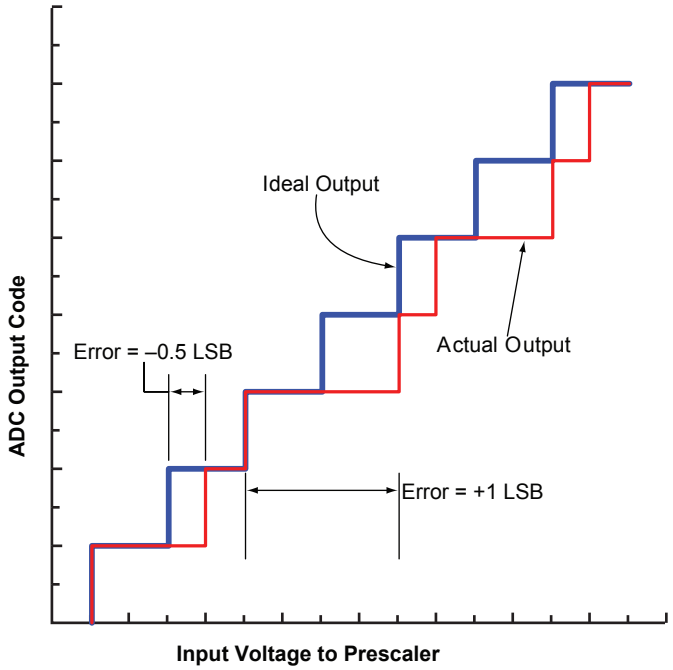

Figure 2-83 • **Differential Non-Linearity (DNL)**

ENOB – Effective Number of Bits

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists only of quantization of noise. As the input frequency increases, the overall noise (particularly in the distortion components) also increases, thereby reducing the ENOB and SINAD (also see "Signal-to-Noise and Distortion Ratio (SINAD)".) ENOB for a full-scale, sinusoidal input waveform is computed using EQ 12.

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

EQ 12

FS Error – Full-Scale Error

Full-scale error is the difference between the actual value that triggers that transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error.

ADC Input Multiplexer

At the input to the Fusion ADC is a 32:1 multiplexer. Of the 32 input channels, up to 30 are user definable. Two of these channels are hardwired internally. Channel 31 connects to an internal temperature diode so the temperature of the Fusion device itself can be monitored. Channel 0 is wired to the FPGA's 1.5 V VCC supply, enabling the Fusion device to monitor its own power supply. Doing this internally makes it unnecessary to use an analog I/O to support these functions. The balance of the MUX inputs are connected to Analog Quads (see the "Analog Quad" section on page 2-80). Table 2-40 defines which Analog Quad inputs are associated with which specific analog MUX channels. The number of Analog Quads present is device-dependent; refer to the family list in the "Fusion Family" table on page I of this datasheet for the number of quads per device. Regardless of the number of quads populated in a device, the internal connections to both VCC and the internal temperature diode remain on Channels 0 and 31, respectively. To sample the internal temperature monitor, it must be strobed (similar to the AT pads). The TMSTBINT pin on the Analog Block macro is the control for strobing the internal temperature measurement diode.

To determine which channel is selected for conversion, there is a five-pin interface on the Analog Block, CHNUMBER[4:0], defined in Table 2-39.

***Table 2-39* • Channel Selection**

Channel Number	CHNUMBER[4:0]
0	00000
1	00001
2	00010
3	00011
. . .	. . .
30	11110
31	11111

Table 2-40 shows the correlation between the analog MUX input channels and the analog input pins.

***Table 2-40* • Analog MUX Channels**

Analog MUX Channel	Signal	Analog Quad Number
0	Vcc_analog	
1	AV0	Analog Quad 0
2	AC0	
3	AT0	
4	AV1	Analog Quad 1
5	AC1	
6	AT1	
7	AV2	Analog Quad 2
8	AC2	
9	AT2	
10	AV3	Analog Quad 3
11	AC3	
12	AT3	
13	AV4	Analog Quad 4
14	AC4	
15	AT4	

Features Supported on Pro I/Os

Table 2-72 lists all features supported by transmitter/receiver for single-ended and differential I/Os.

***Table 2-72* • Fusion Pro I/O Features**

Feature	Description
Single-ended and voltage-referenced transmitter features	• Hot insertion in every mode except PCI or 5 V input tolerant (these modes use clamp diodes and do not allow hot insertion)
	• Activation of hot insertion (disabling the clamp diode) is selectable by I/Os.
	• Weak pull-up and pull-down
	• Two slew rates
	• Skew between output buffer enable/disable time: 2 ns delay (rising edge) and 0 ns delay (falling edge); see "Selectable Skew between Output Buffer Enable/Disable Time" on page 2-149 for more information
	• Five drive strengths
	• 5 V–tolerant receiver ("5 V Input Tolerance" section on page 2-144)
	• LVTTL/LVCMOS 3.3 V outputs compatible with 5 V TTL inputs ("5 V Output Tolerance" section on page 2-148)
	• High performance (Table 2-76 on page 2-143)
Single-ended receiver features	• Schmitt trigger option
	• ESD protection
	• Programmable delay: 0 ns if bypassed, 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V)
	• High performance (Table 2-76 on page 2-143)
	• Separate ground planes, GND/GNDQ, for input buffers only to avoid output-induced noise in the input circuitry
Voltage-referenced differential receiver features	• Programmable Delay: 0 ns if bypassed, 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V)
	• High performance (Table 2-76 on page 2-143)
	• Separate ground planes, GND/GNDQ, for input buffers only to avoid output-induced noise in the input circuitry
CMOS-style LVDS, BLVDS, M-LVDS, or LVPECL transmitter	• Two I/Os and external resistors are used to provide a CMOS-style LVDS, BLVDS, M-LVDS, or LVPECL transmitter solution.
	• Activation of hot insertion (disabling the clamp diode) is selectable by I/Os.
	• Weak pull-up and pull-down
	• Fast slew rate
LVDS/LVPECL differential receiver features	• ESD protection
	• High performance (Table 2-76 on page 2-143)
	• Programmable delay: 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V)
	• Separate input buffer ground and power planes to avoid output-induced noise in the input circuitry

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-90 • Summary of AC Measuring Points Applicable to All I/O Bank Types

Standard	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_REF)	Measuring Trip Point (Vtrip)
3.3 V LVTTL / 3.3 V LVCMOS	–	–	1.4 V
2.5 V LVCMOS	–	–	1.2 V
1.8 V LVCMOS	–	–	0.90 V
1.5 V LVCMOS	–	–	0.75 V
3.3 V PCI	–	–	0.285 * VCCI (RR) 0.615 * VCCI (FF))
3.3 V PCI-X	–	–	0.285 * VCCI (RR) 0.615 * VCCI (FF)
3.3 V GTL	0.8 V	1.2 V	VREF
2.5 V GTL	0.8 V	1.2 V	VREF
3.3 V GTL+	1.0 V	1.5 V	VREF
2.5 V GTL+	1.0 V	1.5 V	VREF
HSTL (I)	0.75 V	0.75 V	VREF
HSTL (II)	0.75 V	0.75 V	VREF
SSTL2 (I)	1.25 V	1.25 V	VREF
SSTL2 (II)	1.25 V	1.25 V	VREF
SSTL3 (I)	1.5 V	1.485 V	VREF
SSTL3 (II)	1.5 V	1.485 V	VREF
LVDS	–	–	Cross point
LVPECL	–	–	Cross point

Table 2-91 • I/O AC Parameter Definitions

Parameter	Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer with Schmitt trigger disabled
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{PYS}	Pad to Data delay through the Input Buffer with Schmitt trigger enabled
t_{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

Timing Characteristics

Table 2-120 • 1.8 V LVCMOS Low Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Pro I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	15.84	0.04	1.45	1.91	0.43	15.65	15.84	2.78	1.58	17.89	18.07	ns
	–1	0.56	13.47	0.04	1.23	1.62	0.36	13.31	13.47	2.37	1.35	15.22	15.37	ns
	–2	0.49	11.83	0.03	1.08	1.42	0.32	11.69	11.83	2.08	1.18	13.36	13.50	ns
4 mA	Std.	0.66	11.39	0.04	1.45	1.91	0.43	11.60	10.76	3.26	2.77	13.84	12.99	ns
	–1	0.56	9.69	0.04	1.23	1.62	0.36	9.87	9.15	2.77	2.36	11.77	11.05	ns
	–2	0.49	8.51	0.03	1.08	1.42	0.32	8.66	8.03	2.43	2.07	10.33	9.70	ns
8 mA	Std.	0.66	8.97	0.04	1.45	1.91	0.43	9.14	8.10	3.57	3.36	11.37	10.33	ns
	–1	0.56	7.63	0.04	1.23	1.62	0.36	7.77	6.89	3.04	2.86	9.67	8.79	ns
	–2	0.49	6.70	0.03	1.08	1.42	0.32	6.82	6.05	2.66	2.51	8.49	7.72	ns
12 mA	Std.	0.66	8.35	0.04	1.45	1.91	0.43	8.50	7.59	3.64	3.52	10.74	9.82	ns
	–1	0.56	7.10	0.04	1.23	1.62	0.36	7.23	6.45	3.10	3.00	9.14	8.35	ns
	–2	0.49	6.24	0.03	1.08	1.42	0.32	6.35	5.66	2.72	2.63	8.02	7.33	ns
16 mA	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	–1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	–2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-144 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
35 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35	181	268	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

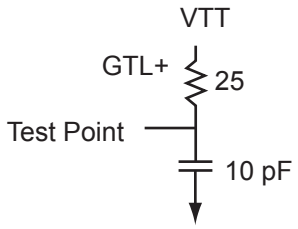

Figure 2-126 • AC Loading

Table 2-145 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-146 • 3.3 V GTL+
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.06	0.04	1.59	0.43	2.09	2.06			4.33	4.29	ns
–1	0.56	1.75	0.04	1.35	0.36	1.78	1.75			3.68	3.65	ns
–2	0.49	1.53	0.03	1.19	0.32	1.56	1.53			3.23	3.20	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-156 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
15 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15	87	83	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

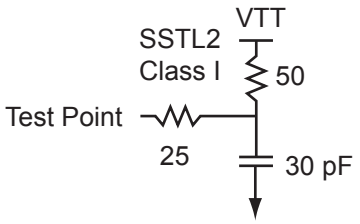

Figure 2-130 • AC Loading

Table 2-157 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-158 • SSTL 2 Class I
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.13	0.04	1.33	0.43	2.17	1.85			4.40	4.08	ns
–1	0.56	1.81	0.04	1.14	0.36	1.84	1.57			3.74	3.47	ns
–2	0.49	1.59	0.03	1.00	0.32	1.62	1.38			3.29	3.05	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-165 • Minimum and Maximum DC Input and Output Levels

SSTL3 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
21 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21	109	103	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

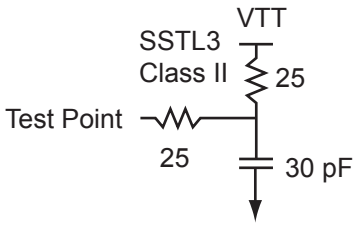

Figure 2-133 • AC Loading

Table 2-166 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-167 • SSTL3- Class II
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.07	0.04	1.25	0.43	2.10	1.67			4.34	3.91	ns
–1	0.56	1.76	0.04	1.06	0.36	1.79	1.42			3.69	3.32	ns
–2	0.49	1.54	0.03	0.93	0.32	1.57	1.25			3.24	2.92	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Input Register

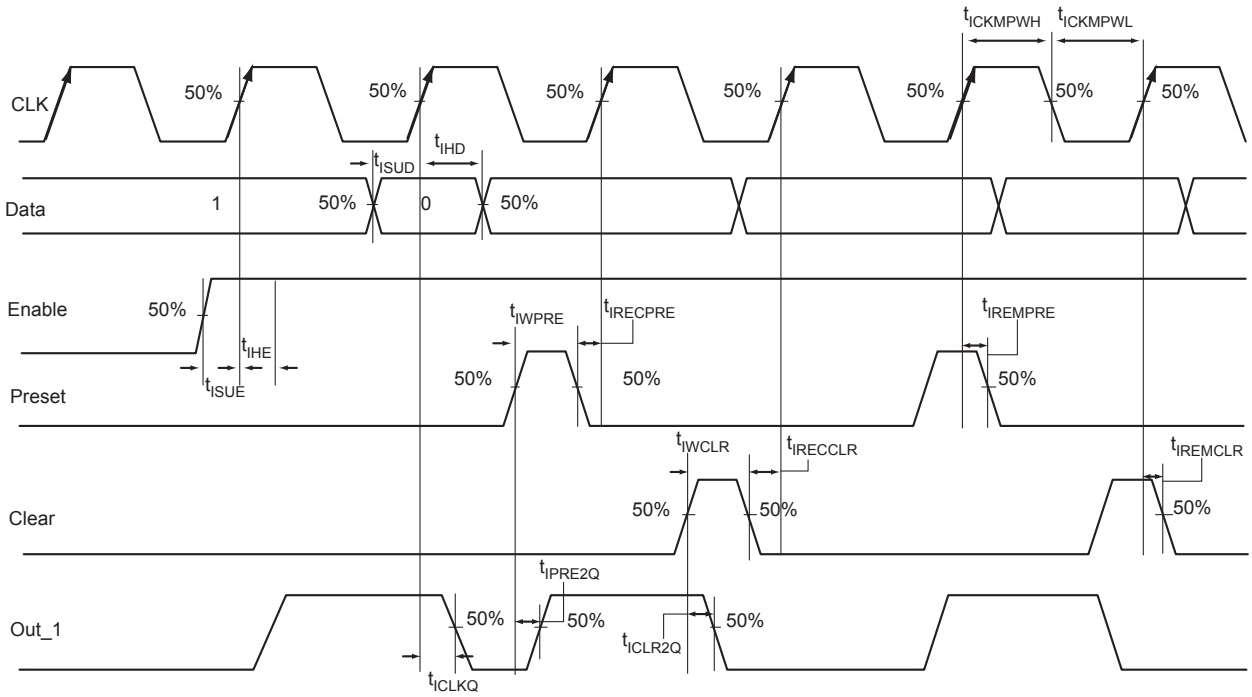

***Figure 2-139* • Input Register Timing Diagram**

Timing Characteristics

***Table 2-176* • Input Data Register Propagation Delays**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.27	0.32	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.26	0.30	0.35	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.37	0.42	0.50	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.45	0.52	0.61	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.45	0.52	0.61	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.41	0.48	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.37	0.43	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 3-3 • **Input Resistance of Analog Pads**

Pads	Pad Configuration	Prescaler Range	Input Resistance to Ground
AV, AC	Analog Input (direct input to ADC)	–	2 kΩ (typical)
		–	> 10 MΩ
	Analog Input (positive prescaler)	+16 V to +2 V	1 MΩ (typical)
		+1 V to +0.125 V	> 10 MΩ
	Analog Input (negative prescaler)	–16 V to –2 V	1 MΩ (typical)
		–1 V to –0.125 V	> 10 MΩ
	Digital input	+16 V to +2 V	1 MΩ (typical)
	Current monitor	+16 V to +2 V	1 MΩ (typical)
		–16 V to –2 V	1 MΩ (typical)
AT	Analog Input (direct input to ADC)	–	1 MΩ (typical)
	Analog Input (positive prescaler)	+16 V, +4 V	1 MΩ (typical)
	Digital input	+16 V, +4 V	1 MΩ (typical)
	Temperature monitor	+16 V, +4 V	> 10 MΩ

Table 3-4 • **Overshoot and Undershoot Limits** [1]

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3.0 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at a junction temperature of 85°C.*
2. *The duration is allowed at one cycle out of six clock cycle. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the AFS600-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

where

θ_{JA} = 19.00°C/W (taken from Table 3-6 on page 3-7).

T_A = 75.00°C

$$\text{Maximum Power Allowed} = \frac{100.00°C - 75.00°C}{19.00°C/W} = 1.3\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculation for Heat Sink

For example, in a design implemented in an AFS600-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent T_a and T_j are given as follows:

T_J = 100.00°C

T_A = 70.00°C

From the datasheet:

θ_{JA} = 17.00°C/W

θ_{JC} = 8.28°C/W

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100°C - 70°C}{17.00\ W} = 1.76\ W$$

EQ 6

Calculating Power Dissipation

Quiescent Supply Current

Table 3-8 • **AFS1500 Quiescent Supply Current Characteristics**

Parameter	Description	Conditions	Temp.	Min.	Typ.	Max.	Unit
ICC[1]	1.5 V quiescent current	Operational standby[4], VCC = 1.575 V	T_J = 25°C		20	40	mA
			T_J = 85°C		32	65	mA
			T_J = 100°C		59	120	mA
		Standby mode[5] or Sleep mode[6], VCC = 0 V			0	0	µA
ICC33[2]	3.3 V analog supplies current	Operational standby[4], VCC33 = 3.63 V	T_J = 25°C		9.8	13	mA
			T_J = 85°C		10.7	14	mA
			T_J = 100°C		10.8	15	mA
		Operational standby, only Analog Quad and –3.3 V output ON, VCC33 = 3.63 V	T_J = 25°C		0.31	2	mA
			T_J = 85°C		0.35	2	mA
			T_J = 100°C		0.45	2	mA
		Standby mode[5], VCC33 = 3.63 V	T_J = 25°C		2.9	3.6	mA
			T_J = 85°C		2.9	4	mA
			T_J = 100°C		3.3	6	mA
		Sleep mode[6], VCC33 = 3.63 V	T_J = 25°C		17	19	µA
			T_J = 85°C		18	20	µA
			T_J = 100°C		24	25	µA
ICCI[3]	I/O quiescent current	Operational standby[4], Standby mode, and Sleep Mode[6], VCCIx = 3.63 V	T_J = 25°C		417	649	µA
			T_J = 85°C		417	649	µA
			T_J = 100°C		417	649	µA

Notes:

1. *ICC is the 1.5 V power supplies, ICC and ICC15A.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPUMP = 0 V.*

Power per I/O Pin

***Table 3-12* • Summary of I/O Input Buffer Power (per pin)—Default I/O Software Settings**

	VCCI (V)	Static Power PDC7 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Applicable to Pro I/O Banks			
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3	–	17.39
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	–	25.51
2.5 V LVCMOS	2.5	–	5.76
2.5 V LVCMOS – Schmitt trigger	2.5	–	7.16
1.8 V LVCMOS	1.8	–	2.72
1.8 V LVCMOS – Schmitt trigger	1.8	–	2.80
1.5 V LVCMOS (JESD8-11)	1.5	–	2.08
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	2.00
3.3 V PCI	3.3	–	18.82
3.3 V PCI – Schmitt trigger	3.3	–	20.12
3.3 V PCI-X	3.3	–	18.82
3.3 V PCI-X – Schmitt trigger	3.3	–	20.12
Voltage-Referenced			
3.3 V GTL	3.3	2.90	8.23
2.5 V GTL	2.5	2.13	4.78
3.3 V GTL+	3.3	2.81	4.14
2.5 V GTL+	2.5	2.57	3.71
HSTL (I)	1.5	0.17	2.03
HSTL (II)	1.5	0.17	2.03
SSTL2 (I)	2.5	1.38	4.48
SSTL2 (II)	2.5	1.38	4.48
SSTL3 (I)	3.3	3.21	9.26
SSTL3 (II)	3.3	3.21	9.26
Differential			
LVDS	2.5	2.26	1.50
LVPECL	3.3	5.71	2.17

Notes:

1. *PDC7 is the static power (where applicable) measured on VCCI.*
2. *PAC9 is the total dynamic power measured on VCC and VCCI.*

Methodology

Total Power Consumption—P_{TOTAL}

Operating Mode, Standby Mode, and Sleep Mode

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

Operating Mode

$P_{STAT} = PDC1 + (N_{NVM\text{-}BLOCKS} * PDC4) + PDC5+ (N_{QUADS} * PDC6) + (N_{INPUTS} * PDC7) + (N_{OUTPUTS} * PDC8) + (N_{PLLS} * PDC9)$

$N_{NVM\text{-}BLOCKS}$ is the number of NVM blocks available in the device.

N_{QUADS} is the number of Analog Quads used in the design.

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{PLLS} is the number of PLLs available in the device.

Standby Mode

$P_{STAT} = PDC2$

Sleep Mode

$P_{STAT} = PDC3$

Total Dynamic Power Consumption—P_{DYN}

Operating Mode

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM} + P_{XTL\text{-}OSC} + P_{RC\text{-}OSC} + P_{AB}$

Standby Mode

$P_{DYN} = P_{XTL\text{-}OSC}$

Sleep Mode

$P_{DYN} = 0$ W

Global Clock Dynamic Contribution—P_{CLOCK}

Operating Mode

$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Fusion and Extended Temperature Fusion FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *Fusion and Extended Temperature Fusion FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

Standby Mode and Sleep Mode

$P_{CLOCK} = 0$ W

Sequential Cells Dynamic Contribution—$P_{S\text{-}CELL}$

Operating Mode

Revision	Changes	Page
Advance 1.0 (continued)	In Table 2-47 • ADC Characteristics in Direct Input Mode, the commercial conditions were updated and note 2 is new.	2-121
	The $V_{CC33ACAP}$ signal name was changed to "XTAL1 Crystal Oscillator Circuit Input".	2-228
	Table 2-48 • Uncalibrated Analog Channel Accuracy* is new.	2-123
	Table 2-49 • Calibrated Analog Channel Accuracy [1,2,3] is new.	2-124
	Table 2-50 • Analog Channel Accuracy: Monitoring Standard Positive Voltages is new.	2-125
	In Table 2-57 • Voltage Polarity Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)*, the following I/O Bank names were changed: Hot-Swap changed to Standard LVDS changed to Advanced	2-131
	In Table 2-58 • Prescaler Op Amp Power-Down Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3), the following I/O Bank names were changed: Hot-Swap changed to Standard LVDS changed to Advanced	2-132
	In the title of Table 2-64 • I/O Standards Supported by Bank Type, LVDS I/O was changed to Advanced I/O.	2-134
	The title was changed from "Fusion Standard, LVDS, and Standard plus Hot-Swap I/O" to Table 2-68 • Fusion Standard and Advanced I/O Features. In addition, the table headings were all updated. The heading used to be Standard and LVDS I/O and was changed to Advanced I/O. Standard Hot-Swap was changed to just Standard.	2-136
	This sentence was deleted from the "Slew Rate Control and Drive Strength" section: The Standard hot-swap I/Os do not support slew rate control. In addition, these references were changed: • From: Fusion hot-swap I/O (Table 2-69 on page 2-122) To: Fusion Standard I/O • From: Fusion LVDS I/O (Table 2-70 on page 2-122) To: Fusion Advanced I/O	2-152
	The "Cold-Sparing Support" section was significantly updated.	2-143
	In the title of Table 2-75 • Fusion Standard I/O Standards—OUT_DRIVE Settings, Hot-Swap was changed to Standard.	2-153
	In the title of Table 2-76 • Fusion Advanced I/O Standards—SLEW and OUT_DRIVE Settings, LVDS was changed to Advanced.	2-153
	In the title of Table 2-81 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications, LVDS was changed to Advanced.	2-157
	In Figure 2-111 • Naming Conventions of Fusion Devices with Three Digital I/O Banks and Figure 2-112 • Naming Conventions of Fusion Devices with Four I/O Banks the following names were changed: Hot-Swap changed to Standard LVDS changed to Advanced	2-160
	The Figure 2-113 • Timing Model was updated.	2-161
	In the notes for Table 2-86 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions, T_J was changed to T_A.	2-166