Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	114
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs250-1fgg256i

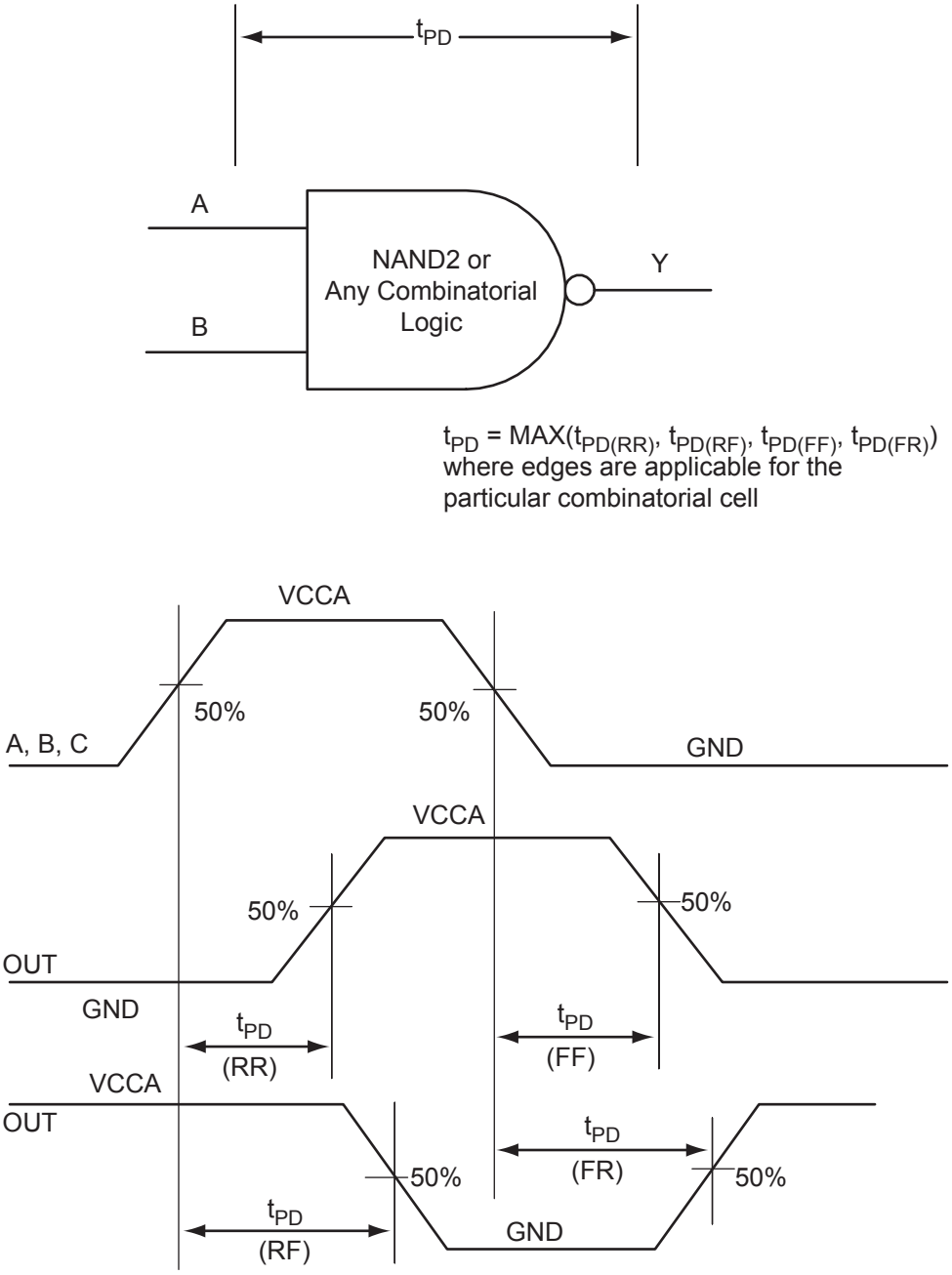

Figure 2-4 • **Combinatorial Timing Model and Waveforms**

The rate at which the gate voltage of the external MOSFET slews is determined by the current, I_g, sourced or sunk by the AG pin and the gate-to-source capacitance, C_{GS}, of the external MOSFET. As an approximation, the slew rate is given by EQ 6.

$$dv/dt = I_g / C_{GS}$$

EQ 6

C_{GS} is not a fixed capacitance but, depending on the circuitry connected to its drain terminal, can vary significantly during the course of a turn-on or turn-off transient. Thus, EQ 6 on page 2-91 can only be used for a first-order estimate of the switching speed of the external MOSFET.

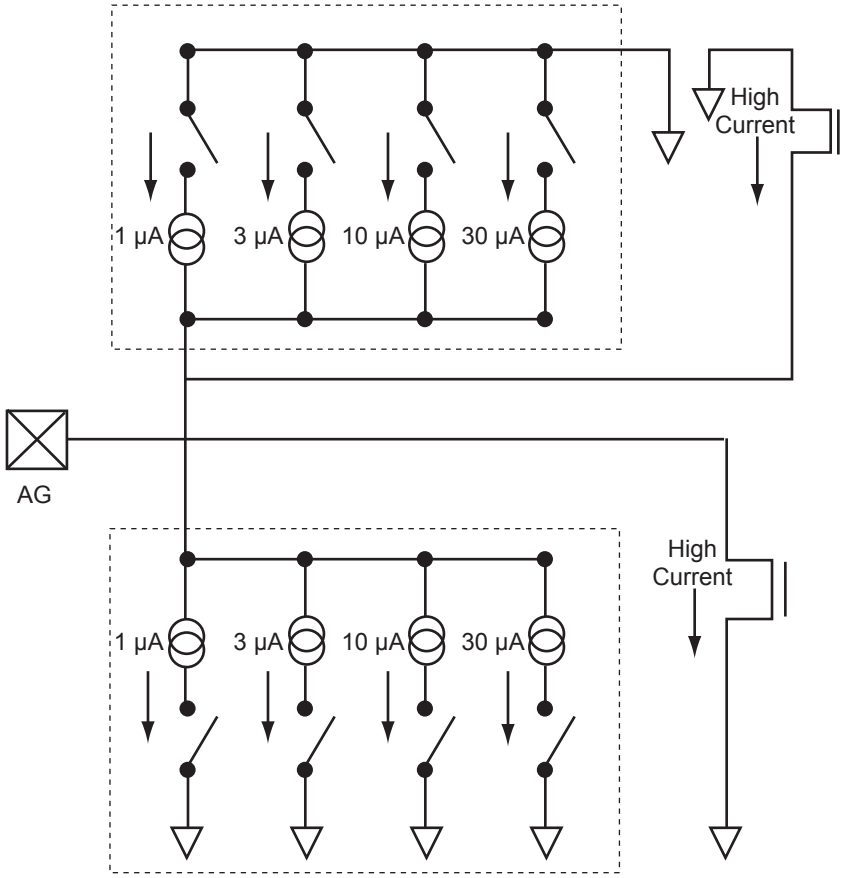

Figure 2-75 • **Gate Driver Example**

The diode's voltage is measured at each current level and the temperature is calculated based on EQ 7.

$$V_{TMSLO} - V_{TMSHI} = n\frac{kT}{q}\left(\ln\frac{I_{TMSLO}}{I_{TMSHI}}\right)$$

EQ 7

where

I_{TMSLO} is the current when the Temperature Strobe is Low, typically 100 µA

I_{TMSHI} is the current when the Temperature Strobe is High, typically 10 µA

V_{TMSLO} is diode voltage while Temperature Strobe is Low

V_{TMSHI} is diode voltage while Temperature Strobe is High

n is the non-ideality factor of the diode-connected transistor. It is typically 1.004 for the Microsemi-recommended transistor type 2N3904.

K = 1.3806 x 10^{-23} J/K is the Boltzman constant

Q = 1.602 x 10^{-19} C is the charge of a proton

When I_{TMSLO} / I_{TMSHI} = 10, the equation can be simplified as shown in EQ 8.

$$\Delta V = V_{TMSLO} - V_{TMSHI} = 1.986 \times 10^{-4} nT$$

EQ 8

In the Fusion TMB, the ideality factor n for 2N3904 is 1.004 and ΔV is amplified 12.5 times by an internal amplifier; hence the voltage before entering the ADC is as given in EQ 9.

$$V_{ADC} = \Delta V \times 12.5 = 2.5\ \text{mV}/(K \times T)$$

EQ 9

This means the temperature to voltage relationship is 2.5 mV per degree Kelvin. The unique design of Fusion has made the Temperature Monitor System simple for the user. When the 10-bit mode ADC is used, each LSB represents 1 degree Kelvin, as shown in EQ 10. That is, e. 25°C is equal to 293°K and is represented by decimal 293 counts from the ADC.

$$1K = 2.5\ \text{mV} \times \frac{2^{10}}{2.56\ \text{V}} = 1\ \text{LSB}$$

EQ 10

If 8-bit mode is used for the ADC resolution, each LSB represents 4 degrees Kelvin; however, the resolution remains as 1 degree Kelvin per LSB, even for 12-bit mode, due to the Temperature Monitor design. An example of the temperature data format for 10-bit mode is shown in Table 2-38.

***Table 2-38* • Temperature Data Format**

Temperature	Temperature (K)	Digital Output (ADC 10-bit mode)
–40°C	233	00 1110 1001
–20°C	253	00 1111 1101
0°C	273	01 0001 0001
1°C	274	01 0001 0010
10 °C	283	01 0001 1011
25°C	298	01 0010 1010
50 °C	323	01 0100 0011
85 °C	358	01 0110 0110

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions Applicable to Pro I/Os

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	IOL	IOH
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI Specification									
3.3 V PCI-X	Per PCI-X Specification									
3.3 V GTL	20 mA[2]	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
2.5 V GTL	20 mA[2]	High	–0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	–	20	20
3.3 V GTL+	35 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35
2.5 V GTL+	33 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	33	33
HSTL (I)	8 mA	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8
HSTL (II)	15 mA[2]	High	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	15	15
SSTL2 (I)	15 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15
SSTL2 (II)	18 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18
SSTL3 (I)	14 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.7	VCCI – 1.1	14	14
SSTL3 (II)	21 mA	High	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *Output drive strength is below JEDEC specification.*
3. *Output slew rate can be extracted by the IBIS models.*

Table 2-87 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions Applicable to Advanced I/Os

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	IOL	IOH
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Note: Currents are measured at 85°C junction temperature.

***Table 2-98* • I/O Short Currents IOSH/IOSL**

	Drive Strength	IOSH (mA)*	IOSL (mA)*
Applicable to Pro I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
Applicable to Advanced I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181

Note: *T_J = 100°C

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-110 • Minimum and Maximum DC Input and Output Levels

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
Applicable to Pro I/O Banks												
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10
Applicable to Advanced I/O Banks												
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	124	169	10	10
Applicable to Standard I/O Banks												
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	18	16	10	10
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	37	32	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

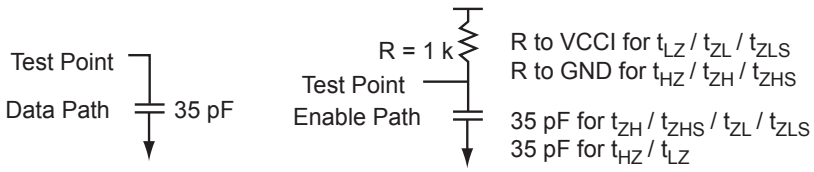

Figure 2-120 • AC Loading

Table 2-111 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

***Table 2-112* • 2.5 V LVCMOS Low Slew**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 2.3 V
Applicable to Pro I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	12.00	0.04	1.51	1.66	0.43	12.23	11.61	2.72	2.20	14.46	13.85	ns
	–1	0.51	10.21	0.04	1.29	1.41	0.36	10.40	9.88	2.31	1.87	12.30	11.78	ns
	–2	0.45	8.96	0.03	1.13	1.24	0.32	9.13	8.67	2.03	1.64	10.80	10.34	ns
8 mA	Std.	0.60	8.73	0.04	1.51	1.66	0.43	8.89	8.01	3.10	2.93	11.13	10.25	ns
	–1	0.51	7.43	0.04	1.29	1.41	0.36	7.57	6.82	2.64	2.49	9.47	8.72	ns
	–2	0.45	6.52	0.03	1.13	1.24	0.32	6.64	5.98	2.32	2.19	8.31	7.65	ns
12 mA	Std.	0.66	6.77	0.04	1.51	1.66	0.43	6.90	6.11	3.37	3.39	9.14	8.34	ns
	–1	0.56	5.76	0.04	1.29	1.41	0.36	5.87	5.20	2.86	2.89	7.77	7.10	ns
	–2	0.49	5.06	0.03	1.13	1.24	0.32	5.15	4.56	2.51	2.53	6.82	6.23	ns
16 mA	Std.	0.66	6.31	0.04	1.51	1.66	0.43	6.42	5.73	3.42	3.52	8.66	7.96	ns
	–1	0.56	5.37	0.04	1.29	1.41	0.36	5.46	4.87	2.91	3.00	7.37	6.77	ns
	–2	0.49	4.71	0.03	1.13	1.24	0.32	4.80	4.28	2.56	2.63	6.47	5.95	ns
24 mA	Std.	0.66	5.93	0.04	1.51	1.66	0.43	6.04	5.70	3.49	4.00	8.28	7.94	ns
	–1	0.56	5.05	0.04	1.29	1.41	0.36	5.14	4.85	2.97	3.40	7.04	6.75	ns
	–2	0.49	4.43	0.03	1.13	1.24	0.32	4.51	4.26	2.61	2.99	6.18	5.93	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-144 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL+	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
35 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	–	35	35	181	268	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

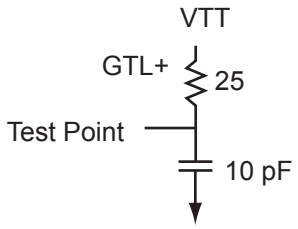

Figure 2-126 • AC Loading

Table 2-145 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-146 • 3.3 V GTL+
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.06	0.04	1.59	0.43	2.09	2.06			4.33	4.29	ns
–1	0.56	1.75	0.04	1.35	0.36	1.78	1.75			3.68	3.65	ns
–2	0.49	1.53	0.03	1.19	0.32	1.56	1.53			3.23	3.20	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-150 • Minimum and Maximum DC Input and Output Levels

HSTL Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
8 mA	–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCCI – 0.4	8	8	39	32	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

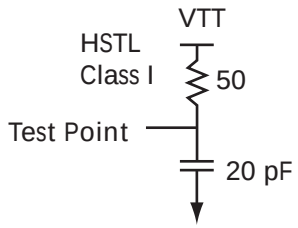

Figure 2-128 • AC Loading

Table 2-151 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.1	VREF + 0.1	0.75	0.75	0.75	20

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-152 • HSTL Class I
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V, VREF = 0.75 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	3.18	0.04	2.12	0.43	3.24	3.14			5.47	5.38	ns
–1	0.56	2.70	0.04	1.81	0.36	2.75	2.67			4.66	4.58	ns
–2	0.49	2.37	0.03	1.59	0.32	2.42	2.35			4.09	4.02	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-156 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
15 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15	87	83	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

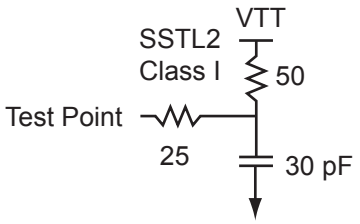

Figure 2-130 • AC Loading

Table 2-157 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-158 • SSTL 2 Class I
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.13	0.04	1.33	0.43	2.17	1.85			4.40	4.08	ns
–1	0.56	1.81	0.04	1.14	0.36	1.84	1.57			3.74	3.47	ns
–2	0.49	1.59	0.03	1.00	0.32	1.62	1.38			3.29	3.05	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-136. The building blocks of the LVPECL transmitter–receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

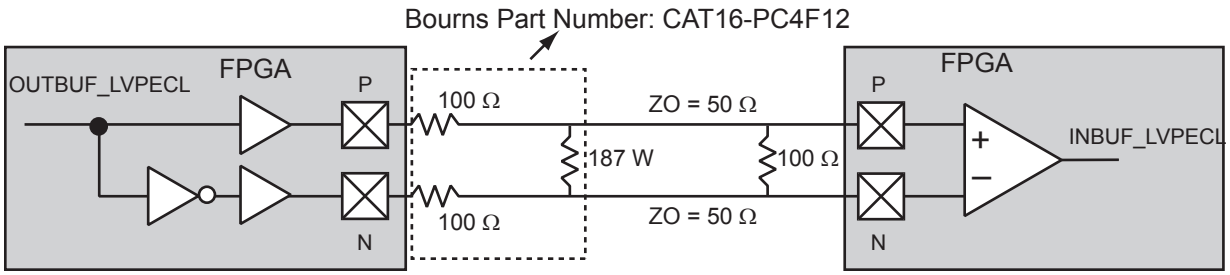

***Figure 2-136* • LVPECL Circuit Diagram and Board-Level Implementation**

***Table 2-171* • Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

***Table 2-172* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)
1.64	1.94	Cross point	–

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

***Table 2-173* • LVPECL**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V
Applicable to Pro I/Os

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.66	2.14	0.04	1.63	ns
–1	0.56	1.82	0.04	1.39	ns
–2	0.49	1.60	0.03	1.22	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

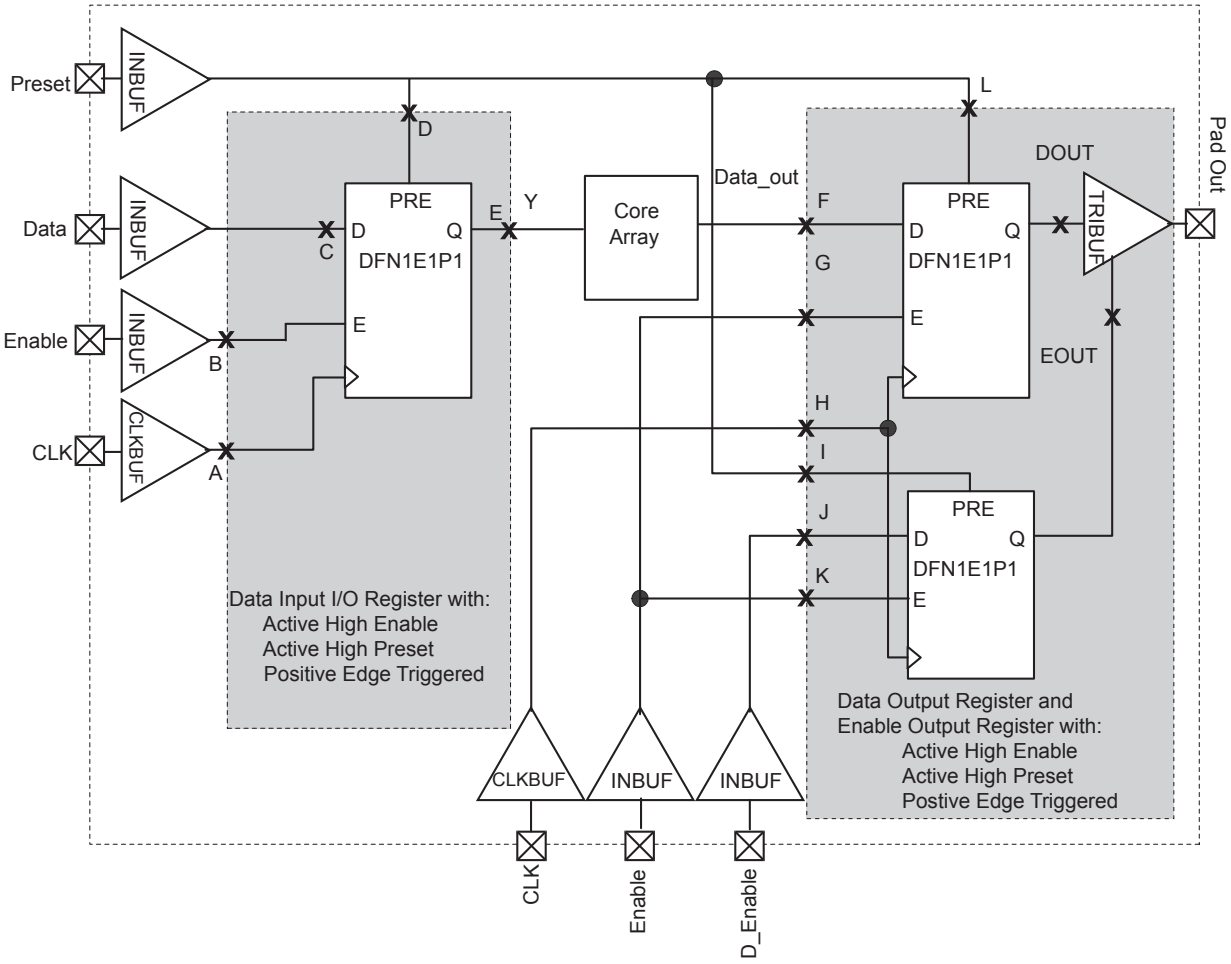

***Figure 2-137* • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Input Register

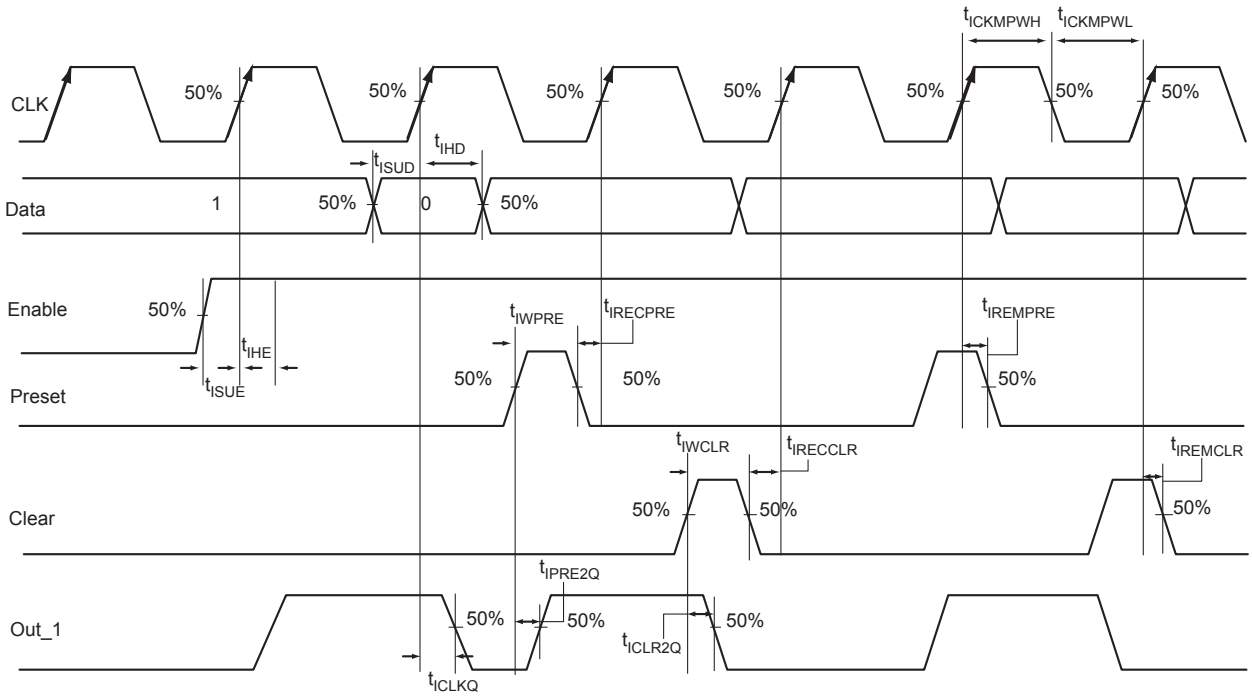

***Figure 2-139* • Input Register Timing Diagram**

Timing Characteristics

***Table 2-176* • Input Data Register Propagation Delays**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.27	0.32	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.26	0.30	0.35	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.37	0.42	0.50	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.45	0.52	0.61	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.45	0.52	0.61	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.41	0.48	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.37	0.43	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

User-Defined Supply Pins

VREF **I/O Voltage Reference**

Reference voltage for I/O minibanks. Both AFS600 and AFS1500 (north bank only) support Microsemi Pro I/O. These I/O banks support voltage reference standard I/O. The VREF pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated as the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One VREF pin can support the number of I/Os available in its minibank.

VAREF **Analog Reference Voltage**

The Fusion device can be configured to generate a 2.56 V internal reference voltage that can be used by the ADC. While using the internal reference, the reference voltage is output on the VAREF pin for use as a system reference. If a different reference voltage is required, it can be supplied by an external source and applied to this pin. The valid range of values that can be supplied to the ADC is 1.0 V to 3.3 V. When VAREF is internally generated by the Fusion device, a bypass capacitor must be connected from this pin to ground. The value of the bypass capacitor should be between 3.3 µF and 22 µF, which is based on the needs of the individual designs. The choice of the capacitor value has an impact on the settling time it takes the VAREF signal to reach the required specification of 2.56 V to initiate valid conversions by the ADC. If the lower capacitor value is chosen, the settling time required for VAREF to achieve 2.56 V will be shorter than when selecting the larger capacitor value. The above range of capacitor values supports the accuracy specification of the ADC, which is detailed in the datasheet. Designers choosing the smaller capacitor value will not obtain as much margin in the accuracy as that achieved with a larger capacitor value. Depending on the capacitor value selected in the Analog System Builder, a tool in Libero SoC, an automatic delay circuit will be generated using logic tiles available within the FPGA to ensure that VAREF has achieved the 2.56 V value. Microsemi recommends customers use 10 µF as the value of the bypass capacitor. Designers choosing to use an external VAREF need to ensure that a stable and clean VAREF source is supplied to the VAREF pin before initiating conversions by the ADC. Designers should also make sure that the ADCRESET signal is deasserted before initiating valid conversions.[2]

If the user connects VAREF to external 3.3 V on their board, the internal VAREF driving OpAmp tries to bring the pin down to the nominal 2.56 V until the device is programmed and up/functional. Under this scenario, it is recommended to connect an external 3.3 V supply through a ~1 KOhm resistor to limit current, along with placing a 10-100nF capacitor between VAREF and GNDA.

User Pins

I/O **User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected. Unused I/O pins are configured as inputs with pull-up resistors.

During programming, I/Os become tristated and weakly pulled up to VCCI. With the VCCI and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os get instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

A*xy* **Analog Input/Output**

Analog I/O pin, where *x* is the analog pad type (C = current pad, G = Gate driver pad, T = Temperature pad, V = Voltage pad) and *y* is the Analog Quad number (0 to 9). There is a minimum 1 MΩ to ground on AV, AC, and AT. This pin can be left floating when it is unused.

2. *The ADC is functional with an external reference down to 1V, however to meet the performance parameters highlighted in the datasheet refer to the VAREF specification in Table 3-2 on page 3-3.*

connected to the internal core logic I/O tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

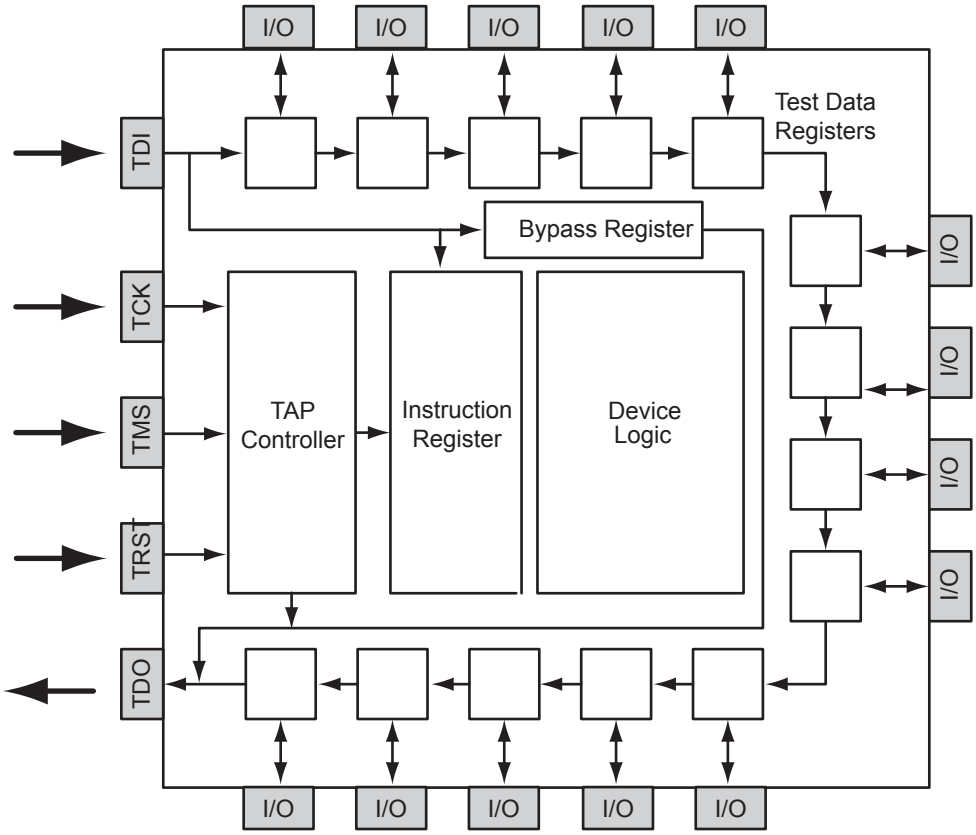

***Figure 2-146* • Boundary Scan Chain in Fusion**

***Table 2-185* • Boundary Scan Opcodes**

	Hex Opcode
EXTEST	00
HIGHZ	07
USERCODE	0E
SAMPLE/PRELOAD	01
IDCODE	0F
CLAMP	05
BYPASS	FF

PQ208		
Pin Number	AFS250 Function	AFS600 Function
74	AV2	AV4
75	AC2	AC4
76	AG2	AG4
77	AT2	AT4
78	ATRTN1	ATRTN2
79	AT3	AT5
80	AG3	AG5
81	AC3	AC5
82	AV3	AV5
83	AV4	AV6
84	AC4	AC6
85	AG4	AG6
86	AT4	AT6
87	ATRTN2	ATRTN3
88	AT5	AT7
89	AG5	AG7
90	AC5	AC7
91	AV5	AV7
92	NC	AV8
93	NC	AC8
94	NC	AG8
95	NC	AT8
96	NC	ATRTN4
97	NC	AT9
98	NC	AG9
99	NC	AC9
100	NC	AV9
101	GNDAQ	GNDAQ
102	VCC33A	VCC33A
103	ADCGNDREF	ADCGNDREF
104	VAREF	VAREF
105	PUB	PUB
106	VCC33A	VCC33A
107	GNDA	GNDA
108	PTEM	PTEM
109	PTBASE	PTBASE
110	GNDNVM	GNDNVM

PQ208		
Pin Number	AFS250 Function	AFS600 Function
111	VCCNVM	VCCNVM
112	VCC	VCC
112	VCC	VCC
113	VPUMP	VPUMP
114	GNDQ	NC
115	VCCIB1	TCK
116	TCK	TDI
117	TDI	TMS
118	TMS	TDO
119	TDO	TRST
120	TRST	VJTAG
121	VJTAG	IO57NDB2V0
122	IO57NDB1V0	GDC2/IO57PDB2V0
123	GDC2/IO57PDB1V0	IO56NDB2V0
124	IO56NDB1V0	GDB2/IO56PDB2V0
125	GDB2/IO56PDB1V0	IO55NDB2V0
126	VCCIB1	GDA2/IO55PDB2V0
127	GND	GDA0/IO54NDB2V0
128	IO55NDB1V0	GDA1/IO54PDB2V0
129	GDA2/IO55PDB1V0	VCCIB2
130	GDA0/IO54NDB1V0	GND
131	GDA1/IO54PDB1V0	VCC
132	GDB0/IO53NDB1V0	GCA0/IO45NDB2V0
133	GDB1/IO53PDB1V0	GCA1/IO45PDB2V0
134	GDC0/IO52NDB1V0	GCB0/IO44NDB2V0
135	GDC1/IO52PDB1V0	GCB1/IO44PDB2V0
136	IO51NSB1V0	GCC0/IO43NDB2V0
137	VCCIB1	GCC1/IO43PDB2V0
138	GND	IO42NDB2V0
139	VCC	IO42PDB2V0
140	IO50NDB1V0	IO41NDB2V0
141	IO50PDB1V0	GCC2/IO41PDB2V0
142	GCA0/IO49NDB1V0	VCCIB2
143	GCA1/IO49PDB1V0	GND
144	GCB0/IO48NDB1V0	VCC
145	GCB1/IO48PDB1V0	IO40NDB2V0
146	GCC0/IO47NDB1V0	GCB2/IO40PDB2V0

FG256				
Pin Number	**AFS090 Function**	**AFS250 Function**	**AFS600 Function**	**AFS1500 Function**
A1	GND	GND	GND	GND
A2	VCCIB0	VCCIB0	VCCIB0	VCCIB0
A3	GAB0/IO02RSB0V0	GAA0/IO00RSB0V0	GAA0/IO01NDB0V0	GAA0/IO01NDB0V0
A4	GAB1/IO03RSB0V0	GAA1/IO01RSB0V0	GAA1/IO01PDB0V0	GAA1/IO01PDB0V0
A5	GND	GND	GND	GND
A6	IO07RSB0V0	IO11RSB0V0	IO10PDB0V1	IO07PDB0V1
A7	IO10RSB0V0	IO14RSB0V0	IO12PDB0V1	IO13PDB0V2
A8	IO11RSB0V0	IO15RSB0V0	IO12NDB0V1	IO13NDB0V2
A9	IO16RSB0V0	IO24RSB0V0	IO22NDB1V0	IO24NDB1V0
A10	IO17RSB0V0	IO25RSB0V0	IO22PDB1V0	IO24PDB1V0
A11	IO18RSB0V0	IO26RSB0V0	IO24NDB1V1	IO29NDB1V1
A12	GND	GND	GND	GND
A13	GBC0/IO25RSB0V0	GBA0/IO38RSB0V0	GBA0/IO28NDB1V1	GBA0/IO42NDB1V2
A14	GBA0/IO29RSB0V0	IO32RSB0V0	IO29NDB1V1	IO43NDB1V2
A15	VCCIB0	VCCIB0	VCCIB1	VCCIB1
A16	GND	GND	GND	GND
B1	VCOMPLA	VCOMPLA	VCOMPLA	VCOMPLA
B2	VCCPLA	VCCPLA	VCCPLA	VCCPLA
B3	GAA0/IO00RSB0V0	IO07RSB0V0	IO00NDB0V0	IO00NDB0V0
B4	GAA1/IO01RSB0V0	IO06RSB0V0	IO00PDB0V0	IO00PDB0V0
B5	NC	GAB1/IO03RSB0V0	GAB1/IO02PPB0V0	GAB1/IO02PPB0V0
B6	IO06RSB0V0	IO10RSB0V0	IO10NDB0V1	IO07NDB0V1
B7	VCCIB0	VCCIB0	VCCIB0	VCCIB0
B8	IO12RSB0V0	IO16RSB0V0	IO18NDB1V0	IO22NDB1V0
B9	IO13RSB0V0	IO17RSB0V0	IO18PDB1V0	IO22PDB1V0
B10	VCCIB0	VCCIB0	VCCIB1	VCCIB1
B11	IO19RSB0V0	IO27RSB0V0	IO24PDB1V1	IO29PDB1V1
B12	GBB0/IO27RSB0V0	GBC0/IO34RSB0V0	GBC0/IO26NPB1V1	GBC0/IO40NPB1V2
B13	GBC1/IO26RSB0V0	GBA1/IO39RSB0V0	GBA1/IO28PDB1V1	GBA1/IO42PDB1V2
B14	GBA1/IO30RSB0V0	IO33RSB0V0	IO29PDB1V1	IO43PDB1V2
B15	NC	NC	VCCPLB	VCCPLB
B16	NC	NC	VCOMPLB	VCOMPLB
C1	VCCIB3	V**CCI**B3	VCCIB4	VCCIB4
C2	GND	GND	GND	GND
C3	VCCIB3	VCCIB3	VCCIB4	VCCIB4
C4	NC	NC	VCCIB0	VCCIB0
C5	VCCIB0	VCCIB0	VCCIB0	VCCIB0
C6	GAC1/IO05RSB0V0	GAC1/IO05RSB0V0	GAC1/IO03PDB0V0	GAC1/IO03PDB0V0

FG484		
Pin Number	AFS600 Function	AFS1500 Function
A1	GND	GND
A2	VCC	NC
A3	GAA1/IO01PDB0V0	GAA1/IO01PDB0V0
A4	GAB0/IO02NDB0V0	GAB0/IO02NDB0V0
A5	GAB1/IO02PDB0V0	GAB1/IO02PDB0V0
A6	IO07NDB0V1	IO07NDB0V1
A7	IO07PDB0V1	IO07PDB0V1
A8	IO10PDB0V1	IO09PDB0V1
A9	IO14NDB0V1	IO13NDB0V2
A10	IO14PDB0V1	IO13PDB0V2
A11	IO17PDB1V0	IO24PDB1V0
A12	IO18PDB1V0	IO26PDB1V0
A13	IO19NDB1V0	IO27NDB1V1
A14	IO19PDB1V0	IO27PDB1V1
A15	IO24NDB1V1	IO35NDB1V2
A16	IO24PDB1V1	IO35PDB1V2
A17	GBC0/IO26NDB1V1	GBC0/IO40NDB1V2
A18	GBA0/IO28NDB1V1	GBA0/IO42NDB1V2
A19	IO29NDB1V1	IO43NDB1V2
A20	IO29PDB1V1	IO43PDB1V2
A21	VCC	NC
A22	GND	GND
AA1	VCC	NC
AA2	GND	GND
AA3	VCCIB4	VCCIB4
AA4	VCCIB4	VCCIB4
AA5	PCAP	PCAP
AA6	AG0	AG0
AA7	GNDA	GNDA
AA8	AG1	AG1
AA9	AG2	AG2
AA10	GNDA	GNDA
AA11	AG3	AG3
AA12	AG6	AG6
AA13	GNDA	GNDA

FG484		
Pin Number	AFS600 Function	AFS1500 Function
AA14	AG7	AG7
AA15	AG8	AG8
AA16	GNDA	GNDA
AA17	AG9	AG9
AA18	VAREF	VAREF
AA19	VCCIB2	VCCIB2
AA20	PTEM	PTEM
AA21	GND	GND
AA22	VCC	NC
AB1	GND	GND
AB2	VCC	NC
AB3	NC	IO94NSB4V0
AB4	GND	GND
AB5	VCC33N	VCC33N
AB6	AT0	AT0
AB7	ATRTN0	ATRTN0
AB8	AT1	AT1
AB9	AT2	AT2
AB10	ATRTN1	ATRTN1
AB11	AT3	AT3
AB12	AT6	AT6
AB13	ATRTN3	ATRTN3
AB14	AT7	AT7
AB15	AT8	AT8
AB16	ATRTN4	ATRTN4
AB17	AT9	AT9
AB18	VCC33A	VCC33A
AB19	GND	GND
AB20	NC	IO76NPB2V0
AB21	VCC	NC
AB22	GND	GND
B1	VCC	NC
B2	GND	GND
B3	GAA0/IO01NDB0V0	GAA0/IO01NDB0V0
B4	GND	GND

FG676	
Pin Number	**AFS1500 Function**
AD5	IO94NPB4V0
AD6	GND
AD7	VCC33N
AD8	AT0
AD9	ATRTN0
AD10	AT1
AD11	AT2
AD12	ATRTN1
AD13	AT3
AD14	AT6
AD15	ATRTN3
AD16	AT7
AD17	AT8
AD18	ATRTN4
AD19	AT9
AD20	VCC33A
AD21	GND
AD22	IO76NPB2V0
AD23	NC
AD24	GND
AD25	NC
AD26	NC
AE1	GND
AE2	GND
AE3	NC
AE4	NC
AE5	NC
AE6	NC
AE7	NC
AE8	NC
AE9	GNDA
AE10	NC
AE11	NC
AE12	GNDA
AE13	NC
AE14	NC

FG676	
Pin Number	**AFS1500 Function**
AE15	GNDA
AE16	NC
AE17	NC
AE18	GNDA
AE19	NC
AE20	NC
AE21	NC
AE22	NC
AE23	NC
AE24	NC
AE25	GND
AE26	GND
AF1	NC
AF2	GND
AF3	NC
AF4	NC
AF5	NC
AF6	NC
AF7	NC
AF8	NC
AF9	VCC33A
AF10	NC
AF11	NC
AF12	VCC33A
AF13	NC
AF14	NC
AF15	VCC33A
AF16	NC
AF17	NC
AF18	VCC33A
AF19	NC
AF20	NC
AF21	NC
AF22	NC
AF23	NC
AF24	NC

FG676	
Pin Number	**AFS1500 Function**
AF25	GND
AF26	NC
B1	GND
B2	GND
B3	NC
B4	NC
B5	NC
B6	VCCIB0
B7	NC
B8	NC
B9	VCCIB0
B10	IO15NDB0V2
B11	IO15PDB0V2
B12	VCCIB0
B13	IO19NDB0V2
B14	IO19PDB0V2
B15	VCCIB1
B16	IO25NDB1V0
B17	IO25PDB1V0
B18	VCCIB1
B19	IO33NDB1V1
B20	IO33PDB1V1
B21	VCCIB1
B22	NC
B23	NC
B24	NC
B25	GND
B26	GND
C1	NC
C2	NC
C3	GND
C4	NC
C5	GAA1/IO01PDB0V0
C6	GAB0/IO02NDB0V0
C7	GAB1/IO02PDB0V0
C8	IO07NDB0V1

Revision	Changes	Page
Advance v0.6 (continued)	The "Analog-to-Digital Converter Block" section was updated with the following statement: "All results are MSB justified in the ADC."	2-99
	The information about the ADCSTART signal was updated in the "ADC Description" section.	2-102
	Table 2-46 · Analog Channel Specifications was updated.	2-118
	Table 2-47 · ADC Characteristics in Direct Input Mode was updated.	2-121
	Table 2-51 • ACM Address Decode Table for Analog Quad was updated.	2-127
	In Table 2-53 • Analog Quad ACM Byte Assignment, the Function and Default Setting for Bit 6 in Byte 3 was updated.	2-130
	The "Introduction" section was updated to include information about digital inputs, outputs, and bibufs.	2-133
	In Table 2-69 • Fusion Pro I/O Features, the programmable delay descriptions were updated for the following features: Single-ended receiver Voltage-referenced differential receiver LVDS/LVPECL differential receiver features	2-137
	The "User I/O Naming Convention" section was updated to include "V" and "z" descriptions	2-159
	The "VCC33PMP Analog Power Supply (3.3 V)" section was updated to include information about avoiding high current draw.	2-224
	The "VCCNVM Flash Memory Block Power Supply (1.5 V)" section was updated to include information about avoiding high current draw.	2-224
	The "VMVx I/O Supply Voltage (quiet)" section was updated to include this statement: VMV and VCCI must be connected to the same power supply and V_{CCI} pins within a given I/O bank.	2-185
	The "PUB Push Button" section was updated to include information about leaving the pin floating if it is not used.	2-228
	The "PTBASE Pass Transistor Base" section was updated to include information about leaving the pin floating if it is not used.	2-228
	The "PTEM Pass Transistor Emitter" section was updated to include information about leaving the pin floating if it is not used.	2-228
	The heading was incorrect in the "208-Pin PQFP" table. It should be AFS250 and not AFS090.	3-8