Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	114
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs250-fgg256i

The FlashPoint tool in the Fusion development software solutions, Libero SoC and Designer, has extensive support for flash memory blocks and FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using the Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

Fusion devices have embedded SRAM blocks along the north and south sides of the device. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be written through a 4-bit port and read as a single bitstream. The SRAM blocks can be initialized from the flash memory blocks or via the device JTAG port (ROM emulation mode), using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal EMPTY and FULL flags. The embedded FIFO control unit contains the counters necessary for the generation of the read and write address pointers. The SRAM/FIFO blocks can be cascaded to create larger configurations.

Clock Resources

PLLs and Clock Conditioning Circuits (CCCs)

Fusion devices provide designers with very flexible clock conditioning capabilities. Each member of the Fusion family contains six CCCs. In the two larger family members, two of these CCCs also include a PLL; the smaller devices support one PLL.

The inputs of the CCC blocks are accessible from the FPGA core or from one of several inputs with dedicated CCC block connections.

The CCC block has the following key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock phase adjustment via programmable and fixed delays from –6.275 ns to +8.75 ns
- Clock skew minimization (PLL)
- Clock frequency synthesis (PLL)
- On-chip analog clocking resources usable as inputs:
  - 100 MHz on-chip RC oscillator
  - Crystal oscillator

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°
- Output duty cycle = 50% ± 1.5%
- Low output jitter. Samples of peak-to-peak period jitter when a single global network is used:
  - 70 ps at 350 MHz
  - 90 ps at 100 MHz
  - 180 ps at 24 MHz
  - Worst case < 2.5% × clock period
- Maximum acquisition time = 150 µs
- Low power consumption of 5 mW

The system application, Level 3, is the larger user application that utilizes one or more applets. Designing at the highest level of abstraction supported by the Fusion technology stack, the application can be easily created in FPGA gates by importing and configuring multiple applets.

In fact, in some cases an entire FPGA system design can be created without any HDL coding.

An optional MCU enables a combination of software and HDL-based design methodologies. The MCU can be on-chip or off-chip as system requirements dictate. System portioning is very flexible, allowing the MCU to reside above the applets or to absorb applets, or applets and backbone, if desired.

The Fusion technology stack enables a very flexible design environment. Users can engage in design across a continuum of abstraction from very low to very high.

Core Architecture

VersaTile

Based upon successful ProASIC3/E logic architecture, Fusion devices provide granularity comparable to gate arrays. The Fusion device core consists of a sea-of-VersaTiles architecture.

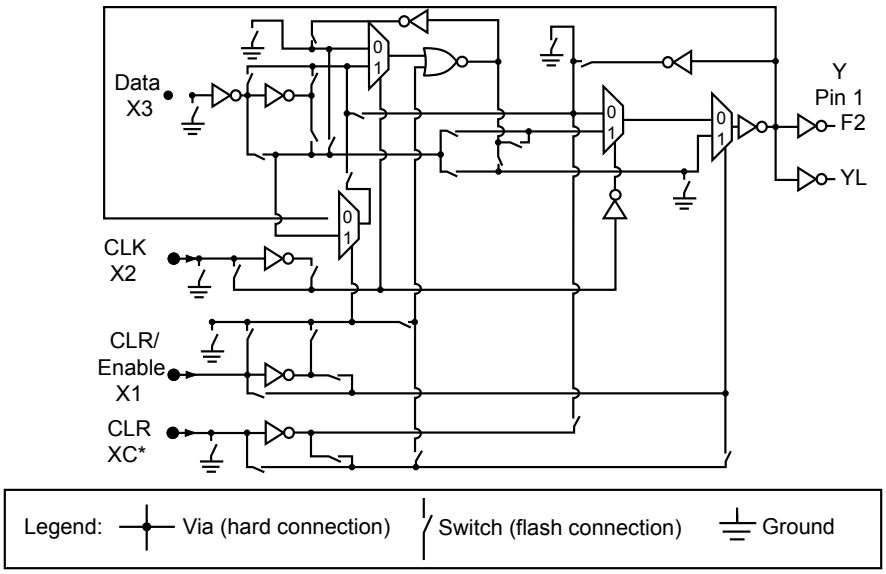
As illustrated in Figure 2-2, there are four inputs in a logic VersaTile cell, and each VersaTile can be configured using the appropriate flash switch connections:

- Any 3-input logic function
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set (on a 4th input)

VersaTiles can flexibly map the logic and sequential gates of a design. The inputs of the VersaTile can be inverted (allowing bubble pushing), and the output of the tile can connect to high-speed, very-long-line routing resources. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy.

When the VersaTile is used as an enable D-flip-flop, the SET/CLR signal is supported by a fourth input, which can only be routed to the core cell over the VersaNet (global) network.

The output of the VersaTile is F2 when the connection is to the ultra-fast local lines, or YL when the connection is to the efficient long-line or very-long-line resources (Figure 2-2).



*Note: *This input can only be connected to the global clock distribution network.*

Figure 2-2 • **Fusion Core VersaTile**

No-Glitch MUX (NGMUX)

Positioned downstream from the PLL/CCC blocks, the NGMUX provides a special switching sequence between two asynchronous clock domains that prevents generating any unwanted narrow clock pulses. The NGMUX is used to switch the source of a global between three different clock sources. Allowable inputs are either two PLL/CCC outputs or a PLL/CCC output and a regular net, as shown in Figure 2-24. The GLMUXCFG[1:0] configuration bits determine the source of the CLK inputs (i.e., internal signal or GLC). These are set by SmartGen during design but can also be changed by dynamically reconfiguring the PLL. The GLMUXSEL[1:0] bits control which clock source is passed through the NGMUX to the global network (GL). See Table 2-13.

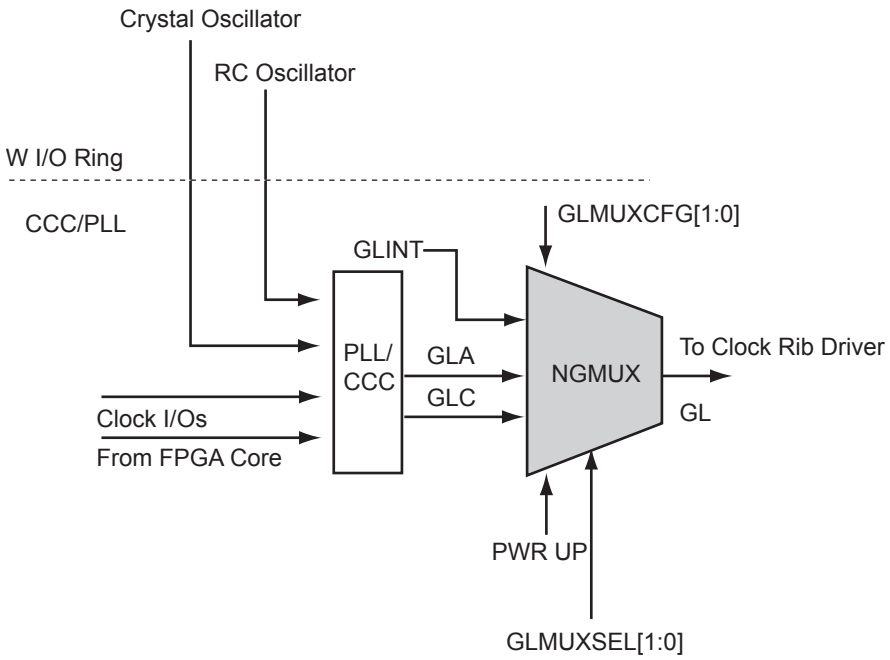


Figure 2-24 • **NGMUX**

Table 2-13 • **NGMUX Configuration and Selection Table**

GLMUXCFG[1:0]	GLMUXSEL[1:0]		Selected Input Signal	MUX Type
00	X	0	GLA	2-to-1 GLMUX
	X	1	GLC	
01	X	0	GLA	2-to-1 GLMUX
	X	1	GLINT	

ESTOP, FSTOP

ESTOP is used to stop the FIFO read counter from further counting once the FIFO is empty (i.e., the EMPTY flag goes High). A High on this signal inhibits the counting.

FSTOP is used to stop the FIFO write counter from further counting once the FIFO is full (i.e., the FULL flag goes High). A High on this signal inhibits the counting.

For more information on these signals, refer to the "ESTOP and FSTOP Usage" section on page 2-70.

FULL, EMPTY

When the FIFO is full and no more data can be written, the FULL flag asserts High. The FULL flag is synchronous to WCLK to inhibit writing immediately upon detection of a full condition and to prevent overflows. Since the write address is compared to a resynchronized (and thus time-delayed) version of the read address, the FULL flag will remain asserted until two WCLK active edges after a read operation eliminates the full condition.

When the FIFO is empty and no more data can be read, the EMPTY flag asserts High. The EMPTY flag is synchronous to RCLK to inhibit reading immediately upon detection of an empty condition and to prevent underflows. Since the read address is compared to a resynchronized (and thus time-delayed) version of the write address, the EMPTY flag will remain asserted until two RCLK active edges after a write operation removes the empty condition.

For more information on these signals, refer to the "FIFO Flag Usage Considerations" section on page 2-70.

AFULL, AEMPTY

These are programmable flags and will be asserted on the threshold specified by AFVAL and AEVAL, respectively.

When the number of words stored in the FIFO reaches the amount specified by AEVAL while reading, the AEMPTY output will go High. Likewise, when the number of words stored in the FIFO reaches the amount specified by AFVAL while writing, the AFULL output will go High.

AFVAL, AEVAL

The AEVAL and AFVAL pins are used to specify the almost-empty and almost-full threshold values, respectively. They are 12-bit signals. For more information on these signals, refer to "FIFO Flag Usage Considerations" section.

ESTOP and FSTOP Usage

The ESTOP pin is used to stop the read counter from counting any further once the FIFO is empty (i.e., the EMPTY flag goes High). Likewise, the FSTOP pin is used to stop the write counter from counting any further once the FIFO is full (i.e., the FULL flag goes High).

The FIFO counters in the Fusion device start the count at 0, reach the maximum depth for the configuration (e.g., 511 for a 512×9 configuration), and then restart at 0. An example application for the ESTOP, where the read counter keeps counting, would be writing to the FIFO once and reading the same content over and over without doing another write.

FIFO Flag Usage Considerations

The AEVAL and AFVAL pins are used to specify the 12-bit AEMPTY and AFULL threshold values, respectively. The FIFO contains separate 12-bit write address (WADDR) and read address (RADDR) counters. WADDR is incremented every time a write operation is performed, and RADDR is incremented every time a read operation is performed. Whenever the difference between WADDR and RADDR is greater than or equal to AFVAL, the AFULL output is asserted. Likewise, whenever the difference between WADDR and RADDR is less than or equal to AEVAL, the AEMPTY output is asserted. To handle different read and write aspect ratios, AFVAL and AEVAL are expressed in terms of total data bits instead of total data words. When users specify AFVAL and AEVAL in terms of read or write words, the SmartGen tool translates them into bit addresses and configures these signals automatically. SmartGen configures the AFULL flag to assert when the write address exceeds the read address by at least a predefined value. In a 2k×8 FIFO, for example, a value of 1,500 for AFVAL means that the AFULL flag will be asserted after a write when the difference between the write address and the read address reaches 1,500 (there have been at least 1500 more writes than reads). It will stay asserted until the difference between the write and read addresses drops below 1,500.

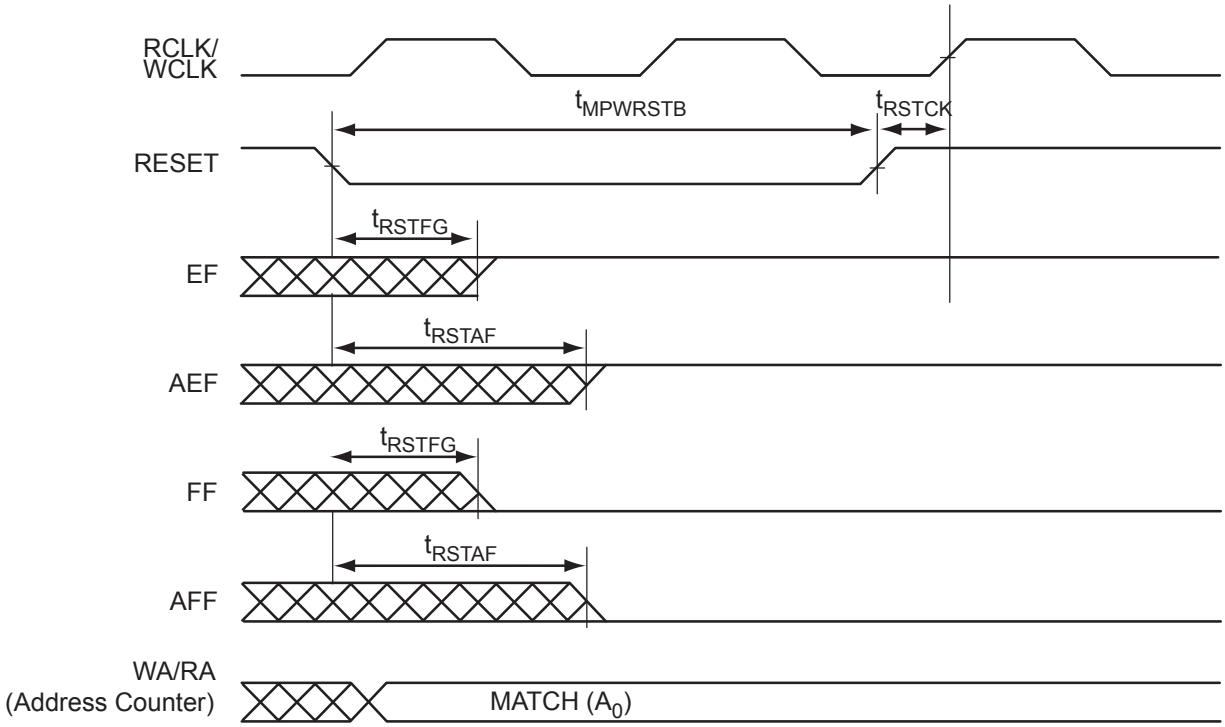


Figure 2-59 • **FIFO Reset**

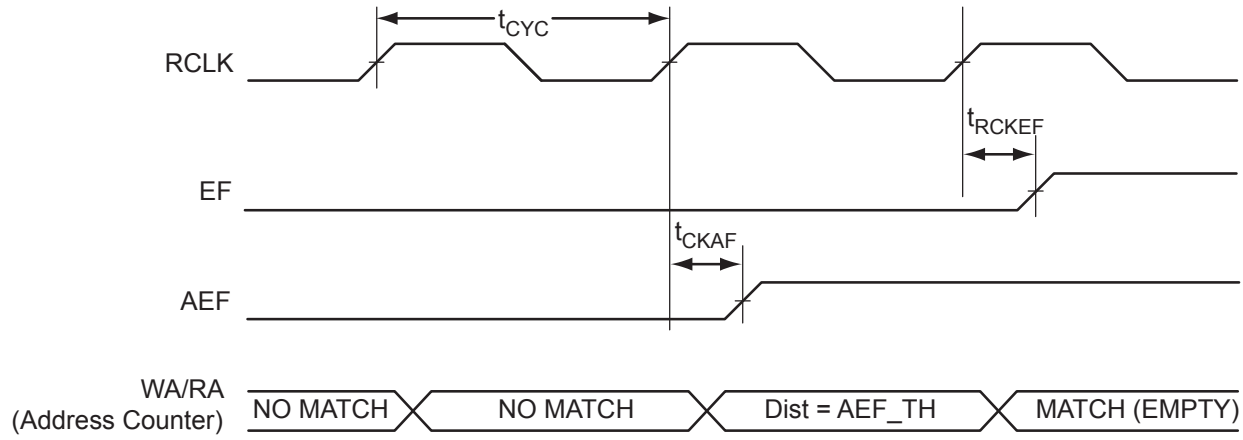


Figure 2-60 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

Channel Input Offset Error

Channel Offset error is measured as the input voltage that causes the transition from zero to a count of one. An Ideal Prescaler will have offset equal to ½ of LSB voltage. Offset error is a positive or negative when the first transition point is higher or lower than ideal. Offset error is expressed in LSB or input voltage.

Total Channel Error

Total Channel Error is defined as the total error measured compared to the ideal value. Total Channel Error is the sum of gain error and offset error combined. Figure 2-68 shows how Total Channel Error is measured.

Total Channel Error is defined as the difference between the actual ADC output and ideal ADC output. In the example shown in Figure 2-68, the Total Channel Error would be a negative number.

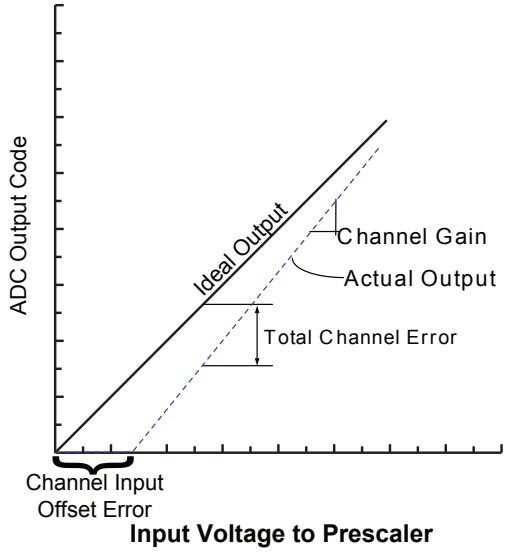


Figure 2-68 • **Total Channel Error Example**

Terminology

Resolution

Resolution defines the smallest temperature change Fusion Temperature Monitor can resolve. For ADC configured as 8-bit mode, each LSB represents 4°C, and 1°C per LSB for 10-bit mode. With 12-bit mode, the Temperature Monitor can still only resolve 1°C due to Temperature Monitor design.

Offset

The Fusion Temperature Monitor has a systematic offset (Table 2-49 on page 2-117), excluding error due to board resistance and ideality factor of the external diode. Microsemi provides an IP block (CalibIP) that is required in order to mitigate the systematic temperature offset. For further details on CalibIP, refer to the "*Temperature*, *Voltage, and Current Calibration in Fusion FPGAs" chapter of the Fusion FPGA Fabric User Guide*.

Table 2-53 • Analog Channel Accuracy: Monitoring Standard Positive Voltages Typical Conditions, T_A = 25°C

Input Voltage (V)	Calibrated Typical Error per Positive Prescaler Setting [1] (%FSR)							Direct ADC [2,3] (%FSR)
	16 V (AT)	16 V (12 V) (AV/AC)	8 V (AV/AC)	4 V (AT)	4 V (AV/AC)	2 V (AV/AC)	1 V (AV/AC)	VAREF = 2.56 V
15	1							
14	1							
12	1	1						
5	2	2	1					
3.3	2	2	1	1	1			
2.5	3	2	1	1	1			1
1.8	4	4	1	1	1	1		1
1.5	5	5	2	2	2	1		1
1.2	7	6	2	2	2	1		1
0.9	9	9	4	3	3	1	1	1

Notes:

1. *Requires enabling Analog Calibration using SmartGen Analog System Builder. For further details, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the* Fusion FPGA Fabric User Guide.
2. *Direct ADC mode using an external VAREF of 2.56V±4.6mV, without Analog Calibration macro.*
3. *For input greater than 2.56 V, the ADC output will saturate. A higher VAREF or prescaler usage is recommended.*

Examples

Calculating Accuracy for an Uncalibrated Analog Channel

Formula

For a given prescaler range, EQ 30 gives the output voltage.

$$Output\ Voltage = (Channel\ Output\ Offset\ in\ V) + (Input\ Voltage \times Channel\ Gain) \quad EQ\ 30$$

where

Channel Output offset in V = Channel Input offset in LSBs x Equivalent voltage per LSB

Channel Gain Factor = 1+ (% Channel Gain / 100)

Example

Input Voltage = 5 V

Chosen Prescaler range = 8 V range

Refer to Table 2-51 on page 2-122.

Max. Output Voltage = (Max Positive input offset) + (Input Voltage x Max Positive Channel Gain)

Max. Positive input offset = (21 LSB) x (8 mV per LSB in 10-bit mode)

Max. Positive input offset = 166 mV

Max. Positive Gain Error = +3%

Max. Positive Channel Gain = 1 + (+3% / 100)

Max. Positive Channel Gain = 1.03

Max. Output Voltage = (166 mV) + (5 V x 1.03)

Max. Output Voltage = **5.316 V**

I/O Software Support

In the Fusion development software, default settings have been defined for the various I/O standards supported. Changes can be made to the default settings via the use of attributes; however, not all I/O attributes are applicable for all I/O standards. Table 2-84 and Table 2-85 list the valid I/O attributes that can be manipulated by the user for each I/O standard.

Single-ended I/O standards in Fusion support up to five different drive strengths.

Table 2-84 • **Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)*	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	3	3	3	3	3	3
LVCMOS 2.5 V	3	3	3	3	3	3
LVCMOS 2.5/5.0 V	3	3	3	3	3	3
LVCMOS 1.8 V	3	3	3	3	3	3
LVCMOS 1.5 V	3	3	3	3	3	3
PCI (3.3 V)			3		3	3
PCI-X (3.3 V)	3		3		3	3
LVDS, BLVDS, M-LVDS			3			3
LVPECL						3

*Note: * This feature does not apply to the standard I/O banks, which are the north I/O banks of AFS090 and AFS250 devices*

Table 2-117 • 2.5 V LVCMOS High Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	8.20	0.04	1.29	0.43	7.24	8.20	2.03	1.91	ns
	–1	0.56	6.98	0.04	1.10	0.36	6.16	6.98	1.73	1.62	ns
	–2	0.49	6.13	0.03	0.96	0.32	5.41	6.13	1.52	1.43	ns
4 mA	Std.	0.66	8.20	0.04	1.29	0.43	7.24	8.20	2.03	1.91	ns
	–1	0.56	6.98	0.04	1.10	0.36	6.16	6.98	1.73	1.62	ns
	–2	0.49	6.13	0.03	0.96	0.32	5.41	6.13	1.52	1.43	ns
6 mA	Std.	0.66	4.77	0.04	1.29	0.43	4.55	4.77	2.38	2.55	ns
	–1	0.56	4.05	0.04	1.10	0.36	3.87	4.05	2.03	2.17	ns
	–2	0.49	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns
8 mA	Std.	0.66	4.77	0.04	1.29	0.43	4.55	4.77	2.38	2.55	ns
	–1	0.56	4.05	0.04	1.10	0.36	3.87	4.05	2.03	2.17	ns
	–2	0.49	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-125 • 1.8 V LVCMOS High Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Standard I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	11.21	0.04	1.20	0.43	8.53	11.21	1.99	1.21	ns
	–1	0.56	9.54	0.04	1.02	0.36	7.26	9.54	1.69	1.03	ns
	–2	0.49	8.37	0.03	0.90	0.32	6.37	8.37	1.49	0.90	ns
4 mA	Std.	0.66	6.34	0.04	1.20	0.43	5.38	6.34	2.41	2.48	ns
	–1	0.56	5.40	0.04	1.02	0.36	4.58	5.40	2.05	2.11	ns
	–2	0.49	4.74	0.03	0.90	0.32	4.02	4.74	1.80	1.85	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Pin Descriptions

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ needs to always be connected on the board to GND. Note: In FG256, FG484, and FG676 packages, GNDQ and GND pins are connected within the package and are labeled as GND pins in the respective package pin assignment tables.

ADCGNDREF **Analog Reference Ground**

Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.

GNDA **Ground (analog)**

Quiet ground supply voltage to the Analog Block of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation.

GNDAQ **Ground (analog quiet)**

Quiet ground supply voltage to the analog I/O of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation. Note: In FG256, FG484, and FG676 packages, GNDAQ and GNDA pins are connected within the package and are labeled as GNDA pins in the respective package pin assignment tables.

GNDNVM **Flash Memory Ground**

Ground supply used by the Fusion device's flash memory block module(s).

GNDOSC **Oscillator Ground**

Ground supply for both integrated RC oscillator and crystal oscillator circuit.

VCC15A **Analog Power Supply (1.5 V)**

1.5 V clean analog power supply input for use by the 1.5 V portion of the analog circuitry.

VCC33A **Analog Power Supply (3.3 V)**

3.3 V clean analog power supply input for use by the 3.3 V portion of the analog circuitry.

VCC33N **Negative 3.3 V Output**

This is the –3.3 V output from the voltage converter. A 2.2 µF capacitor must be connected from this pin to ground.

VCC33PMP **Analog Power Supply (3.3 V)**

3.3 V clean analog power supply input for use by the analog charge pump. To avoid high current draw, VCC33PMP should be powered up simultaneously with or after VCC33A.

VCCNVM **Flash Memory Block Power Supply (1.5 V)**

1.5 V power supply input used by the Fusion device's flash memory block module(s). To avoid high current draw, VCC should be powered up before or simultaneously with VCCNVM.

VCCOSC **Oscillator Power Supply (3.3 V)**

Power supply for both integrated RC oscillator and crystal oscillator circuit. The internal 100 MHz oscillator, powered by the VCCOSC pin, is needed for device programming, operation of the VDDN33 pump, and eNVM operation. VCCOSC is off only when VCCA is off. VCCOSC must be powered whenever the Fusion device needs to function.

XTAL2 Crystal Oscillator Circuit Input

Input to crystal oscillator circuit. Pin for connecting external crystal, ceramic resonator, RC network, or external clock input. When using an external crystal or ceramic oscillator, external capacitors are also recommended (Please refer to the crystal oscillator manufacturer for proper capacitor value).

If using external RC network or clock input, XTAL1 should be used and XTAL2 left unconnected. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.

Security

Fusion devices have a built-in 128-bit AES decryption core. The decryption core facilitates highly secure, in-system programming of the FPGA core array fabric and the FlashROM. The FlashROM and the FPGA core fabric can be programmed independently from each other, allowing the FlashROM to be updated without the need for change to the FPGA core fabric. The AES master key is stored in on-chip nonvolatile memory (flash). The AES master key can be preloaded into parts in a security-protected programming environment (such as the Microsemi in-house programming center), and then "blank" parts can be shipped to an untrusted programming or manufacturing center for final personalization with an AES-encrypted bitstream. Late stage product changes or personalization can be implemented easily and with high level security by simply sending a STAPL file with AES-encrypted data. Highly secure remote field updates over public networks (such as the Internet) are possible by sending and programming a STAPL file with AES-encrypted data. For more information, refer to the *Fusion Security* application note.

128-Bit AES Decryption

The 128-bit AES standard (FIPS-197) block cipher is the National Institute of Standards and Technology (NIST) replacement for DES (Data Encryption Standard FIPS46-2). AES has been designed to protect sensitive government information well into the 21st century. It replaces the aging DES, which NIST adopted in 1977 as a Federal Information Processing Standard used by federal agencies to protect sensitive, unclassified information. The 128-bit AES standard has 3.4×10^{38} possible 128-bit key variants, and it has been estimated that it would take 1,000 trillion years to crack 128-bit AES cipher text using exhaustive techniques. Keys are stored (protected with security) in Fusion devices in nonvolatile flash memory. All programming files sent to the device can be authenticated by the part prior to programming to ensure that bad programming data is not loaded into the part that may possibly damage it. All programming verification is performed on-chip, ensuring that the contents of Fusion devices remain as secure as possible.

AES decryption can also be used on the 1,024-bit FlashROM to allow for remote updates of the FlashROM contents. This allows for easy support of subscription model products and protects them with measures designed to provide the highest level of security available. See the application note *Fusion Security* for more details.

AES for Flash Memory

AES decryption can also be used on the flash memory blocks. This provides the best available security during update of the flash memory blocks. During runtime, the encrypted data can be clocked in via the JTAG interface. The data can be passed through the internal AES decryption engine, and the decrypted data can then be stored in the flash memory block.

Programming

Programming can be performed using various programming tools, such as Silicon Sculptor II (BP Micro Systems) or FlashPro3 (Microsemi).

The user can generate STP programming files from the Designer software and can use these files to program a device.

Fusion devices can be programmed in-system. During programming, VCCOSC is needed in order to power the internal 100 MHz oscillator. This oscillator is used as a source for the 20 MHz oscillator that is used to drive the charge pump for programming.

ISP

Fusion devices support IEEE 1532 ISP via JTAG and require a single VPUMP voltage of 3.3 V during programming. In addition, programming via a microcontroller in a target system can be achieved. Refer to the standard or the "In-System Programming (ISP) of Microsemi's Low Power Flash Devices Using FlashPro4/3/3X" chapter of the *Fusion FPGA Fabric User's Guide* for more details.

JTAG IEEE 1532

Programming with IEEE 1532

Fusion devices support the JTAG-based IEEE1532 standard for ISP. As part of this support, when a Fusion device is in an unprogrammed state, all user I/O pins are disabled. This is achieved by keeping the global IO_EN signal deactivated, which also has the effect of disabling the input buffers. Consequently, the SAMPLE instruction will have no effect while the Fusion device is in this unprogrammed state—different behavior from that of the ProASIC$^{PLUS®}$ device family. This is done because SAMPLE is defined in the IEEE1532 specification as a noninvasive instruction. If the input buffers were to be enabled by SAMPLE temporarily turning on the I/Os, then it would not truly be a noninvasive instruction. Refer to the standard or the "In-System Programming (ISP) of Microsemi's Low Power Flash Devices Using FlashPro4/3/3X" chapter of the *Fusion FPGA Fabric User's Guide* for more details.

Boundary Scan

Fusion devices are compatible with IEEE Standard 1149.1, which defines a hardware architecture and the set of mechanisms for boundary scan testing. The basic Fusion boundary scan logic circuit is composed of the test access port (TAP) controller, test data registers, and instruction register (Figure 2-146 on page 2-230). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD, and BYPASS) and the optional IDCODE instruction (Table 2-185 on page 2-230).

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI, TDO (test data input and output), TMS (test mode selector), and TRST (test reset input). TMS, TDI, and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary scan test usage. Refer to the "JTAG Pins" section on page 2-226 for pull-up/-down recommendations for TDO and TCK pins. The TAP controller is a 4-bit state machine (16 states) that operates as shown in Figure 2-146 on page 2-230. The 1s and 0s represent the values that must be present on TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

***Table 2-184* • TRST and TCK Pull-Down Recommendations**

VJTAG	Tie-Off Resistance*
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

*Note: *Equivalent parallel resistance if more than one device is on JTAG chain.*

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain High for five TCK cycles. The TRST pin can also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

Fusion devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (LSB, ID number, part number, and version). The boundary scan register observes and controls the state of each I/O pin. Each I/O cell has three boundary scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin.

The serial pins are used to serially connect all the boundary scan register cells in a device into a boundary scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are

Table 3-11 • **AFS090 Quiescent Supply Current Characteristics**

Parameter	Description	Conditions	Temp.	Min	Typ	Max	Unit
ICC[1]	1.5 V quiescent current	Operational standby[4], VCC = 1.575 V	T_J = 25°C		5	7.5	mA
			T_J = 85°C		6.5	20	mA
			T_J = 100°C		14	48	mA
		Standby mode[5] or Sleep mode[6], V_{CC} = 0 V			0	0	µA
ICC33[2]	3.3 V analog supplies current	Operational standby[4], VCC33 = 3.63 V	T_J = 25°C		9.8	12	mA
			T_J = 85°C		9.8	12	mA
			T_J = 100°C		10.7	15	mA
		Operational standby, only Analog Quad and –3.3 V output ON, VCC33 = 3.63 V	T_J = 25°C		0.30	2	mA
			T_J = 85°C		0.30	2	mA
			T_J = 100°C		0.45	2	mA
		Standby mode[5], VCC33 = 3.63 V	T_J = 25°C		2.9	2.9	mA
			T_J = 85°C		2.9	3.0	mA
			T_J = 100°C		3.5	6	mA
		Sleep mode[6], VCC33 = 3.63 V	T_J = 25°C		17	18	µA
			T_J = 85°C		18	20	µA
			T_J = 100°C		24	25	µA
ICCI[3]	I/O quiescent current	Operational standby[6], VCCIx = 3.63 V	T_J = 25°C		260	437	µA
			T_J = 85°C		260	437	µA
			T_J = 100°C		260	437	µA
IJTAG	JTAG I/O quiescent current	Operational standby[4], VJTAG = 3.63 V	T_J = 25°C		80	100	µA
			T_J = 85°C		80	100	µA
			T_J = 100°C		80	100	µA
		Standby mode[5] or Sleep mode[6], VJTAG = 0 V			0	0	µA
IPP	Programming supply current	Non-programming mode, VPUMP = 3.63 V	T_J = 25°C		37	80	µA
			T_J = 85°C		37	80	µA
			T_J = 100°C		80	100	µA
		Standby mode[5] or Sleep mode[6], VPUMP = 0 V			0	0	µA

Notes:

1. *ICC is the 1.5 V power supplies, ICC, ICCPLL, ICC15A, ICCNVM.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, and ICCI2.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPUMP = 0 V.*

***Table 3-11* • AFS090 Quiescent Supply Current Characteristics (continued)**

Parameter	Description	Conditions	Temp.	Min	Typ	Max	Unit
ICCNVM	Embedded NVM current	Reset asserted, VCCNVM = 1.575 V	T_J = 25°C		10	40	µA
			T_J = 85°C		14	40	µA
			T_J = 100°C		14	40	µA
ICCPLL	1.5 V PLL quiescent current	Operational standby, VCCPLL = 1.575 V	T_J = 25°C		65	100	µA
			T_J = 85°C		65	100	µA
			T_J = 100°C		65	100	µA

Notes:

1. *ICC is the 1.5 V power supplies, ICC, ICCPLL, ICC15A, ICCNVM.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, and ICCI2.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPUMP = 0 V.*

Example of Power Calculation

This example considers a shift register with 5,000 storage tiles, including a counter and memory that stores analog information. The shift register is clocked at 50 MHz and stores and reads information from a RAM.

The device used is a commercial AFS600 device operating in typical conditions.

The calculation below uses the power calculation methodology previously presented and shows how to determine the dynamic and static power consumption of resources used in the application.

Also included in the example is the calculation of power consumption in operating, standby, and sleep modes to illustrate the benefit of power-saving modes.

Global Clock Contribution—P_{CLOCK}

F_{CLK} = 50 MHz

Number of sequential VersaTiles: $N_{S\text{-}CELL}$ = 5,000

Estimated number of Spines: N_{SPINES} = 5

Estimated number of Rows: N_{ROW} = 313

Operating Mode

$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$

$P_{CLOCK} = (0.0128 + 5 * 0.0019 + 313 * 0.00081 + 5{,}000 * 0.00011) * 50$

P_{CLOCK} = 41.28 mW

Standby Mode and Sleep Mode

P_{CLOCK} = 0 W

Logic—Sequential Cells, Combinational Cells, and Routing Net Contributions—$P_{S\text{-}CELL}$, $P_{C\text{-}CELL}$, and P_{NET}

F_{CLK} = 50 MHz

Number of sequential VersaTiles: $N_{S\text{-}CELL}$ = 5,000

Number of combinatorial VersaTiles: $N_{C\text{-}CELL}$ = 6,000

Estimated toggle rate of VersaTile outputs: α_1 = 0.1 (10%)

Operating Mode

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + (\alpha_1 / 2) * PAC6) * F_{CLK}$

$P_{S\text{-}CELL} = 5{,}000 * (0.00007 + (0.1 / 2) * 0.00029) * 50$

$P_{S\text{-}CELL}$ = 21.13 mW

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * (\alpha_1 / 2) * PAC7 * F_{CLK}$

$P_{C\text{-}CELL} = 6{,}000 * (0.1 / 2) * 0.00029 * 50$

$P_{C\text{-}CELL}$ = 4.35 mW

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * (\alpha_1 / 2) * PAC8 * F_{CLK}$

$P_{NET} = (5{,}000 + 6{,}000) * (0.1 / 2) * 0.0007 * 50$

P_{NET} = 19.25 mW

$P_{LOGIC} = P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET}$

P_{LOGIC} = 21.13 mW + 4.35 mW + 19.25 mW

P_{LOGIC} = 44.73 mW

Standby Mode and Sleep Mode

Revision	Changes	Page
Advance v1.5 (continued)	This bullet was added to the "Integrated A/D Converter (ADC) and Analog I/O" section: ADC Accuracy is Better than 1%	I
	In the "Integrated Analog Blocks and Analog I/Os" section, ±4 LSB was changed to 0.72. The following sentence was deleted: The input range for voltage signals is from –12 V to +12 V with full-scale output values from 0.125 V to 16 V. In addition, 2°C was changed to 3°C: "One analog input in each quad can be connected to an external temperature monitor diode and achieves detection accuracy of ±3ºC." The following sentence was deleted: The input range for voltage signals is from –12 V to +12 V with full-scale output values from 0.125 V to 16 V.	1-4
	The title of the datasheet changed from Actel Programmable System Chips to Actel Fusion Mixed Signal FPGAs. In addition, all instances of programmable system chip were changed to mixed signal FPGA.	N/A
Advance v1.4 (July 2008)	In Table 3-8 · Quiescent Supply Current Characteristics (IDDQ)1, footnote references were updated for I_{DC2} and I_{DC3}. Footnote 3 and 4 were updated and footnote 5 is new.	3-11
Advance v1.3 (July 2008)	The "ADC Description" section was significantly updated. Please review carefully.	2-102
Advance v1.2 (May 2008)	Table 2-25 • Flash Memory Block Timing was significantly updated.	2-55
	The "V_{AREF} Analog Reference Voltage" pin description section was significantly update. Please review it carefully.	2-226
	Table 2-45 • ADC Interface Timing was significantly updated.	2-110
	Table 2-56 • Direct Analog Input Switch Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3) was significantly updated.	2-131
	The following sentence was deleted from the "Voltage Monitor" section: The Analog Quad inputs are tolerant up to 12 V + 10%.	2-86
	The "180-Pin QFN" figure was updated. D1 to D4 are new and the figure was changed to bottom view. The note below the figure is new.	3-3
Advance v1.1 (May 2008)	The following text was incorrect and therefore deleted: **VCC33A** **Analog Power Filter** Analog power pin for the analog power supply low-pass filter. An external 100 pF capacitor should be connected between this pin and ground. There is still a description of V_{CC33A} on page 2-224.	2-204

Revision	Changes	Page
Advance 1.0 (continued)	In Table 2-47 • ADC Characteristics in Direct Input Mode, the commercial conditions were updated and note 2 is new.	2-121
	The $V_{CC33ACAP}$ signal name was changed to "XTAL1 Crystal Oscillator Circuit Input".	2-228
	Table 2-48 • Uncalibrated Analog Channel Accuracy* is new.	2-123
	Table 2-49 • Calibrated Analog Channel Accuracy [1,2,3] is new.	2-124
	Table 2-50 • Analog Channel Accuracy: Monitoring Standard Positive Voltages is new.	2-125
	In Table 2-57 • Voltage Polarity Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)*, the following I/O Bank names were changed: Hot-Swap changed to Standard LVDS changed to Advanced	2-131
	In Table 2-58 • Prescaler Op Amp Power-Down Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3), the following I/O Bank names were changed: Hot-Swap changed to Standard LVDS changed to Advanced	2-132
	In the title of Table 2-64 • I/O Standards Supported by Bank Type, LVDS I/O was changed to Advanced I/O.	2-134
	The title was changed from "Fusion Standard, LVDS, and Standard plus Hot-Swap I/O" to Table 2-68 • Fusion Standard and Advanced I/O Features. In addition, the table headings were all updated. The heading used to be Standard and LVDS I/O and was changed to Advanced I/O. Standard Hot-Swap was changed to just Standard.	2-136
	This sentence was deleted from the "Slew Rate Control and Drive Strength" section: The Standard hot-swap I/Os do not support slew rate control. In addition, these references were changed: • From: Fusion hot-swap I/O (Table 2-69 on page 2-122) To: Fusion Standard I/O • From: Fusion LVDS I/O (Table 2-70 on page 2-122) To: Fusion Advanced I/O	2-152
	The "Cold-Sparing Support" section was significantly updated.	2-143
	In the title of Table 2-75 • Fusion Standard I/O Standards—OUT_DRIVE Settings, Hot-Swap was changed to Standard.	2-153
	In the title of Table 2-76 • Fusion Advanced I/O Standards—SLEW and OUT_DRIVE Settings, LVDS was changed to Advanced.	2-153
	In the title of Table 2-81 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications, LVDS was changed to Advanced.	2-157
	In Figure 2-111 • Naming Conventions of Fusion Devices with Three Digital I/O Banks and Figure 2-112 • Naming Conventions of Fusion Devices with Four I/O Banks the following names were changed: Hot-Swap changed to Standard LVDS changed to Advanced	2-160
	The Figure 2-113 • Timing Model was updated.	2-161
	In the notes for Table 2-86 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions, T_J was changed to T_A.	2-166

Revision	Changes	Page
Advance v0.8 (continued)	The voltage range in the "VPUMP Programming Supply Voltage" section was updated. The parenthetical reference to "pulled up" was removed from the statement, "VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and 3.6 V."	2-225
	The "ATRTNx Temperature Monitor Return" section was updated with information about grounding and floating the pin.	2-226
	The following text was deleted from the "VREF I/O Voltage Reference" section: (all digital I/O).	2-225
	The "NCAP Negative Capacitor" section and "PCAP Positive Capacitor" section were updated to include information about the type of capacitor that is required to connect the two.	2-228
	1 µF was changed to 100 pF in the "XTAL1 Crystal Oscillator Circuit Input".	2-228
	The "Programming" section was updated to include information about V_{CCOSC}.	2-229
	The VMV pins have now been tied internally with the V_{CCI} pins.	N/A
	The AFS090"108-Pin QFN" table was updated.	3-2
	The AFS090 and AFS250 devices were updated in the "108-Pin QFN" table.	3-2
	The AFS250 device was updated in the "208-Pin PQFP" table.	3-8
	The AFS600 device was updated in the "208-Pin PQFP" table.	3-8
	The AFS090, AFS250, AFS600, and AFS1500 devices were updated in the "256-Pin FBGA" table.	3-12
	The AFS600 and AFS1500 devices were updated in the "484-Pin FBGA" table.	3-20
Advance v0.7 (January 2007)	The AFS600 device was updated in the "676-Pin FBGA" table.	3-28
	The AFS1500 digital I/O count was updated in the "Fusion Family" table.	I
	The AFS1500 digital I/O count was updated in the "Package I/Os: Single-/Double-Ended (Analog)" table.	II
Advance v0.6 (October 2006)	The second paragraph of the "PLL Macro" section was updated to include information about POWERDOWN.	2-30
	The description for bit 0 was updated in Table 2-17 · RTC Control/Status Register.	2-38
	3.9 was changed to 7.8 in the "Crystal Oscillator (Xtal Osc)" section.	2-40.
	All function descriptions in Table 2-18 · Signals for VRPSM Macro.	2-42
	In Table 2-19 • Flash Memory Block Pin Names, the RD[31:0] description was updated.	2-43
	The "RESET" section was updated.	2-61
	The "RESET" section was updated.	2-64
	Table 2-35 • FIFO was updated.	2-79
	The VAREF function description was updated in Table 2-36 • Analog Block Pin Description.	2-82
	The "Voltage Monitor" section was updated to include information about low power mode and sleep mode.	2-86
	The text in the "Current Monitor" section was changed from 2 mV to 1 mV.	2-90
	The "Gate Driver" section was updated to include information about forcing 1 V on the drain.	2-94