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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	- ·
Total RAM Bits	110592
Number of I/O	119
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs600-1fgg256i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

The on-chip crystal and RC oscillators work in conjunction with the integrated phase-locked loops (PLLs) to provide clocking support to the FPGA array and on-chip resources. In addition to supporting typical RTC uses such as watchdog timer, the Fusion RTC can control the on-chip voltage regulator to power down the device (FPGA fabric, flash memory block, and ADC), enabling a low power standby mode.

The Fusion family offers revolutionary features, never before available in an FPGA. The nonvolatile flash technology gives the Fusion solution the advantage of being a highly secure, low power, single-chip solution that is Instant On. Fusion is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, high performance, and ease of use. Flashbased Fusion devices are Instant On and do not need to be loaded from an external boot PROM.

On-board security mechanisms prevent access to the programming information and enable remote updates of the FPGA logic that are protected with high level security. Designers can perform remote insystem reprogramming to support future design iterations and field upgrades, with confidence that valuable IP is highly unlikely to be compromised or copied. ISP can be performed using the

industry-standard AES algorithm with MAC data authentication on the device. The Fusion family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the Fusion family a cost-effective ASIC replacement solution for applications in the consumer, networking and communications, computing, and avionics markets.

Security

As the nonvolatile, flash-based Fusion family requires no boot PROM, there is no vulnerable external bitstream. Fusion devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

Fusion devices utilize a 128-bit flash-based key lock and a separate AES key to provide the highest level of protection in the FPGA industry for programmed IP and configuration data. The FlashROM data in Fusion devices can also be encrypted prior to loading. Additionally, the flash memory blocks can be programmed during runtime using the industry-leading AES-128 block cipher encryption standard (FIPS Publication 192). The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the DES standard, which was adopted in 1977. Fusion devices have a

built-in AES decryption engine and a flash-based AES key that make Fusion devices the most comprehensive programmable logic device security solution available today. Fusion devices with

AES-based security provide a high level of protection for remote field updates over public networks, such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. As an additional security measure, the FPGA configuration data of a programmed Fusion device cannot be read back, although secure design verification is possible. During design, the user controls and defines both internal and external access to the flash memory blocks.

Security, built into the FPGA fabric, is an inherent component of the Fusion family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. Fusion with FlashLock and AES security is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with

industry-standard security, making remote ISP possible. A Fusion device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based Fusion FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Global Buffers with No Programmable Delays

The CLKBUF and CLKBUF_LVPECL/LVDS macros are composite macros that include an I/O macro driving a global buffer, hardwired together (Figure 2-20).

The CLKINT macro provides a global buffer function driven by the FPGA core.

The CLKBUF, CLKBUF_LVPECL/LVDS, and CLKINT macros are pass-through clock sources and do not use the PLL or provide any programmable delay functionality.

Many specific CLKBUF macros support the wide variety of single-ended and differential I/O standards supported by Fusion devices. The available CLKBUF macros are described in the *IGLOO*, *ProASIC3*, *SmartFusion and Fusion Macro Library Guide*.

Clock Source	Clock Conditioning	Output	
			GLA
CLKBUF_LVDS/LVPECL Macro CLKBUF Macro	CLKINT Macro		or
		None	GLB
			or
			GLC

Figure 2-20 • Global Buffers with No Programmable Delay

Global Buffers with Programmable Delay

The CLKDLY macro is a pass-through clock source that does not use the PLL, but provides the ability to delay the clock input using a programmable delay (Figure 2-21 on page 2-25). The CLKDLY macro takes the selected clock input and adds a user-defined delay element. This macro generates an output clock phase shift from the input clock.

The CLKDLY macro can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

Many specific INBUF macros support the wide variety of single-ended and differential I/O standards supported by the Fusion family. The available INBUF macros are described in the *IGLOO*, *ProASIC3*, *SmartFusion and Fusion Macro Library Guide*.

The CLKDLY macro can be driven directly from the FPGA core.

The CLKDLY macro can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

The visual CLKDLY configuration in the SmartGen part of the Libero SoC and Designer tools allows the user to select the desired amount of delay and configures the delay elements appropriately. SmartGen also allows the user to select the input clock source. SmartGen will automatically instantiate the special macro, PLLINT, when needed.

CCC Physical Implementation

The CCC circuit is composed of the following (Figure 2-23):

- PLL core
- · 3 phase selectors
- 6 programmable delays and 1 fixed delay
- 5 programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 2-23 because they are automatically configured based on the user's required frequencies)
- 1 dynamic shift register that provides CCC dynamic reconfiguration capability (not shown)

CCC Programming

The CCC block is fully configurable. It is configured via static flash configuration bits in the array, set by the user in the programming bitstream, or configured through an asynchronous dedicated shift register, dynamically accessible from inside the Fusion device. The dedicated shift register permits changes of parameters such as PLL divide ratios and delays during device operation. This latter mode allows the user to dynamically reconfigure the PLL without the need for core programming. The register file is accessed through a simple serial interface.



Note: Clock divider and multiplier blocks are not shown in this figure or in SmartGen. They are automatically configured based on the user's required frequencies.

Figure 2-23 • PLL Block

Modes of Operation

Standby Mode

Standby mode allows periodic power-up and power-down of the FPGA fabric. In standby mode, the real-time counter and crystal block are ON. The FPGA is not powered by disabling the 1.5 V voltage regulator. The 1.5 V voltage regulator can be enabled when the preset count is matched. Refer to the "Real-Time Counter (part of AB macro)" section for details. To enter standby mode, the RTC must be first configured and enabled. Then VRPSM is shut off by deasserting the VRPU signal. The 1.5 V voltage regulator is then disabled, and shuts off the 1.5 V output.

Sleep Mode

In sleep mode, the real-time counter and crystal blocks are OFF. The 1.5 V voltage regulator inside the VRPSM can only be enabled by the PUB or TRST pin. Refer to the "Voltage Regulator and Power System Monitor (VRPSM)" section on page 2-36 for details on power-up and power-down of the 1.5 V voltage regulator.

Standby and Sleep Mode Circuit Implementation

For extra power savings, VJTAG and VPUMP should be at the same voltage as VCC, floated or ground, during standby and sleep modes. Note that when VJTAG is not powered, the 1.5 V voltage regulator cannot be enabled through TRST.

VPUMP and VJTAG can be controlled through an external switch. Microsemi recommends ADG839, ADG849, or ADG841 as possible switches. Figure 2-28 shows the implementation for controlling VPUMP. The IN signal of the switch can be connected to PTBASE of the Fusion device. VJTAG can be controlled in same manner.



Figure 2-28 • Implementation to Control VPUMP



Real-Time Counter (part of AB macro)

The RTC is a 40-bit loadable counter and used as the primary timekeeping element (Figure 2-29). The clock source, RTCCLK, must come from the CLKOUT signal of the crystal oscillator. The RTC can be configured to reset itself when a count value reaches the match value set in the Match Register.

The RTC is part of the Analog Block (AB) macro. The RTC is configured by the analog configuration MUX (ACM). Each address contains one byte of data. The circuitry in the RTC is powered by VCC33A, so the RTC can be used in standby mode when the 1.5 V supply is not present.



Figure 2-29 • RTC Block Diagram

Signal Name	Width	Direction	Function								
RTCCLK	1	In	Must come from CLKOUT of XTLOSC.								
RTCXTLMODE[1:0]	2	Out	Controlled by xt_mode in CTRL_STAT. Signal must connect to the RTC_MODE signal in XTLOSC, as shown in Figure 2-27.								
RTCXTLSEL	1	Out	Controlled by xtal_en from CTRL_STAT register. Signal must connect RTC_MODE signal in XTLOSC in Figure 2-27.								
RTCMATCH	1	Out	Match signal for FPGA								
			0 – Counter value does not equal the Match Register value.								
			1 – Counter value equals the Match Register value.								
RTCPSMMATCH	1	Out	Same signal as RTCMATCH. Signal must connect to RTCPSMMATCH in VRPSM, as shown in Figure 2-27.								

The 40-bit counter can be preloaded with an initial value as a starting point by the Counter Register. The count from the 40-bit counter can be read through the same set of address space. The count comes from a Read-Hold Register to avoid data changing during read. When the counter value equals the Match Register value, all Match Bits Register values will be 0xFFFFFFFFF. The RTCMATCH and RTCPSMMATCH signals will assert. The 40-bit counter can be configured to automatically reset to 0x000000000 when the counter value equals the Match Register value. The automatic reset does not apply if the Match Register value is 0x000000000. The RTCCLK has a prescaler to divide the clock by 128 before it is used for the 40-bit counter. Below is an example of how to calculate the OFF time.

Flash Memory Block Pin Names

Table 2-19 • Flash Memory Block Pin Names

Interface Name	Width	Direction	Description
ADDR[17:0]	18	In	Byte offset into the FB. Byte-based address.
AUXBLOCK	1	In	When asserted, the page addressed is used to access the auxiliary block within that page.
BUSY	1	Out	When asserted, indicates that the FB is performing an operation.
CLK	1	In	User interface clock. All operations and status are synchronous to the rising edge of this clock.
DATAWIDTH[1:0]	2	In	Data width 00 = 1 byte in RD/WD[7:0] 01 = 2 bytes in RD/WD[15:0] 1x = 4 bytes in RD/WD[31:0]
DISCARDPAGE	1	In	When asserted, the contents of the Page Buffer are discarded so that a new page write can be started.
ERASEPAGE	1	In	When asserted, the address page is to be programmed with all zeros. ERASEPAGE must transition synchronously with the rising edge of CLK.
LOCKREQUEST	1	In	When asserted, indicates to the JTAG controller that the FPGA interface is accessing the FB.
OVERWRITEPAGE	1	In	When asserted, the page addressed is overwritten with the contents of the Page Buffer if the page is writable.
OVERWRITEPROTECT	1	In	When asserted, all program operations will set the overwrite protect bit of the page being programmed.
PAGESTATUS	1	In	When asserted with REN, initiates a read page status operation.
PAGELOSSPROTECT	1	In	When asserted, a modified Page Buffer must be programmed or discarded before accessing a new page.
PIPE	1	In	Adds a pipeline stage to the output for operation above 50 MHz.
PROGRAM	1	In	When asserted, writes the contents of the Page Buffer into the FB page addressed.
RD[31:0]	32	Out	Read data; data will be valid from the first non-busy cycle (BUSY = 0) after REN has been asserted.
READNEXT	1	In	When asserted with REN, initiates a read-next operation.
REN	1	In	When asserted, initiates a read operation.
RESET	1	In	When asserted, resets the state of the FB (active low).
SPAREPAGE	1	In	When asserted, the sector addressed is used to access the spare page within that sector.

ESTOP, FSTOP

ESTOP is used to stop the FIFO read counter from further counting once the FIFO is empty (i.e., the EMPTY flag goes High). A High on this signal inhibits the counting.

FSTOP is used to stop the FIFO write counter from further counting once the FIFO is full (i.e., the FULL flag goes High). A High on this signal inhibits the counting.

For more information on these signals, refer to the "ESTOP and FSTOP Usage" section on page 2-70.

FULL, EMPTY

When the FIFO is full and no more data can be written, the FULL flag asserts High. The FULL flag is synchronous to WCLK to inhibit writing immediately upon detection of a full condition and to prevent overflows. Since the write address is compared to a resynchronized (and thus time-delayed) version of the read address, the FULL flag will remain asserted until two WCLK active edges after a read operation eliminates the full condition.

When the FIFO is empty and no more data can be read, the EMPTY flag asserts High. The EMPTY flag is synchronous to RCLK to inhibit reading immediately upon detection of an empty condition and to prevent underflows. Since the read address is compared to a resynchronized (and thus time-delayed) version of the write address, the EMPTY flag will remain asserted until two RCLK active edges after a write operation removes the empty condition.

For more information on these signals, refer to the "FIFO Flag Usage Considerations" section on page 2-70.

AFULL, AEMPTY

These are programmable flags and will be asserted on the threshold specified by AFVAL and AEVAL, respectively.

When the number of words stored in the FIFO reaches the amount specified by AEVAL while reading, the AEMPTY output will go High. Likewise, when the number of words stored in the FIFO reaches the amount specified by AFVAL while writing, the AFULL output will go High.

AFVAL, AEVAL

The AEVAL and AFVAL pins are used to specify the almost-empty and almost-full threshold values, respectively. They are 12-bit signals. For more information on these signals, refer to "FIFO Flag Usage Considerations" section.

ESTOP and FSTOP Usage

The ESTOP pin is used to stop the read counter from counting any further once the FIFO is empty (i.e., the EMPTY flag goes High). Likewise, the FSTOP pin is used to stop the write counter from counting any further once the FIFO is full (i.e., the FULL flag goes High).

The FIFO counters in the Fusion device start the count at 0, reach the maximum depth for the configuration (e.g., 511 for a 512×9 configuration), and then restart at 0. An example application for the ESTOP, where the read counter keeps counting, would be writing to the FIFO once and reading the same content over and over without doing another write.

FIFO Flag Usage Considerations

The AEVAL and AFVAL pins are used to specify the 12-bit AEMPTY and AFULL threshold values, respectively. The FIFO contains separate 12-bit write address (WADDR) and read address (RADDR) counters. WADDR is incremented every time a write operation is performed, and RADDR is incremented every time a read operation is performed. Whenever the difference between WADDR and RADDR is greater than or equal to AFVAL, the AFULL output is asserted. Likewise, whenever the difference between WADDR and RADDR is less than or equal to AEVAL, the AEMPTY output is asserted. To handle different read and write aspect ratios, AFVAL and AEVAL are expressed in terms of total data bits instead of total data words. When users specify AFVAL and AEVAL in terms of read or write words, the SmartGen tool translates them into bit addresses and configures these signals automatically. SmartGen configures the AFULL flag to assert when the write address exceeds the read address by at least a predefined value. In a 2k×8 FIFO, for example, a value of 1,500 for AFVAL means that the AFULL flag will be asserted after a write when the difference between the write address and the read address reaches 1,500 (there have been at least 1500 more writes than reads). It will stay asserted until the difference between the write and read addresses drops below 1,500.

Analog Block

With the Fusion family, Microsemi has introduced the world's first mixed-mode FPGA solution. Supporting a robust analog peripheral mix, Fusion devices will support a wide variety of applications. It is this Analog Block that separates Fusion from all other FPGA solutions on the market today.

By combining both flash and high-speed CMOS processes in a single chip, these devices offer the best of both worlds. The high-performance CMOS is used for building RAM resources. These high-performance structures support device operation up to 350 MHz. Additionally, the advanced Microsemi 0.13 μ m flash process incorporates high-voltage transistors and a high-isolation, triple-well process. Both of these are suited for the flash-based programmable logic and nonvolatile memory structures.

High-voltage transistors support the integration of analog technology in several ways. They aid in noise immunity so that the analog portions of the chip can be better isolated from the digital portions, increasing analog accuracy. Because they support high voltages, Microsemi flash FPGAs can be connected directly to high-voltage input signals, eliminating the need for external resistor divider networks, reducing component count, and increasing accuracy. By supporting higher internal voltages, the Microsemi advanced flash process enables high dynamic range on analog circuitry, increasing precision and signal–noise ratio. Microsemi flash FPGAs also drive high-voltage outputs, eliminating the need for external level shifters and drivers.

The unique triple-well process enables the integration of high-performance analog features with increased noise immunity and better isolation. By increasing the efficiency of analog design, the triple-well process also enables a smaller overall design size, reducing die size and cost.

The Analog Block consists of the Analog Quad I/O structure, RTC (for details refer to the "Real-Time Counter System" section on page 2-31), ADC, and ACM. All of these elements are combined in the single Analog Block macro, with which the user implements this functionality (Figure 2-64).

The Analog Block needs to be reset/reinitialized after the core powers up or the device is programmed. An external reset/initialize signal, which can come from the internal voltage regulator when it powers up, must be applied.

Table 2-50 • ADC Characteristics in Direct Input ModeCommercial Temperature Range Conditions, TJ = 85°C (unless noted otherwise),Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Тур.	Max.	Units
Direct Input	using Analog Pad AV, AC, A	Г				
VINADC	Input Voltage (Direct Input)	Refer to Table 3-2 on page 3-3				
CINADC	Input Capacitance	Channel not selected		7		pF
		Channel selected but not sampling		8		pF
		Channel selected and sampling		18		pF
ZINADC	Input Impedance	8-bit mode		2		kΩ
		10-bit mode		2		kΩ
		12-bit mode		2		kΩ
Analog Refe	erence Voltage VAREF					
VAREF	Accuracy	T _J = 25°C	2.537	2.56	2.583	V
	Temperature Drift of Internal Reference			65		ppm / °C
	External Reference		2.527		VCC33A + 0.05	V
ADC Accura	acy (using external reference) 1,2				
DC Accurac	у					
TUE	Total Unadjusted Error	8-bit mode		0.2	29	LSB
		10-bit mode		0.7	72	LSB
		12-bit mode		LSB		
INL	Integral Non-Linearity	8-bit mode		0.20	0.25	LSB
		10-bit mode		0.32	0.43	LSB
		12-bit mode		1.71	1.80	LSB
DNL	Differential Non-Linearity (no missing code)	8-bit mode		0.20	0.24	LSB
		10-bit mode		0.60	0.65	LSB
		12-bit mode		2.40	2.48	LSB
	Offset Error	8-bit mode		0.01	0.17	LSB
		10-bit mode		0.05	0.20	LSB
		12-bit mode		0.20	0.40	LSB
	Gain Error	8-bit mode		0.0004	0.003	LSB
		10-bit mode		0.002	0.011	LSB
		12-bit mode		0.007	0.044	LSB
	Gain Error (with internal reference)	All modes		2		% FSR

Notes:

1. Accuracy of the external reference is 2.56 V \pm 4.6 mV.

2. Data is based on characterization.

3. The sample rate is time-shared among active analog inputs.

Solution 3

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-4 on page 3-4. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCIX configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the bus switch, as shown in Figure 2-105. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.





Solution 4



Figure 2-106 • Solution 4



Device Architecture

Table 2-121 • 1.8 V LVCMOS High Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V

Applicable to Pro I/Os

Drive	Speed													
Strength	Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{PYS}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
2 mA	Std.	0.66	12.10	0.04	1.45	1.91	0.43	9.59	12.10	2.78	1.64	11.83	14.34	ns
	-1	0.56	10.30	0.04	1.23	1.62	0.36	8.16	10.30	2.37	1.39	10.06	12.20	ns
	-2	0.49	9.04	0.03	1.08	1.42	0.32	7.16	9.04	2.08	1.22	8.83	10.71	ns
4 mA	Std.	0.66	7.05	0.04	1.45	1.91	0.43	6.20	7.05	3.25	2.86	8.44	9.29	ns
	-1	0.56	6.00	0.04	1.23	1.62	0.36	5.28	6.00	2.76	2.44	7.18	7.90	ns
	-2	0.49	5.27	0.03	1.08	1.42	0.32	4.63	5.27	2.43	2.14	6.30	6.94	ns
8 mA	Std.	0.66	4.52	0.04	1.45	1.91	0.43	4.47	4.52	3.57	3.47	6.70	6.76	ns
	-1	0.56	3.85	0.04	1.23	1.62	0.36	3.80	3.85	3.04	2.95	5.70	5.75	ns
	-2	0.49	3.38	0.03	1.08	1.42	0.32	3.33	3.38	2.66	2.59	5.00	5.05	ns
12 mA	Std.	0.66	4.12	0.04	1.45	1.91	0.43	4.20	3.99	3.63	3.62	6.43	6.23	ns
	-1	0.56	3.51	0.04	1.23	1.62	0.36	3.57	3.40	3.09	3.08	5.47	5.30	ns
	-2	0.49	3.08	0.03	1.08	1.42	0.32	3.14	2.98	2.71	2.71	4.81	4.65	ns
16 mA	Std.	0.66	3.80	0.04	1.45	1.91	0.43	3.87	3.09	3.73	4.24	6.10	5.32	ns
	-1	0.56	3.23	0.04	1.23	1.62	0.36	3.29	2.63	3.18	3.60	5.19	4.53	ns
	-2	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-125 • 1.8 V LVCMOS High Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 1.7 V
Applicable to Standard I/Os

Drive	Speed										
Strength	Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.66	11.21	0.04	1.20	0.43	8.53	11.21	1.99	1.21	ns
	-1	0.56	9.54	0.04	1.02	0.36	7.26	9.54	1.69	1.03	ns
	-2	0.49	8.37	0.03	0.90	0.32	6.37	8.37	1.49	0.90	ns
4 mA	Std.	0.66	6.34	0.04	1.20	0.43	5.38	6.34	2.41	2.48	ns
	-1	0.56	5.40	0.04	1.02	0.36	4.58	5.40	2.05	2.11	ns
	-2	0.49	4.74	0.03	0.90	0.32	4.02	4.74	1.80	1.85	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-141 • Minimum and Maximum DC Input and Output Levels

2.5 GTL		VIL	VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
20 mA ³	-0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	-	20	20	124	169	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.



Figure 2-125 • AC Loading

Table 2-142 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.05	VREF + 0.05	0.8	0.8	1.2	10

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-143 • 2.5 V GTL

```
Commercial Temperature Range Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 0.8 V
```

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{zLS}	t _{zHS}	Units
Std.	0.66	2.13	0.04	2.46	0.43	2.16	2.13			4.40	4.36	ns
-1	0.56	1.81	0.04	2.09	0.36	1.84	1.81			3.74	3.71	ns
-2	0.49	1.59	0.03	1.83	0.32	1.61	1.59			3.28	3.26	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

VCC Core Supply Voltage

Supply voltage to the FPGA core, nominally 1.5 V. VCC is also required for powering the JTAG state machine, in addition to VJTAG. Even when a Fusion device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the Fusion device.

VCCIBx I/O Supply Voltage

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are either four (AFS090 and AFS250) or five (AFS600 and AFS1500) I/O banks on the Fusion devices plus a dedicated VJTAG bank.

Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VCCPLA/B PLL Supply Voltage

Supply voltage to analog PLL, nominally 1.5 V, where A and B refer to the PLL. AFS090 and AFS250 each have a single PLL. The AFS600 and AFS1500 devices each have two PLLs. Microsemi recommends tying VCCPLX to VCC and using proper filtering circuits to decouple VCC noise from PLL.

If unused, VCCPLA/B should be tied to GND.

VCOMPLA/B Ground for West and East PLL

VCOMPLA is the ground of the west PLL (CCC location F) and VCOMPLB is the ground of the east PLL (CCC location C).

VJTAG JTAG Supply Voltage

Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a Fusion device is in a JTAG chain of interconnected boards and it is desired to power down the board containing the Fusion device, this may be done provided both VJTAG and VCC to the Fusion part remain powered; otherwise, JTAG signals will not be able to transition the Fusion device, even in bypass mode.

VPUMP Programming Supply Voltage

Fusion devices support single-voltage ISP programming of the configuration flash and FlashROM. For programming, VPUMP should be in the 3.3 V +/-5% range. During normal device operation, VPUMP can be left floating or can be tied to any voltage between 0 V and 3.6 V.

When the VPUMP pin is tied to ground, it shuts off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 μ F and 0.33 μ F capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Dynamic Power Consumption of Various Internal Resources

Table 3-14 • Different Components Contributing to the Dynamic Power Consumption in Fusion Devices

		Power	Supply	Device-Specific ply Dynamic Contributions					
Parameter	Definition	Name	Setting	AFS1500	AFS600	AFS250	AFS090	Units	
PAC1	Clock contribution of a Global Rib	VCC	1.5 V	14.5	12.8	11	11	µW/MHz	
PAC2	Clock contribution of a Global Spine	VCC	1.5 V	2.5	1.9	1.6	0.8	µW/MHz	
PAC3	Clock contribution of a VersaTile row	VCC	1.5 V		0.8	1		µW/MHz	
PAC4	Clock contribution of a VersaTile used as a sequential module	VCC	1.5 V		0.1	1		µW/MHz	
PAC5	First contribution of a VersaTile used as a sequential module	VCC	1.5 V		0.0	7		µW/MHz	
PAC6	Second contribution of a VersaTile used as a sequential module	VCC	1.5 V		0.2	9		µW/MHz	
PAC7	Contribution of a VersaTile used as a combinatorial module	VCC	1.5 V		0.2	9		µW/MHz	
PAC8	Average contribution of a routing net	VCC	1.5 V	V 0.70					
PAC9	Contribution of an I/O input pin (standard dependent)	VCCI	See Table 3-12 on page 3-18						
PAC10	Contribution of an I/O output pin (standard dependent)	VCCI		See	Table 3-13	on page 3	-20		
PAC11	Average contribution of a RAM block during a read operation	VCC	1.5 V		25	5		µW/MHz	
PAC12	Average contribution of a RAM block during a write operation	VCC	1.5 V		30)		µW/MHz	
PAC13	Dynamic Contribution for PLL	VCC	1.5 V		2.6	6		µW/MHz	
PAC15	Contribution of NVM block during a read operation (F < $33MHz$)	VCC	1.5 V		35	8		µW/MHz	
PAC16	1st contribution of NVM block during a read operation (F > 33 MHz)	VCC	1.5 V	V 12.88				mW	
PAC17	2nd contribution of NVM block during a read operation (F > 33 MHz)	VCC	1.5 V	4.8				µW/MHz	
PAC18	Crystal Oscillator contribution	VCC33A	3.3 V		0.6	3		mW	
PAC19	RC Oscillator contribution	VCC33A	3.3 V		3.3	3		mW	
PAC20	Analog Block dynamic power contribution of ADC	VCC	1.5 V		3			mW	

FG256									
Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function					
A1	GND	GND GND		GND					
A2	VCCIB0	VCCIB0 VCCIB0		VCCIB0					
A3	GAB0/IO02RSB0V0	GAA0/IO00RSB0V0	GAA0/IO01NDB0V0	GAA0/IO01NDB0V0					
A4	GAB1/IO03RSB0V0	GAA1/IO01RSB0V0	GAA1/IO01PDB0V0	GAA1/IO01PDB0V0					
A5	GND	GND	GND	GND					
A6	IO07RSB0V0	IO11RSB0V0	IO10PDB0V1	IO07PDB0V1					
A7	IO10RSB0V0	IO14RSB0V0	IO12PDB0V1	IO13PDB0V2					
A8	IO11RSB0V0	IO15RSB0V0	IO12NDB0V1	IO13NDB0V2					
A9	IO16RSB0V0	IO24RSB0V0 IO22NDB1V		IO24NDB1V0					
A10	IO17RSB0V0	IO25RSB0V0 IO22PDB1V0		IO24PDB1V0					
A11	IO18RSB0V0	IO26RSB0V0	IO26RSB0V0 IO24NDB1V1						
A12	GND	GND	GND	GND					
A13	GBC0/IO25RSB0V0	GBA0/IO38RSB0V0	GBA0/IO28NDB1V1	GBA0/IO42NDB1V2					
A14	GBA0/IO29RSB0V0	IO32RSB0V0	IO29NDB1V1	IO43NDB1V2					
A15	VCCIB0	VCCIB0	VCCIB1	VCCIB1					
A16	GND	GND	GND	GND					
B1	VCOMPLA	VCOMPLA	VCOMPLA	VCOMPLA					
B2	VCCPLA	VCCPLA	VCCPLA	VCCPLA					
B3	GAA0/IO00RSB0V0	IO07RSB0V0	IO00NDB0V0	IO00NDB0V0					
B4	GAA1/IO01RSB0V0	IO06RSB0V0	IO00PDB0V0	IO00PDB0V0					
B5	NC	GAB1/IO03RSB0V0	GAB1/IO02PPB0V0	GAB1/IO02PPB0V0					
B6	IO06RSB0V0	IO10RSB0V0	IO10NDB0V1	IO07NDB0V1					
B7	VCCIB0	VCCIB0	VCCIB0	VCCIB0					
B8	IO12RSB0V0	IO16RSB0V0	IO18NDB1V0	IO22NDB1V0					
В9	IO13RSB0V0	IO17RSB0V0	IO18PDB1V0	IO22PDB1V0					
B10	VCCIB0	VCCIB0	VCCIB1	VCCIB1					
B11	IO19RSB0V0	IO27RSB0V0	IO24PDB1V1	IO29PDB1V1					
B12	GBB0/IO27RSB0V0	GBC0/IO34RSB0V0	GBC0/IO26NPB1V1	GBC0/IO40NPB1V2					
B13	GBC1/IO26RSB0V0	GBA1/IO39RSB0V0	GBA1/IO28PDB1V1	GBA1/IO42PDB1V2					
B14	GBA1/IO30RSB0V0	IO33RSB0V0	IO29PDB1V1	IO43PDB1V2					
B15	NC	NC	VCCPLB	VCCPLB					
B16	NC	NC	VCOMPLB	VCOMPLB					
C1	VCCIB3	VCCIB3	VCCIB4	VCCIB4					
C2	GND	GND	GND	GND					
C3	VCCIB3	VCCIB3	VCCIB4	VCCIB4					
C4	NC	NC	VCCIB0	VCCIB0					
C5	VCCIB0	VCCIB0	VCCIB0 VCCIB0 VC						
C6	GAC1/IO05RSB0V0	GAC1/IO05RSB0V0	GAC1/IO03PDB0V0	GAC1/IO03PDB0V0					



Package Pin Assignments

FG256									
Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function					
H3	XTAL2	XTAL2	XTAL2	XTAL2					
H4	XTAL1	XTAL1	XTAL1	XTAL1					
H5	GNDOSC	GNDOSC	GNDOSC	GNDOSC					
H6	VCCOSC	VCCOSC	VCCOSC VCCOSC						
H7	VCC	VCC VCC		VCC					
H8	GND	GND	GND	GND					
H9	VCC	VCC VCC		VCC					
H10	GND	GND	GND	GND					
H11	GDC0/IO38NDB1V0	IO51NDB1V0	IO51NDB1V0 IO47NDB2V0						
H12	GDC1/IO38PDB1V0	IO51PDB1V0	IO47PDB2V0	IO69PDB2V0					
H13	GDB1/IO39PDB1V0	GCA1/IO49PDB1V0	GCA1/IO45PDB2V0	GCA1/IO64PDB2V0					
H14	GDB0/IO39NDB1V0	GCA0/IO49NDB1V0	GCA0/IO45NDB2V0	GCA0/IO64NDB2V0					
H15	GCA0/IO36NDB1V0	GCB0/IO48NDB1V0	GCB0/IO44NDB2V0	GCB0/IO63NDB2V0					
H16	GCA1/IO36PDB1V0	GCB1/IO48PDB1V0	GCB1/IO44PDB2V0	GCB1/IO63PDB2V0					
J1	GEA0/IO44NDB3V0	GFA0/IO66NDB3V0	GFA0/IO70NDB4V0	GFA0/IO105NDB4V0					
J2	GEA1/IO44PDB3V0	GFA1/IO66PDB3V0	GFA1/IO70PDB4V0	GFA1/IO105PDB4V0					
J3	IO43NDB3V0	GFB0/IO67NDB3V0	GFB0/IO71NDB4V0	GFB0/IO106NDB4V0					
J4	GEC2/IO43PDB3V0	GFB1/IO67PDB3V0	GFB1/IO71PDB4V0	GFB1/IO106PDB4V0					
J5	NC	GFC0/IO68NDB3V0 GFC0/IO72NDB4V0		GFC0/IO107NDB4V0					
J6	NC	GFC1/IO68PDB3V0	GFC1/IO72PDB4V0	GFC1/IO107PDB4V0					
J7	GND	GND	GND	GND					
J8	VCC	VCC	VCC	VCC					
J9	GND	GND	GND	GND					
J10	VCC	VCC	VCC	VCC					
J11	GDC2/IO41NPB1V0	IO56NPB1V0	IO56NPB2V0	IO83NPB2V0					
J12	NC	GDB0/IO53NPB1V0	GDB0/IO53NPB2V0	GDB0/IO80NPB2V0					
J13	NC	GDA1/IO54PDB1V0	GDA1/IO54PDB2V0	GDA1/IO81PDB2V0					
J14	GDA0/IO40PDB1V0	GDC1/IO52PPB1V0	GDC1/IO52PPB2V0	GDC1/IO79PPB2V0					
J15	NC	IO50NPB1V0	IO51NSB2V0	IO77NSB2V0					
J16	GDA2/IO40NDB1V0	GDC0/IO52NPB1V0	GDC0/IO52NPB2V0	GDC0/IO79NPB2V0					
K1	NC	IO65NPB3V0 IO67NPB4V0		IO92NPB4V0					
K2	VCCIB3	VCCIB3 VCCIB4		VCCIB4					
K3	NC	IO65PPB3V0	IO67PPB4V0	IO92PPB4V0					
K4	NC	IO64PDB3V0	IO65PDB4V0	IO96PDB4V0					
K5	GND	GND	GND	GND					
K6	NC	IO64NDB3V0	IO65NDB4V0	IO96NDB4V0					
K7	VCC	VCC	VCC	VCC					
K8	GND	GND	GND	GND					



FG484



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/default.aspx.



FG676



Note

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Package Pin Assignments

FG676		FG676		FG676	
Pin Number	AFS1500 Function	Pin Number	AFS1500 Function	Pin Number	AFS1500 Function
L17	VCCIB2	N1	NC	P11	VCC
L18	GCB2/IO60PDB2V0	N2	NC	P12	GND
L19	IO58NDB2V0	N3	IO108NDB4V0	P13	VCC
L20	IO57NDB2V0	N4	VCCOSC	P14	GND
L21	IO59NDB2V0	N5	VCCIB4	P15	VCC
L22	GCC2/IO61PDB2V0	N6	XTAL2	P16	GND
L23	IO55PPB2V0	N7	GFC1/IO107PDB4V0	P17	VCCIB2
L24	IO56PDB2V0	N8	VCCIB4	P18	IO70NDB2V0
L25	IO55NPB2V0	N9	GFB1/IO106PDB4V0	P19	VCCIB2
L26	GND	N10	VCCIB4	P20	IO69NDB2V0
M1	NC	N11	GND	P21	GCA0/IO64NDB2V0
M2	VCCIB4	N12	VCC	P22	VCCIB2
M3	GFC2/IO108PDB4V0	N13	GND	P23	GCB0/IO63NDB2V0
M4	GND	N14	VCC	P24	GCB1/IO63PDB2V0
M5	IO109NDB4V0	N15	GND	P25	IO66NDB2V0
M6	IO110NDB4V0	N16	VCC	P26	IO67PDB2V0
M7	GND	N17	VCCIB2	R1	NC
M8	IO104NDB4V0	N18	IO70PDB2V0	R2	VCCIB4
M9	IO111NDB4V0	N19	VCCIB2	R3	IO103NDB4V0
M10	GND	N20	IO69PDB2V0	R4	GND
M11	VCC	N21	GCA1/IO64PDB2V0	R5	IO101PDB4V0
M12	GND	N22	VCCIB2	R6	IO100NPB4V0
M13	VCC	N23	GCC0/IO62NDB2V0	R7	GND
M14	GND	N24	GCC1/IO62PDB2V0	R8	IO99PDB4V0
M15	VCC	N25	IO66PDB2V0	R9	IO97PDB4V0
M16	GND	N26	IO65NDB2V0	R10	GND
M17	GND	P1	NC	R11	GND
M18	IO60NDB2V0	P2	NC	R12	VCC
M19	IO58PDB2V0	P3	IO103PDB4V0	R13	GND
M20	GND	P4	XTAL1	R14	VCC
M21	IO68NPB2V0	P5	VCCIB4	R15	GND
M22	IO61NDB2V0	P6	GNDOSC	R16	VCC
M23	GND	P7	GFC0/IO107NDB4V0	R17	GND
M24	IO56NDB2V0	P8	VCCIB4	R18	GDB2/IO83PDB2V0
M25	VCCIB2	P9	GFB0/IO106NDB4V0	R19	IO78PDB2V0
M26	IO65PDB2V0	P10	VCCIB4	R20	GND