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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	119
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs600-2fg256

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RC Oscillator

The RC oscillator is an on-chip free-running clock source generating a 100 MHz clock. It can be used as a source clock for both on-chip and off-chip resources. When used in conjunction with the Fusion PLL and CCC circuits, the RC oscillator clock source can be used to generate clocks of varying frequency and phase.

The Fusion RC oscillator is very accurate at $\pm 1\%$ over commercial temperature ranges and and $\pm 3\%$ over industrial temperature ranges. It is an automated clock, requiring no setup or configuration by the user. It requires only that the power and GNDOSC pins be connected; no external components are required. The RC oscillator can be used to drive either a PLL or another internal signal.

RC Oscillator Characteristics

Parameter	Description	Conditions	Min.	Тур.	Max.	Units
	Operating Frequency			100		MHz
F _{RC}	Accuracy	Temperature: 0°C to 85°C Voltage: 3.3 V ± 5%		1		%
		Temperature: -40° C to 125° C Voltage: 3.3 V ± 5%		3		%
	Output Jitter	Period Jitter (at 5 k cycles)		100		ps
		Cycle–Cycle Jitter (at 5 k cycles)		100		ps
		Period Jitter (at 5 k cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps
		Cycle–Cycle Jitter (at 5 k cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps
	Output Duty Cycle			50		%
IDYNRC	Operating Current			1		mA

Table 2-9 • Electrical Characteristics of RC Oscillator



Table 2-19 • Flash Memory Block Pin Names (continued)

Interface Name	Width	Direction	Description
STATUS[1:0]	2	Out	Status of the last operation completed:
			00: Successful completion
			01: Read-/Unprotect-Page: single error detected and corrected
			Write: operation addressed a write-protected page Erase-Page: protection violation Program: Page Buffer is unmodified Protection violation
			10: Read-/Unprotect-Page: two or more errors detected
			11: Write: attempt to write to another page before programming current page
			Erase-Page/Program: page write count has exceeded the 10-year retention threshold
UNPROTECTPAGE	1	In	When asserted, the page addressed is copied into the Page Buffer and the Page Buffer is made writable.
WD[31:0]	32	In	Write data
WEN	1	In	When asserted, stores WD in the page buffer.

All flash memory block input signals are active high, except for RESET.



Table 2-25 • Flash Memory Block Timing (continued)Commercial Temperature Range Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{SUPGLOSSPRO}	Page Loss Protect Setup Time for the Control Logic	1.69	1.93	2.27	ns
t _{HDPGLOSSPRO}	Page Loss Protect Hold Time for the Control Logic	0.00	0.00	0.00	ns
t _{SUPGSTAT}	Page Status Setup Time for the Control Logic	2.49	2.83	3.33	ns
t _{HDPGSTAT}	Page Status Hold Time for the Control Logic	0.00	0.00	0.00	ns
t _{SUOVERWRPG}	Over Write Page Setup Time for the Control Logic	1.88	2.14	2.52	ns
t _{HDOVERWRPG}	Over Write Page Hold Time for the Control Logic	0.00	0.00	0.00	ns
t _{SULOCKREQUEST}	Lock Request Setup Time for the Control Logic	0.87	0.99	1.16	ns
t _{HDLOCKREQUEST}	Lock Request Hold Time for the Control Logic	0.00	0.00	0.00	ns
t _{RECARNVM}	Reset Recovery Time	0.94	1.07	1.25	ns
t _{REMARNVM}	Reset Removal Time	0.00	0.00	0.00	ns
t _{mpwarnvm}	Asynchronous Reset Minimum Pulse Width for the Control Logic	10.00	12.50	12.50	ns
t _{MPWCLKNVM}	Clock Minimum Pulse Width for the Control Logic	4.00	5.00	5.00	ns
+	Maximum Frequency for Clock for the Control Logic – for AFS1500/AFS600	80.00	80.00	80.00	MHz
'FMAXCLKNVM	Maximum Frequency for Clock for the Control Logic – for AFS250/AFS090	100.00	80.00	80.00	MHz

FlashROM

Fusion devices have 1 kbit of on-chip nonvolatile flash memory that can be read from the FPGA core fabric. The FlashROM is arranged in eight banks of 128 bits during programming. The 128 bits in each bank are addressable as 16 bytes during the read-back of the FlashROM from the FPGA core (Figure 2-45).

The FlashROM can only be programmed via the IEEE 1532 JTAG port. It cannot be programmed directly from the FPGA core. When programming, each of the eight 128-bit banks can be selectively reprogrammed. The FlashROM can only be reprogrammed on a bank boundary. Programming involves an automatic, on-chip bank erase prior to reprogramming the bank. The FlashROM supports a synchronous read and can be read on byte boundaries. The upper three bits of the FlashROM address from the FPGA core define the bank that is being accessed. The lower four bits of the FlashROM address from the FPGA core define which of the 16 bytes in the bank is being accessed.

The maximum FlashROM access clock is given in Table 2-26 on page 2-54. Figure 2-46 shows the timing behavior of the FlashROM access cycle—the address has to be set up on the rising edge of the clock for DOUT to be valid on the next falling edge of the clock.

If the address is unchanged for two cycles:

- D0 becomes invalid t_{CK2Q} ns after the second rising edge of the clock.
- D0 becomes valid again t_{CK2Q} ns after the second falling edge.

If the address unchanged for three cycles:

- D0 becomes invalid t_{CK2Q} ns after the second rising edge of the clock.
- D0 becomes valid again t_{CK2Q} ns after the second falling edge.
- D0 becomes invalid t_{CK2Q} ns after the third rising edge of the clock.
- D0 becomes valid again t_{CK2Q} ns after the third falling edge.



RAM4K9 Description



Figure 2-48 • RAM4K9



The following signals are used to configure the FIFO4K18 memory element.

WW and RW

These signals enable the FIFO to be configured in one of the five allowable aspect ratios (Table 2-33).

TADIE 2-33 · ASDECLINALIO SELLINUS IOI WWWIZ.VI

WW2, WW1, WW0	RW2, RW1, RW0	D×W	
000	000	4k×1	
001	001	2k×2	
010	010	1k×4	
011	011	512×9	
100	100	256×18	
101, 110, 111	101, 110, 111	Reserved	

WBLK and RBLK

These signals are active low and will enable the respective ports when Low. When the RBLK signal is High, the corresponding port's outputs hold the previous value.

WEN and REN

Read and write enables. WEN is active low and REN is active high by default. These signals can be configured as active high or low.

WCLK and RCLK

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

RPIPE

This signal is used to specify pipelined read on the output. A Low on RPIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A High indicates a pipelined read, and data appears on the output in the next clock cycle.

RESET

This active low signal resets the output to zero when asserted. It resets the FIFO counters. It also sets all the RD pins Low, the FULL and AFULL pins Low, and the EMPTY and AEMPTY pins High (Table 2-34).

Table 2-34 • Input Data Signal Usage for Different Aspect Ratios

D×W	WD/RD Unused
4k×1	WD[17:1], RD[17:1]
2k×2	WD[17:2], RD[17:2]
1k×4	WD[17:4], RD[17:4]
512×9	WD[17:9], RD[17:9]
256×18	-

WD

This is the input data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. When a data width less than 18 is specified, unused higher-order signals must be grounded (Table 2-34).

RD

This is the output data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. Like the WD bus, high-order bits become unusable if the data width is less than 18. The output data on unused pins is undefined (Table 2-34).





Figure 2-60 • FIFO EMPTY Flag and AEMPTY Flag Assertion



	VAREF		
	ADCGNDREF		
	AV0	DAVOUT0	
	AC0	DACOUT0	
	ΔΤΟ		
	•	DAIOUIU	
	• • •		
	AV9	DAVOUT9	
	AC9	DACOU19	
	AT9	DATOUT9	
	ATRETURN01		
	•	AG0	
	Å TRETURN9	AG1	
	DENAV0	•	
		<u>م</u>	
		A09	
	DENAIU		
	•		
	DENAV0		
	DENAC0		
	DENAT0		
	CMSTB0		
	•		
	ĊSMTB9		
	GDONO		
	CDON0		
	GDON9		
	IMSTBO		
	•		
	TMSTB9		
	MODE[3:0]	BUSY	
	TVC[7:0]	CALIBRATE	
	STC[7:0]	DATAVALID	
	CHNUMBER[4:0]	SAMPLE	
	TMSTINT	RESULTI11:01	
	ADCSTART	RTCMATCH	
	PWRDWN	RICXILSEL	
	ADCRESET	RTCPSMMATCH	
	RTCCLK		
	SYSCLK		
	ACMIVEN	ACMRDATA[7:0]	
<u> </u>	ACMRESET		
	ACMWDATA		
	ACMADDR		
	ACMCLK		
	AE	3	

Figure 2-64 • Analog Block Macro



Figure 2-72 • Positive Current Monitor

Care must be taken when choosing the right resistor for current measurement application. Note that because of the 10× amplification, the maximum measurable difference between the AV and AC pads is V_{AREF} / 10. A larger AV-to-AC voltage drop will result in ADC saturation; that is, the digital code put out by the ADC will stay fixed at the full scale value. Therefore, the user must select the external sense resistor appropriately. Table 2-38 shows recommended resistor values for different current measurement ranges. When choosing resistor values for a system, there is a trade-off between measurement accuracy and power consumption. Choosing a large resistor will increase the voltage drop and hence increase accuracy of the measurement; however the larger voltage drop dissipates more power (P = I² × R).

The Current Monitor is a unipolar system, meaning that the differential voltage swing must be from 0 V to $V_{AREF}/10$. Therefore, the Current Monitor only supports differential voltage where $|V_{AV}-V_{AC}|$ is greater than 0 V. This results in the requirement that the potential of the AV pad must be larger than the potential of the AC pad. This is straightforward for positive voltage systems. For a negative voltage system, it means that the AV pad must be "more negative" than the AC pad. This is shown in Figure 2-73.

In this case, both the AV pad and the AC pad are configured for negative operations and the output of the differential amplifier still falls between 0 V and V_{AREF} as required.

Current Range Recommended Minimum Resistor Value (Ohms		
> 5 mA – 10 mA	10 – 20	
> 10 mA – 20 mA	5 – 10	
> 20 mA – 50 mA	2.5 – 5	
> 50 mA – 100 mA	1 – 2	
> 100 mA – 200 mA	0.5 – 1	
> 200 mA – 500 mA	0.3 – 0.5	
> 500 mA – 1 A	0.1 – 0.2	
> 1 A – 2 A	0.05 – 0.1	
> 2 A – 4 A	0.025 – 0.05	
> 4 A – 8 A	0.0125 – 0.025	
> 8 A – 12 A	0.00625 – 0.02	

Table 2-37 • Recommended Resistor for Different Current Range Measurement



Fusion uses a remote diode as a temperature sensor. The Fusion Temperature Monitor uses a differential input; the AT pin and ATRTN (AT Return) pin are the differential inputs to the Temperature Monitor. There is one Temperature Monitor in each Quad. A simplified block diagram is shown in Figure 2-77.



Figure 2-77 • Block Diagram for Temperature Monitor Circuit

The Fusion approach to measuring temperature is forcing two different currents through the diode with a ratio of 10:1. The switch that controls the different currents is controlled by the Temperature Monitor Strobe signal, TMSTB. Setting TMSTB to '1' will initiate a Temperature reading. The TMSTB should remain '1' until the ADC finishes sampling the voltage from the Temperature Monitor. The minimum sample time for the Temperature Monitor cannot be less than the minimum strobe high time minus the setup time. Figure 2-78 shows the timing diagram.





Note: When the IEEE 1149.1 Boundary Scan EXTEST instruction is executed, the AG pad drive strength ceases and becomes a 1 µA sink into the Fusion device.

INL – Integral Non-Linearity

INL is the deviation of an actual transfer function from a straight line. After nullifying offset and gain errors, the straight line is either a best-fit straight line or a line drawn between the end points of the transfer function (Figure 2-85).



Figure 2-85 • Integral Non-Linearity (INL)

LSB – Least Significant Bit

In a binary number, the LSB is the least weighted bit in the group. Typically, the LSB is the furthest right bit. For an ADC, the weight of an LSB equals the full-scale voltage range of the converter divided by 2^N , where N is the converter's resolution.

EQ 13 shows the calculation for a 10-bit ADC with a unipolar full-scale voltage of 2.56 V:

EQ 13

No Missing Codes

An ADC has no missing codes if it produces all possible digital codes in response to a ramp signal applied to the analog input.

Analog MUX Channel	Signal	Analog Quad Number
16	AV5	
17	AC5	Analog Quad 5
18	AT5	
19	AV6	
20	AC6	Analog Quad 6
21	AT6	
22	AV7	
23	AC7	Analog Quad 7
24	AT7	
25	AV8	
26	AC8	Analog Quad 8
27	AT8	
28	AV9	
29	AC9	Analog Quad 9
30	AT9	
31	Internal temperature monitor	

Table 2-40 • Analog MUX Channels (continued)

The ADC can be powered down independently of the FPGA core, as an additional control or for powersaving considerations, via the PWRDWN pin of the Analog Block. The PWRDWN pin controls only the comparators in the ADC.

ADC Modes

The Fusion ADC can be configured to operate in 8-, 10-, or 12-bit modes, power-down after conversion, and dynamic calibration. This is controlled by MODE[3:0], as defined in Table 2-41 on page 2-106.

The output of the ADC is the RESULT[11:0] signal. In 8-bit mode, the Most Significant 8 Bits RESULT[11:4] are used as the ADC value and the Least Significant 4 Bits RESULT[3:0] are logical '0's. In 10-bit mode, RESULT[11:2] are used the ADC value and RESULT[1:0] are logical 0s.

Name	Bits	Function
MODE	3	 0 – Internal calibration after every conversion; two ADCCLK cycles are used after the conversion. 1 – No calibration after every conversion
MODE	2	0 – Power-down after conversion 1 – No Power-down after conversion
MODE	1:0	00 – 10-bit 01 – 12-bit 10 – 8-bit 11 – Unused



Table 2-50 • ADC Characteristics in Direct Input Mode (continued)

Commercial Temperature Range Conditions, $T_J = 85^{\circ}C$ (unless noted otherwise), Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Тур.	Max.	Units
Dynamic Pe	erformance					
SNR	Signal-to-Noise Ratio	8-bit mode	48.0	49.5		dB
		10-bit mode	58.0	60.0		dB
		12-bit mode	62.9	64.5		dB
SINAD	Signal-to-Noise Distortion	8-bit mode	47.6	49.5		dB
		10-bit mode	57.4	59.8		dB
		12-bit mode	62.0	64.2		dB
THD	Total Harmonic Distortion	8-bit mode		-74.4	-63.0	dBc
		10-bit mode		-78.3	-63.0	dBc
		12-bit mode		-77.9	-64.4	dBc
ENOB	Effective Number of Bits	8-bit mode	7.6	7.9		bits
		10-bit mode	9.5	9.6		bits
		12-bit mode	10.0	10.4		bits
Conversion	Rate	ŀ				
	Conversion Time	8-bit mode	1.7			μs
		10-bit mode	1.8			μs
		12-bit mode	2			μs
	Sample Rate	8-bit mode			600	Ksps
		10-bit mode			550	Ksps
		12-bit mode			500	Ksps

Notes:

1. Accuracy of the external reference is 2.56 V \pm 4.6 mV.

2. Data is based on characterization.

3. The sample rate is time-shared among active analog inputs.

Table 2-109 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Standard I/Os

Drive	Speed										
Strength	Grade	^t DOUT	τ _{DP}	τ _{DIN}	τ _{PY}	^t EOUT	۲ _{ZL}	τ _{ZH}	τ _{LZ}	τ _{HZ}	Units
2 mA	Std.	0.66	7.07	0.04	1.00	0.43	7.20	6.23	2.07	2.15	ns
	-1	0.56	6.01	0.04	0.85	0.36	6.12	5.30	1.76	1.83	ns
	-2 ²	0.49	5.28	0.03	0.75	0.32	5.37	4.65	1.55	1.60	ns
4 mA	Std.	0.66	7.07	0.04	1.00	0.43	7.20	6.23	2.07	2.15	ns
	-1	0.56	6.01	0.04	0.85	0.36	6.12	5.30	1.76	1.83	ns
	-2	0.49	5.28	0.03	0.75	0.32	5.37	4.65	1.55	1.60	ns
6 mA	Std.	0.66	4.41	0.04	1.00	0.43	4.49	3.75	2.39	2.69	ns
	-1	0.56	3.75	0.04	0.85	0.36	3.82	3.19	2.04	2.29	ns
	-2	0.49	3.29	0.03	0.75	0.32	3.36	2.80	1.79	2.01	ns
8 mA	Std.	0.66	4.41	0.04	1.00	0.43	4.49	3.75	2.39	2.69	ns
	-1	0.56	3.75	0.04	0.85	0.36	3.82	3.19	2.04	2.29	ns
	-2	0.49	3.29	0.03	0.75	0.32	3.36	2.80	1.79	2.01	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

2.5 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 2.5 V.

Table 2-141 • Minimum and Maximum DC Input and Output Levels

2.5 GTL		VIL	VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
20 mA ³	-0.3	VREF – 0.05	VREF + 0.05	3.6	0.4	-	20	20	124	169	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.



Figure 2-125 • AC Loading

Table 2-142 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.05	VREF + 0.05	0.8	0.8	1.2	10

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-143 • 2.5 V GTL

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Commercial Temperature Range Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 0.8 V
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Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{zLS}	t _{zHS}	Units
Std.	0.66	2.13	0.04	2.46	0.43	2.16	2.13			4.40	4.36	ns
-1	0.56	1.81	0.04	2.09	0.36	1.84	1.81			3.74	3.71	ns
-2	0.49	1.59	0.03	1.83	0.32	1.61	1.59			3.28	3.26	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Symbol	Parameter	Commercial	Industrial	Units
AV, AC	Unpowered, ADC reset asserted or unconfigured	-11.0 to 12.6	-11.0 to 12.0	V
	Analog input (+16 V to +2 V prescaler range)	-0.4 to 12.6	-0.4 to 12.0	V
	Analog input (+1 V to +0.125 V prescaler range)	-0.4 to 3.75	-0.4 to 3.75	V
	Analog input (–16 V to –2 V prescaler range)	-11.0 to 0.4	-11.0 to 0.4	V
	Analog input (–1 V to –0.125 V prescaler range)	-3.75 to 0.4	-3.75 to 0.4	V
	Analog input (direct input to ADC)	-0.4 to 3.75	-0.4 to 3.75	V
	Digital input	-0.4 to 12.6	-0.4 to 12.0	V
AG	Unpowered, ADC reset asserted or unconfigured	-11.0 to 12.6	-11.0 to 12.0	V
	Low Current Mode (1 μ A, 3 μ A, 10 μ A, 30 μ A)	-0.4 to 12.6	-0.4 to 12.0	V
	Low Current Mode (–1 μΑ, –3 μΑ, –10 μΑ, –30 μΑ)	-11.0 to 0.4	-11.0 to 0.4	V
	High Current Mode ³	-11.0 to 12.6	-11.0 to 12.0	V
AT	Unpowered, ADC reset asserted or unconfigured	–0.4 to 16.0	-0.4 to 15.0	V
	Analog input (+16 V, 4 V prescaler range)	-0.4 to 16.0	-0.4 to 15.0	V
	Analog input (direct input to ADC)	-0.4 to 3.75	-0.4 to 3.75	V
	Digital input	-0.4 to 16.0	-0.4 to 15.0	V
T _{STG} ⁴	Storage temperature	-65	°C	
T _J ⁴	Junction temperature	+	125	°C

Table 3-1 •	Absolute	Maximum	Ratings	(continued)
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Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-4 on page 3-4.

2. Analog data not valid beyond 3.65 V.

3. The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.

4. For flash programming and retention maximum limits, refer to Table 3-5 on page 3-5. For recommended operating limits refer to Table 3-2 on page 3-3.



DC and Power Characteristics

Table 3-10 • AFS250 Q	Quiescent Supply Current	Characteristics (continued)
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Parameter	Description	Conditions	Temp.	Min	Тур	Max	Unit
IPP	Programming supply	Non-programming mode,	T _J = 25°C		37	80	μA
	current	VPUMP = 3.63 V	T _J = 85°C		37	80	μA
			T _J = 100°C		80	100	μA
		Standby mode ⁵ or Sleep mode ⁶ , VPUMP = 0 V			0	0	μA
ICCNVM	Embedded NVM current	Reset asserted,	T _J = 25°C		10	40	μA
		VCCNVM = 1.575 V	T _J = 85°C		14	40	μA
			T _J = 100°C		14	40	μA
ICCPLL	1.5 V PLL quiescent current	Operational standby,	T _J = 25°C		65	100	μA
		VCCPLL = 1.575 V	T _J = 85°C		65	100	μA
			T _J = 100°C		65	100	μA

Notes:

- 1. ICC is the 1.5 V power supplies, ICC, ICCPLL, ICC15A, ICCNVM.
- 2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.
- 3. ICCI includes all ICCI0, ICCI1, and ICCI2.
- 4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.
- 5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.
- 6. Sleep Mode, VCC = VJTA G = VPUMP = 0 V.

RAM Dynamic Contribution—P_{MEMORY}

Operating Mode

 $P_{MEMORY} = (N_{BLOCKS} * PAC11 * \beta_2 * F_{READ-CLOCK}) + (N_{BLOCKS} * PAC12 * \beta_3 * F_{WRITE-CLOCK})$ $N_{BLOCKS} \text{ is the number of RAM blocks used in the design.}$

F_{READ-CLOCK} is the memory read clock frequency.

 β_2 is the RAM enable rate for read operations—guidelines are provided in Table 3-17 on page 3-27.

 β_3 the RAM enable rate for write operations—guidelines are provided in Table 3-17 on page 3-27.

 $\mathsf{F}_{\mathsf{WRITE}\text{-}\mathsf{CLOCK}}$ is the memory write clock frequency.

Standby Mode and Sleep Mode

P_{MEMORY} = 0 W

PLL/CCC Dynamic Contribution—PPLL

Operating Mode

P_{PLL} = PAC13 * F_{CLKOUT}

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.¹

Standby Mode and Sleep Mode

 $P_{PLL} = 0 W$

Nonvolatile Memory Dynamic Contribution—P_{NVM}

Operating Mode

The NVM dynamic power consumption is a piecewise linear function of frequency.

 $P_{NVM} = N_{NVM-BLOCKS} * \beta_4 * PAC15 * F_{READ-NVM}$ when $F_{READ-NVM} \le 33$ MHz,

 $P_{NVM} = N_{NVM-BLOCKS} * \beta_4 * (PAC16 + PAC17 * F_{READ-NVM} \text{ when } F_{READ-NVM} > 33 \text{ MHz}$

N_{NVM-BLOCKS} is the number of NVM blocks used in the design (2 inAFS600).

 β_4 is the NVM enable rate for read operations. Default is 0 (NVM mainly in idle state). F_{READ-NVM} is the NVM read clock frequency.

Standby Mode and Sleep Mode

P_{NVM} = 0 W

Crystal Oscillator Dynamic Contribution—P_{XTL-OSC}

Operating Mode

 $P_{XTL-OSC} = PAC18$

Standby Mode

 $P_{XTL-OSC} = PAC18$

Sleep Mode

 $P_{XTL-OSC} = 0 W$

The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula output clock by adding its corresponding contribution (P_{AC14} * F_{CLKOUT} product) to the total PLL contribution.



FG256								
Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function				
C7	IO09RSB0V0	IO12RSB0V0	IO06NDB0V0	IO09NDB0V1				
C8	IO14RSB0V0	IO22RSB0V0	IO16PDB1V0	IO23PDB1V0				
C9	IO15RSB0V0	IO23RSB0V0	IO16NDB1V0	IO23NDB1V0				
C10	IO22RSB0V0	IO30RSB0V0	IO25NDB1V1	IO31NDB1V1				
C11	IO20RSB0V0	IO31RSB0V0	IO25PDB1V1	IO31PDB1V1				
C12	VCCIB0	VCCIB0	VCCIB1	VCCIB1				
C13	GBB1/IO28RSB0V0	GBC1/IO35RSB0V0	GBC1/IO26PPB1V1	GBC1/IO40PPB1V2				
C14	VCCIB1	VCCIB1	VCCIB2	VCCIB2				
C15	GND	GND	GND	GND				
C16	VCCIB1	VCCIB1	VCCIB2	VCCIB2				
D1	GFC2/IO50NPB3V0	IO75NDB3V0	IO84NDB4V0	IO124NDB4V0				
D2	GFA2/IO51NDB3V0	GAB2/IO75PDB3V0	GAB2/IO84PDB4V0	GAB2/IO124PDB4V0				
D3	GAC2/IO51PDB3V0	IO76NDB3V0	IO85NDB4V0	IO125NDB4V0				
D4	GAA2/IO52PDB3V0	GAA2/IO76PDB3V0	GAA2/IO85PDB4V0	GAA2/IO125PDB4V0				
D5	GAB2/IO52NDB3V0	GAB0/IO02RSB0V0	GAB0/IO02NPB0V0	GAB0/IO02NPB0V0				
D6	GAC0/IO04RSB0V0	GAC0/IO04RSB0V0	GAC0/IO03NDB0V0	GAC0/IO03NDB0V0				
D7	IO08RSB0V0	IO13RSB0V0	IO06PDB0V0	IO09PDB0V1				
D8	NC	IO20RSB0V0	IO14NDB0V1	IO15NDB0V2				
D9	NC	IO21RSB0V0	IO14PDB0V1	IO15PDB0V2				
D10	IO21RSB0V0	IO28RSB0V0	IO23PDB1V1	IO37PDB1V2				
D11	IO23RSB0V0	GBB0/IO36RSB0V0	GBB0/IO27NDB1V1	GBB0/IO41NDB1V2				
D12	NC	NC	VCCIB1	VCCIB1				
D13	GBA2/IO31PDB1V0	GBA2/IO40PDB1V0	GBA2/IO30PDB2V0	GBA2/IO44PDB2V0				
D14	GBB2/IO31NDB1V0	IO40NDB1V0	IO30NDB2V0	IO44NDB2V0				
D15	GBC2/IO32PDB1V0	GBB2/IO41PDB1V0	GBB2/IO31PDB2V0	GBB2/IO45PDB2V0				
D16	GCA2/IO32NDB1V0	IO41NDB1V0	IO31NDB2V0	IO45NDB2V0				
E1	GND	GND	GND	GND				
E2	GFB0/IO48NPB3V0	IO73NDB3V0	IO81NDB4V0	IO118NDB4V0				
E3	GFB2/IO50PPB3V0	IO73PDB3V0	IO81PDB4V0	IO118PDB4V0				
E4	VCCIB3	VCCIB3	VCCIB4	VCCIB4				
E5	NC	IO74NPB3V0	IO83NPB4V0	IO123NPB4V0				
E6	NC	IO08RSB0V0	IO04NPB0V0	IO05NPB0V1				
E7	GND	GND	GND	GND				
E8	NC	IO18RSB0V0	IO08PDB0V1	IO11PDB0V1				
E9	NC	NC	IO20NDB1V0	IO27NDB1V1				
E10	GND	GND	GND	GND				
E11	IO24RSB0V0	GBB1/IO37RSB0V0	GBB1/IO27PDB1V1	GBB1/IO41PDB1V2				
E12	NC	IO50PPB1V0	IO33PSB2V0	IO48PSB2V0				



Package Pin Assignments

FG256								
Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function				
H3	XTAL2	XTAL2	XTAL2	XTAL2				
H4	XTAL1	XTAL1	XTAL1	XTAL1				
H5	GNDOSC	GNDOSC	GNDOSC	GNDOSC				
H6	VCCOSC	VCCOSC	VCCOSC	VCCOSC				
H7	VCC	VCC	VCC	VCC				
H8	GND	GND	GND	GND				
H9	VCC	VCC	VCC	VCC				
H10	GND	GND	GND	GND				
H11	GDC0/IO38NDB1V0	IO51NDB1V0	IO47NDB2V0	IO69NDB2V0				
H12	GDC1/IO38PDB1V0	IO51PDB1V0	IO47PDB2V0	IO69PDB2V0				
H13	GDB1/IO39PDB1V0	GCA1/IO49PDB1V0	GCA1/IO45PDB2V0	GCA1/IO64PDB2V0				
H14	GDB0/IO39NDB1V0	GCA0/IO49NDB1V0	GCA0/IO45NDB2V0	GCA0/IO64NDB2V0				
H15	GCA0/IO36NDB1V0	GCB0/IO48NDB1V0	GCB0/IO44NDB2V0	GCB0/IO63NDB2V0				
H16	GCA1/IO36PDB1V0	GCB1/IO48PDB1V0	GCB1/IO44PDB2V0	GCB1/IO63PDB2V0				
J1	GEA0/IO44NDB3V0	GFA0/IO66NDB3V0	GFA0/IO70NDB4V0	GFA0/IO105NDB4V0				
J2	GEA1/IO44PDB3V0	GFA1/IO66PDB3V0	GFA1/IO70PDB4V0	GFA1/IO105PDB4V0				
J3	IO43NDB3V0	GFB0/IO67NDB3V0	GFB0/IO71NDB4V0	GFB0/IO106NDB4V0				
J4	GEC2/IO43PDB3V0	GFB1/IO67PDB3V0	GFB1/IO71PDB4V0	GFB1/IO106PDB4V0				
J5	NC	GFC0/IO68NDB3V0	GFC0/IO72NDB4V0	GFC0/IO107NDB4V0				
J6	NC	GFC1/IO68PDB3V0	GFC1/IO72PDB4V0	GFC1/IO107PDB4V0				
J7	GND	GND	GND	GND				
J8	VCC	VCC	VCC	VCC				
J9	GND	GND	GND	GND				
J10	VCC	VCC	VCC	VCC				
J11	GDC2/IO41NPB1V0	IO56NPB1V0	IO56NPB2V0	IO83NPB2V0				
J12	NC	GDB0/IO53NPB1V0	GDB0/IO53NPB2V0	GDB0/IO80NPB2V0				
J13	NC	GDA1/IO54PDB1V0	GDA1/IO54PDB2V0	GDA1/IO81PDB2V0				
J14	GDA0/IO40PDB1V0	GDC1/IO52PPB1V0	GDC1/IO52PPB2V0	GDC1/IO79PPB2V0				
J15	NC	IO50NPB1V0	IO51NSB2V0	IO77NSB2V0				
J16	GDA2/IO40NDB1V0	GDC0/IO52NPB1V0	GDC0/IO52NPB2V0	GDC0/IO79NPB2V0				
K1	NC	IO65NPB3V0	IO67NPB4V0	IO92NPB4V0				
K2	VCCIB3	VCCIB3	VCCIB4	VCCIB4				
K3	NC	IO65PPB3V0	IO67PPB4V0	IO92PPB4V0				
K4	NC	IO64PDB3V0	IO65PDB4V0	IO96PDB4V0				
K5	GND	GND	GND	GND				
K6	NC	IO64NDB3V0	IO65NDB4V0	IO96NDB4V0				
K7	VCC	VCC	VCC	VCC				
K8	GND	GND	GND	GND				

Revision	Changes	Page
v2.0, Revision 1 (continued)	The data in the 2.5 V LCMOS and LVCMOS 2.5 V / 5.0 V rows were updated in Table 2-75 \bullet Fusion Standard and Advanced I/O – Hot-Swap and 5 V Input Tolerance Capabilities.	2-143
	In Table 2-78 • Fusion Standard I/O Standards—OUT_DRIVE Settings, LVCMOS 1.5 V, for OUT_DRIVE 2, was changed from a dash to a check mark.	2-152
	The "VCC15A Analog Power Supply (1.5 V)" definition was changed from "A 1.5 V analog power supply input should be used to provide this input" to "1.5 V clean analog power supply input for use by the 1.5 V portion of the analog circuitry."	2-223
	In the "VCC33PMP Analog Power Supply (3.3 V)" pin description, the following text was changed from "VCC33PMP should be powered up before or simultaneously with VCC33A" to "VCC33PMP should be powered up simultaneously with or after VCC33A."	2-223
	The "VCCOSC Oscillator Power Supply (3.3 V)" section was updated to include information about when to power the pin.	2-223
	In the "128-Bit AES Decryption" section, FIPS-192 was incorrect and changed to FIPS-197.	2-228
	The note in Table 2-84 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications was updated.	2-156
	For 1.5 V LVCMOS, the VIL and VIH parameters, 0.30 * VCCI was changed to 0.35 * VCCI and 0.70 * VCCI was changed to 0.65 * VCCI in Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions, Table 2-87 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions, and Table 2-88 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions, and Table 2-88 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions, and Table 2-88 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions.	2-164 to 2-165
	In Table 2-87 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions, the VIH max column was updated.	
	Table 2-89 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions was updated to include notes 3 and 4. The temperature ranges were also updated in notes 1 and 2.	2-165
	The titles in Table 2-92 • Summary of I/O Timing Characteristics – Software Default Settings to Table 2-94 • Summary of I/O Timing Characteristics – Software Default Settings were updated to "VCCI = I/O Standard Dependent."	2-167 to 2-168
	Below Table 2-98 • I/O Short Currents IOSH/IOSL, the paragraph was updated to change 110°C to 100°C and three months was changed to six months.	2-172
	Table 2-99 • Short Current Event Duration before Failure was updated to remove110°C data.	2-174
	In Table 2-101 • I/O Input Rise Time, Fall Time, and Related I/O Reliability, LVTTL/LVCMOS rows were changed from 110°C to 100°C.	2-174
	VCC33PMP was added to Table 3-1 • Absolute Maximum Ratings. In addition, conditions for AV, AC, AG, and AT were also updated.	3-1
	VCC33PMP was added to Table 3-2 • Recommended Operating Conditions1. In addition, conditions for AV, AC, AG, and AT were also updated.	3-3
	Table 3-5 • FPGA Programming, Storage, and Operating Limits was updated to include new data and the temperature ranges were changed. The notes were removed from the table.	3-5