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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	119
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/afs600-2fg256i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Global Clocking

Fusion devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there are on-chip oscillators as well as a comprehensive global clock distribution network.

The integrated RC oscillator generates a 100 MHz clock. It is used internally to provide a known clock source to the flash memory read and write control. It can also be used as a source for the PLLs.

The crystal oscillator supports the following operating modes:

- Crystal (32.768 KHz to 20 MHz)
- Ceramic (500 KHz to 8 MHz)
- RC (32.768 KHz to 4 MHz)

Each VersaTile input and output port has access to nine VersaNets: six main and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via MUXes. The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

Digital I/Os with Advanced I/O Standards

The Fusion family of FPGAs features a flexible digital I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). Fusion FPGAs support many different digital I/O standards, both single-ended and differential.

The I/Os are organized into banks, with four or five banks per device. The configuration of these banks determines the I/O standards supported. The banks along the east and west sides of the device support the full range of I/O standards (single-ended and differential). The south bank supports the Analog Quads (analog I/O). In the family's two smaller devices, the north bank supports multiple single-ended digital I/O standards. In the family's larger devices, the north bank is divided into two banks of digital Pro I/Os, supporting a wide variety of single-ended, differential, and voltage-referenced I/O standards.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following applications:

- Single-Data-Rate (SDR) applications
- Double-Data-Rate (DDR) applications—DDR LVDS I/O for chip-to-chip communications
- Fusion banks support LVPECL, LVDS, BLVDS, and M-LVDS with 20 multi-drop points.

VersaTiles

The Fusion core consists of VersaTiles, which are also used in the successful ProASIC3 family. The Fusion VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set and optional enable

Refer to Figure 1-2 for the VersaTile configuration arrangement.







Figure 2-4 • Combinatorial Timing Model and Waveforms





Figure 2-9 • Efficient Long-Line Resources



Real-Time Counter (part of AB macro)

The RTC is a 40-bit loadable counter and used as the primary timekeeping element (Figure 2-29). The clock source, RTCCLK, must come from the CLKOUT signal of the crystal oscillator. The RTC can be configured to reset itself when a count value reaches the match value set in the Match Register.

The RTC is part of the Analog Block (AB) macro. The RTC is configured by the analog configuration MUX (ACM). Each address contains one byte of data. The circuitry in the RTC is powered by VCC33A, so the RTC can be used in standby mode when the 1.5 V supply is not present.



Figure 2-29 • RTC Block Diagram

Signal Name	Width	Direction	Function
RTCCLK	1	In	Must come from CLKOUT of XTLOSC.
RTCXTLMODE[1:0]	2	Out	Controlled by xt_mode in CTRL_STAT. Signal must connect to the RTC_MODE signal in XTLOSC, as shown in Figure 2-27.
RTCXTLSEL	1	Out	Controlled by xtal_en from CTRL_STAT register. Signal must connect to RTC_MODE signal in XTLOSC in Figure 2-27.
RTCMATCH	1	Out	Match signal for FPGA
			0 – Counter value does not equal the Match Register value.
			1 – Counter value equals the Match Register value.
RTCPSMMATCH	1	Out	Same signal as RTCMATCH. Signal must connect to RTCPSMMATCH in VRPSM, as shown in Figure 2-27.

The 40-bit counter can be preloaded with an initial value as a starting point by the Counter Register. The count from the 40-bit counter can be read through the same set of address space. The count comes from a Read-Hold Register to avoid data changing during read. When the counter value equals the Match Register value, all Match Bits Register values will be 0xFFFFFFFFF. The RTCMATCH and RTCPSMMATCH signals will assert. The 40-bit counter can be configured to automatically reset to 0x000000000 when the counter value equals the Match Register value. The automatic reset does not apply if the Match Register value is 0x000000000. The RTCCLK has a prescaler to divide the clock by 128 before it is used for the 40-bit counter. Below is an example of how to calculate the OFF time.

Flash Memory Block Diagram

A simplified diagram of the flash memory block is shown in Figure 2-33.





The logic consists of the following sub-blocks:

Flash Array

Contains all stored data. The flash array contains 64 sectors, and each sector contains 33 pages of data.

Page Buffer

A page-wide volatile register. A page contains 8 blocks of data and an AUX block.

- Block Buffer
 - Contains the contents of the last block accessed. A block contains 128 data bits.
- ECC Logic

The FB stores error correction information with each block to perform single-bit error correction and double-bit error detection on all data blocks.

Channel Input Offset Error

Channel Offset error is measured as the input voltage that causes the transition from zero to a count of one. An Ideal Prescaler will have offset equal to $\frac{1}{2}$ of LSB voltage. Offset error is a positive or negative when the first transition point is higher or lower than ideal. Offset error is expressed in LSB or input voltage.

Total Channel Error

Total Channel Error is defined as the total error measured compared to the ideal value. Total Channel Error is the sum of gain error and offset error combined. Figure 2-68 shows how Total Channel Error is measured.

Total Channel Error is defined as the difference between the actual ADC output and ideal ADC output. In the example shown in Figure 2-68, the Total Channel Error would be a negative number.



Figure 2-68 • Total Channel Error Example



Direct Digital Input

The AV, AC, and AT pads can also be configured as high-voltage digital inputs (Figure 2-69). As these pads are 12 V–tolerant, the digital input can also be up to 12 V. However, the frequency at which these pads can operate is limited to 10 MHz.

To enable one of these analog input pads to operate as a digital input, its corresponding Digital Input Enable (DENAxy) pin on the Analog Block must be pulled High, where x is either V, C, or T (for AV, AC, or AT pads, respectively) and y is in the range 0 to 9, corresponding to the appropriate Analog Quad.

When the pad is configured as a digital input, the signal will come out of the Analog Block macro on the appropriate DAxOUTy pin, where x represents the pad type (V for AV pad, C for AC pad, or T for AT pad) and y represents the appropriate Analog Quad number. Example: If the AT pad in Analog Quad 5 is configured as a digital input, it will come out on the DATOUT5 pin of the Analog Block macro.



Figure 2-69 • Analog Quad Direct Digital Input Configuration



Device Architecture

ADC Description

The Fusion ADC is a 12-bit SAR ADC. It offers a wide variety of features for different use models. Figure 2-80 shows a block diagram of the Fusion ADC.

- · Configurable resolution: 8-bit, 10-bit, and 12-bit mode
- DNL: 0.6 LSB for 10-bit mode
- INL: 0.4 LSB for 10-bit mode
- No missing code
- Internal VAREF = 2.56 V
- Maximum Sample Rate = 600 Ksps
- Power-up calibration and dynamic calibration after every sample to compensate for temperature drift over time



Figure 2-80 • ADC Simplified Block Diagram

ADC Theory of Operation

An analog-to-digital converter is used to capture discrete samples of a continuous analog voltage and provide a discrete binary representation of the signal. Analog-to-digital converters are generally characterized in three ways:

- Input voltage range
- Resolution
- Bandwidth or conversion rate

The input voltage range of an ADC is determined by its reference voltage (VREF). Fusion devices include an internal 2.56 V reference, or the user can supply an external reference of up to 3.3 V. The following examples use the internal 2.56 V reference, so the full-scale input range of the ADC is 0 to 2.56 V.

The resolution (LSB) of the ADC is a function of the number of binary bits in the converter. The ADC approximates the value of the input voltage using 2n steps, where n is the number of bits in the converter. Each step therefore represents VREF÷ 2n volts. In the case of the Fusion ADC configured for 12-bit operation, the LSB is 2.56 V / 4096 = 0.625 mV.

Finally, bandwidth is an indication of the maximum number of conversions the ADC can perform each second. The bandwidth of an ADC is constrained by its architecture and several key performance characteristics.

INL – Integral Non-Linearity

INL is the deviation of an actual transfer function from a straight line. After nullifying offset and gain errors, the straight line is either a best-fit straight line or a line drawn between the end points of the transfer function (Figure 2-85).

Figure 2-85 • Integral Non-Linearity (INL)

LSB – Least Significant Bit

In a binary number, the LSB is the least weighted bit in the group. Typically, the LSB is the furthest right bit. For an ADC, the weight of an LSB equals the full-scale voltage range of the converter divided by 2^N , where N is the converter's resolution.

EQ 13 shows the calculation for a 10-bit ADC with a unipolar full-scale voltage of 2.56 V:

EQ 13

No Missing Codes

An ADC has no missing codes if it produces all possible digital codes in response to a ramp signal applied to the analog input.

Typical Performance Characteristics

Temperature Errror vs. Die Temperature

Figure 2-95 • Effect of External Sensor Capacitance

Device Architecture

Table 2-50 • ADC Characteristics in Direct Input Mode (continued)

Commercial Temperature Range Conditions, $T_J = 85^{\circ}C$ (unless noted otherwise), Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Тур.	Max.	Units
Dynamic Pe	erformance					
SNR	Signal-to-Noise Ratio	8-bit mode	48.0	49.5		dB
		10-bit mode	58.0	60.0		dB
		12-bit mode	62.9	64.5		dB
SINAD	Signal-to-Noise Distortion	8-bit mode	47.6	49.5		dB
		10-bit mode	57.4	59.8		dB
		12-bit mode	62.0	64.2		dB
THD	Total Harmonic Distortion	8-bit mode		-74.4	-63.0	dBc
		10-bit mode		-78.3	-63.0	dBc
		12-bit mode		-77.9	-64.4	dBc
ENOB	Effective Number of Bits	8-bit mode	7.6	7.9		bits
		10-bit mode	9.5	9.6		bits
		12-bit mode	10.0	10.4		bits
Conversion	Rate					
	Conversion Time	8-bit mode	1.7			μs
		10-bit mode	1.8			μs
		12-bit mode	2			μs
	Sample Rate	8-bit mode			600	Ksps
		10-bit mode			550	Ksps
		12-bit mode			500	Ksps

Notes:

1. Accuracy of the external reference is 2.56 V \pm 4.6 mV.

2. Data is based on characterization.

3. The sample rate is time-shared among active analog inputs.

Table 2-57 details the settings available to control the prescaler values of the AV, AC, and AT pins. Note that the AT pin has a reduced number of available prescaler values.

Control Lines Bx[2:0]	Scaling Factor, Pad to ADC Input	LSB for an 8-Bit Conversion ¹ (mV)	LSB for a 10-Bit Conversion ¹ (mV)	LSB for a 12-Bit Conversion ¹ (mV)	Full-Scale Voltage in 10-Bit Mode ²	Range Name
000 ³	0.15625	64	16	4	16.368 V	16 V
001	0.3125	32	8	2	8.184 V	8 V
010 ³	0.625	16	4	1	4.092 V	4 V
011	1.25	8	2	0.5	2.046 V	2 V
100	2.5	4	1	0.25	1.023 V	1 V
101	5.0	2	0.5	0.125	0.5115 V	0.5 V
110	10.0	1	0.25	0.0625	0.25575 V	0.25 V
111	20.0	0.5	0.125	0.03125	0.127875 V	0.125 V

Table 2-57 • Prescaler Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)

Notes:

1. LSB voltage equivalences assume VAREF = 2.56 V.

2. Full Scale voltage for n-bit mode: ((2ⁿ) - 1) x (LSB for a n-bit Conversion)

3. These are the only valid ranges for the Temperature Monitor Block Prescaler.

Table 2-58 details the settings available to control the MUX within each of the AV, AC, and AT circuits. This MUX determines whether the signal routed to the ADC is the direct analog input, prescaled signal, or output of either the Current Monitor Block or the Temperature Monitor Block.

Table 2-58 • Analog Multiplexer Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)

Control Lines Bx[4]	Control Lines Bx[3]	ADC Connected To
0	0	Prescaler
0	1	Direct input
1	0	Current amplifier temperature monitor
1	1	Not valid

Table 2-59 details the settings available to control the Direct Analog Input switch for the AV, AC, and AT pins.

Table 2-59 • Direct Analog Input Switch Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)

Control Lines Bx[5]	Direct Input Switch
0	Off
1	On

Table 2-60 details the settings available to control the polarity of the signals coming to the AV, AC, and AT pins. Note that the only valid setting for the AT pin is logic 0 to support positive voltages.

Table 2-60 • Voltage Polarity Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)*

Control Lines Bx[6]	Input Signal Polarity
0	Positive
1	Negative

Note: *The B3[6] signal for the AT pad should be kept at logic 0 to accept only positive voltages.

Detailed I/O DC Characteristics

Table 2-95 • Input Capacitance

Symbol	Definition Conditions Min.		Min.	Max.	Units
C _{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C _{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

Table 2-96 • I/O Output Buffer Maximum Resistances ¹

Drive Strength	R _{PULL-DOWN} (ohms) ²	R _{PULL-UP} (ohms) ³
4 mA	100	300
8 mA	50	150
12 mA	25	75
16 mA	17	50
24 mA	11	33
4 mA	100	200
8 mA	50	100
12 mA	25	50
16 mA	20	40
24 mA	11	22
2 mA	200	225
4 mA	100	112
6 mA	50	56
8 mA	50	56
12 mA	20	22
16 mA	20	22
2 mA	200	224
4 mA	100	112
6 mA	67	75
8 mA	33	37
12 mA	33	37
Per PCI/PCI-X specification	25	75
20 mA	11	-
20 mA	14	-
35 mA	12	-
33 mA	15	_
	Drive Strength 4 mA 8 mA 12 mA 16 mA 24 mA 4 mA 8 mA 12 mA 16 mA 24 mA 4 mA 8 mA 12 mA 16 mA 24 mA 6 mA 8 mA 112 mA 16 mA 2 mA 4 mA 6 mA 8 mA 12 mA 16 mA 8 mA 12 mA 12 mA 13 mA Per PCI/PCI-X specification 20 mA 35 mA 33 mA	Drive Strength "PULL-DOWN (ohms) 2" 4 mA 100 8 mA 50 12 mA 25 16 mA 17 24 mA 11 4 mA 100 8 mA 50 12 mA 25 16 mA 11 4 mA 100 8 mA 50 12 mA 25 16 mA 20 24 mA 11 2 mA 200 4 mA 100 6 mA 50 12 mA 20 16 mA 20 2 mA 200 4 mA 100 6 mA 50 12 mA 20 2 mA 200 4 mA 100 6 mA 67 8 mA 33 12 mA 33 Per PCI/PCI-X specification 25 20 mA 11 20 mA 14 <

Notes:

 These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/techdocs/models/ibis.html.

2. R_(PULL-DOWN-MAX) = VOLspec / I_{OLspec}

3. R_(PULL-UP-MAX) = (VCCImax – VOHspec) / IOHspec

Device Architecture

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-156 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class I		VIL	VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
15 mA	-0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15	87	83	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

Figure 2-130 • AC Loading

Table 2-157	•	AC Waveforms.	Measuring Po	ints. and Ca	pacitive Loads
		Ao marononino,	mououring i o	millo, ama oaj	

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-158 • SSTL 2 Class I

```
Commercial Temperature Range Conditions: T_J = 70^{\circ}C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V
```

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{zLS}	t _{zHS}	Units
Std.	0.66	2.13	0.04	1.33	0.43	2.17	1.85			4.40	4.08	ns
-1	0.56	1.81	0.04	1.14	0.36	1.84	1.57			3.74	3.47	ns
-2	0.49	1.59	0.03	1.00	0.32	1.62	1.38			3.29	3.05	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

connected to the internal core logic I/O tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

Figure 2-146 • Boundary Scan Chain in Fusion

Table 2-185 • Boundary Scan Opcodes

	Hex Opcode
EXTEST	00
HIGHZ	07
USERCODE	0E
SAMPLE/PRELOAD	01
IDCODE	0F
CLAMP	05
BYPASS	FF

Symbol	Parameter ²		Commercial	Industrial	Units
Τ _J	Junction temperature		0 to +85	-40 to +100	°C
VCC	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage	Programming mode ³	3.15 to 3.45	3.15 to 3.45	V
		Operation ⁴	0 to 3.6	0 to 3.6	V
VCCPLL	Analog power supply (PLL)		1.425 to 1.575	1.425 to 1.575	V
VCCI	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V
VCC33A	+3.3 V power supply		2.97 to 3.63	2.97 to 3.63	V
VCC33PMP	+3.3 V power supply		2.97 to 3.63	2.97 to 3.63	V
VAREF	Voltage reference for ADC	2.527 to 2.593	2.527 to 2.593	V	
VCC15A ⁵	Digital power supply for the analog system		1.425 to 1.575	1.425 to 1.575	V
VCCNVM	Embedded flash power supply		1.425 to 1.575	1.425 to 1.575	V
VCCOSC	Oscillator power supply		2.97 to 3.63	2.97 to 3.63	V
AV, AC ⁶	Unpowered, ADC reset asserted or	unconfigured	-10.5 to 12.0	-10.5 to 11.6	V
	Analog input (+16 V to +2 V presca	ller range)	-0.3 to 12.0	–0.3 to 11.6	V
	Analog input (+1 V to + 0.125 V pre	escaler range)	-0.3 to 3.6	-0.3 to 3.6	V
	Analog input (–16 V to –2 V presca	ler range)	-10.5 to 0.3	-10.5 to 0.3	V
	Analog input (–1 V to –0.125 V pres	scaler range)	-3.6 to 0.3	-3.6 to 0.3	V
	Analog input (direct input to ADC)		-0.3 to 3.6	-0.3 to 3.6	V
	Digital input		-0.3 to 12.0	–0.3 to 11.6	V
AG ⁶	Unpowered, ADC reset asserted or	unconfigured	-10.5 to 12.0	-10.5 to 11.6	V
	Low Current Mode (1 µA, 3 µA, 10	μΑ, 30 μΑ)	-0.3 to 12.0	–0.3 to 11.6	V
	Low Current Mode (–1 µA, –3 µA, -	-10.5 to 0.3	-10.5 to 0.3	V	
	High Current Mode ⁷		-10.5 to 12.0	-10.5 to 11.6	V
AT ⁶	Unpowered, ADC reset asserted or	unconfigured	-0.3 to 15.5	–0.3 to 14.5	V
	Analog input (+16 V, +4 V prescale	r range)	-0.3 to 15.5	–0.3 to 14.5	V
	Analog input (direct input to ADC)	-0.3 to 3.6	-0.3 to 3.6	V	
	Digital input		-0.3 to 15.5	-0.3 to 14.5	V

Table 3-2 • Recommended Operating Conditions¹

Notes:

1. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-85 on page 2-157.

- 2. All parameters representing voltages are measured with respect to GND unless otherwise specified.
- 3. The programming temperature range supported is $T_{ambient} = 0^{\circ}C$ to 85°C.
- 4. VPUMP can be left floating during normal operation (not programming mode).
- 5. Violating the V_{CC15A} recommended voltage supply during an embedded flash program cycle can corrupt the page being programmed.
- 6. The input voltage may overshoot by up to 500 mV above the Recommended Maximum (150 mV in Direct mode), provided the duration of the overshoot is less than 50% of the operating lifetime of the device.
- 7. The AG pad should also conform to the limits as specified in Table 2-48 on page 2-114.

Power per I/O Pin

Table 3-12 • Summary of I/O Input Buffer Power (per pin)—Default I/O Software Settings

	VCCI (V)	Static Power PDC7 (mW) ¹	Dynamic Power PAC9 (µW/MHz) ²
Applicable to Pro I/O Banks	<u> </u>		
Single-Ended			
3.3 V LVTTL/LVCMOS	3.3		17.39
3.3 V LVTTL/LVCMOS – Schmitt trigger	3.3	_	25.51
2.5 V LVCMOS	2.5	_	5.76
2.5 V LVCMOS – Schmitt trigger	2.5	_	7.16
1.8 V LVCMOS	1.8	_	2.72
1.8 V LVCMOS – Schmitt trigger	1.8	_	2.80
1.5 V LVCMOS (JESD8-11)	1.5	_	2.08
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	_	2.00
3.3 V PCI	3.3	_	18.82
3.3 V PCI – Schmitt trigger	3.3	_	20.12
3.3 V PCI-X	3.3	_	18.82
3.3 V PCI-X – Schmitt trigger	3.3	_	20.12
Voltage-Referenced	<u></u>		
3.3 V GTL	3.3	2.90	8.23
2.5 V GTL	2.5	2.13	4.78
3.3 V GTL+	3.3	2.81	4.14
2.5 V GTL+	2.5	2.57	3.71
HSTL (I)	1.5	0.17	2.03
HSTL (II)	1.5	0.17	2.03
SSTL2 (I)	2.5	1.38	4.48
SSTL2 (II)	2.5	1.38	4.48
SSTL3 (I)	3.3	3.21	9.26
SSTL3 (II)	3.3	3.21	9.26
Differential	<u>.</u>		•
LVDS	2.5	2.26	1.50
LVPECL	3.3	5.71	2.17

Notes:

1. PDC7 is the static power (where applicable) measured on VCCI.

2. PAC9 is the total dynamic power measured on VCC and VCCI.

FG256						
Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function		
C7	IO09RSB0V0	IO12RSB0V0	IO06NDB0V0	IO09NDB0V1		
C8	IO14RSB0V0	IO22RSB0V0	IO16PDB1V0	IO23PDB1V0		
C9	IO15RSB0V0	IO23RSB0V0	IO16NDB1V0	IO23NDB1V0		
C10	IO22RSB0V0	IO30RSB0V0	IO25NDB1V1	IO31NDB1V1		
C11	IO20RSB0V0	IO31RSB0V0	IO25PDB1V1	IO31PDB1V1		
C12	VCCIB0	VCCIB0	VCCIB1	VCCIB1		
C13	GBB1/IO28RSB0V0	GBC1/IO35RSB0V0	GBC1/IO26PPB1V1	GBC1/IO40PPB1V2		
C14	VCCIB1	VCCIB1	VCCIB2	VCCIB2		
C15	GND	GND	GND	GND		
C16	VCCIB1	VCCIB1	VCCIB2	VCCIB2		
D1	GFC2/IO50NPB3V0	IO75NDB3V0	IO84NDB4V0	IO124NDB4V0		
D2	GFA2/IO51NDB3V0	GAB2/IO75PDB3V0	GAB2/IO84PDB4V0	GAB2/IO124PDB4V0		
D3	GAC2/IO51PDB3V0	IO76NDB3V0	IO85NDB4V0	IO125NDB4V0		
D4	GAA2/IO52PDB3V0	GAA2/IO76PDB3V0	GAA2/IO85PDB4V0	GAA2/IO125PDB4V0		
D5	GAB2/IO52NDB3V0	GAB0/IO02RSB0V0	GAB0/IO02NPB0V0	GAB0/IO02NPB0V0		
D6	GAC0/IO04RSB0V0	GAC0/IO04RSB0V0	GAC0/IO03NDB0V0	GAC0/IO03NDB0V0		
D7	IO08RSB0V0	IO13RSB0V0	IO06PDB0V0	IO09PDB0V1		
D8	NC	IO20RSB0V0	IO14NDB0V1	IO15NDB0V2		
D9	NC	IO21RSB0V0	IO14PDB0V1	IO15PDB0V2		
D10	IO21RSB0V0	IO28RSB0V0	IO23PDB1V1	IO37PDB1V2		
D11	IO23RSB0V0	GBB0/IO36RSB0V0	GBB0/IO27NDB1V1	GBB0/IO41NDB1V2		
D12	NC	NC	VCCIB1	VCCIB1		
D13	GBA2/IO31PDB1V0	GBA2/IO40PDB1V0	GBA2/IO30PDB2V0	GBA2/IO44PDB2V0		
D14	GBB2/IO31NDB1V0	IO40NDB1V0	IO30NDB2V0	IO44NDB2V0		
D15	GBC2/IO32PDB1V0	GBB2/IO41PDB1V0	GBB2/IO31PDB2V0	GBB2/IO45PDB2V0		
D16	GCA2/IO32NDB1V0	IO41NDB1V0	IO31NDB2V0	IO45NDB2V0		
E1	GND	GND	GND	GND		
E2	GFB0/IO48NPB3V0	IO73NDB3V0	IO81NDB4V0	IO118NDB4V0		
E3	GFB2/IO50PPB3V0	IO73PDB3V0	IO81PDB4V0	IO118PDB4V0		
E4	VCCIB3	VCCIB3	VCCIB4	VCCIB4		
E5	NC	IO74NPB3V0	IO83NPB4V0	IO123NPB4V0		
E6	NC	IO08RSB0V0	IO04NPB0V0	IO05NPB0V1		
E7	GND	GND	GND	GND		
E8	NC	IO18RSB0V0	IO08PDB0V1	IO11PDB0V1		
E9	NC	NC	IO20NDB1V0	IO27NDB1V1		
E10	GND	GND	GND	GND		
E11	IO24RSB0V0	GBB1/IO37RSB0V0	GBB1/IO27PDB1V1	GBB1/IO41PDB1V2		
E12	NC	IO50PPB1V0	IO33PSB2V0	IO48PSB2V0		

FG256						
Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function		
E13	VCCIB1	VCCIB1	VCCIB2	VCCIB2		
E14	GCC2/IO33NDB1V0	IO42NDB1V0	IO32NDB2V0	IO46NDB2V0		
E15	GCB2/IO33PDB1V0	GBC2/IO42PDB1V0	GBC2/IO32PDB2V0	GBC2/IO46PDB2V0		
E16	GND	GND	GND	GND		
F1	NC	NC	IO79NDB4V0	IO111NDB4V0		
F2	NC	NC	IO79PDB4V0	IO111PDB4V0		
F3	GFB1/IO48PPB3V0	IO72NDB3V0	IO76NDB4V0	IO112NDB4V0		
F4	GFC0/IO49NDB3V0	IO72PDB3V0	IO76PDB4V0	IO112PDB4V0		
F5	NC	NC	IO82PSB4V0	IO120PSB4V0		
F6	GFC1/IO49PDB3V0	GAC2/IO74PPB3V0	GAC2/IO83PPB4V0	GAC2/IO123PPB4V0		
F7	NC	IO09RSB0V0	IO04PPB0V0	IO05PPB0V1		
F8	NC	IO19RSB0V0	IO08NDB0V1	IO11NDB0V1		
F9	NC	NC	IO20PDB1V0	IO27PDB1V1		
F10	NC	IO29RSB0V0	IO23NDB1V1	IO37NDB1V2		
F11	NC	IO43NDB1V0	IO36NDB2V0	IO50NDB2V0		
F12	NC	IO43PDB1V0	IO36PDB2V0	IO50PDB2V0		
F13	NC	IO44NDB1V0	IO39NDB2V0	IO59NDB2V0		
F14	NC	GCA2/IO44PDB1V0	GCA2/IO39PDB2V0	GCA2/IO59PDB2V0		
F15	GCC1/IO34PDB1V0	GCB2/IO45PDB1V0	GCB2/IO40PDB2V0	GCB2/IO60PDB2V0		
F16	GCC0/IO34NDB1V0	IO45NDB1V0	IO40NDB2V0	IO60NDB2V0		
G1	GEC0/IO46NPB3V0	IO70NPB3V0	IO74NPB4V0	IO109NPB4V0		
G2	VCCIB3	VCCIB3	VCCIB4	VCCIB4		
G3	GEC1/IO46PPB3V0	GFB2/IO70PPB3V0	GFB2/IO74PPB4V0	GFB2/IO109PPB4V0		
G4	GFA1/IO47PDB3V0	GFA2/IO71PDB3V0	GFA2/IO75PDB4V0	GFA2/IO110PDB4V0		
G5	GND	GND	GND	GND		
G6	GFA0/IO47NDB3V0	IO71NDB3V0	IO75NDB4V0	IO110NDB4V0		
G7	GND	GND	GND	GND		
G8	VCC	VCC	VCC	VCC		
G9	GND	GND	GND	GND		
G10	VCC	VCC	VCC	VCC		
G11	GDA1/IO37NDB1V0	GCC0/IO47NDB1V0	GCC0/IO43NDB2V0	GCC0/IO62NDB2V0		
G12	GND	GND	GND	GND		
G13	IO37PDB1V0	GCC1/IO47PDB1V0	GCC1/IO43PDB2V0	GCC1/IO62PDB2V0		
G14	GCB0/IO35NPB1V0	IO46NPB1V0	IO41NPB2V0	IO61NPB2V0		
G15	VCCIB1	VCCIB1	VCCIB2	VCCIB2		
G16	GCB1/IO35PPB1V0	GCC2/IO46PPB1V0	GCC2/IO41PPB2V0	GCC2/IO61PPB2V0		
H1	GEB1/IO45PDB3V0	GFC2/IO69PDB3V0	GFC2/IO73PDB4V0	GFC2/IO108PDB4V0		
H2	GEB0/IO45NDB3V0	IO69NDB3V0	IO73NDB4V0	IO108NDB4V0		

Datasheet Information

Revision	Changes	Page
Advance v1.0 (continued)	This change table states that in the "208-Pin PQFP" table listed under the Advance v0.8 changes, the AFS090 device had a pin change. That is incorrect. Pin 102 was updated for AFS250 and AFS600. The function name changed from $V_{CC33ACAP}$ to V_{CC33A} .	3-8
Advance v0.9 (October 2007)	In the "Package I/Os: Single-/Double-Ended (Analog)" table, the AFS1500/M7AFS1500 I/O counts were updated for the following devices: FG484: 223/109 FG676: 252/126	II
	In the "108-Pin QFN" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pin: B25	3-2
	In the "180-Pin QFN" table, the function changed from V _{CC33ACAP} to V _{CC33A} for the following pins: AFS090: B29 AFS250: B29	3-4
	In the "208-Pin PQFP" table, the function changed from V _{CC33ACAP} to V _{CC33A} for the following pins: AFS090: 102 AFS250: 102	3-8
	In the "256-Pin FBGA" table, the function changed from $V_{CC33ACAP}$ to V_{CC33A} for the following pins: AFS090: T14 AFS250: T14 AFS600: T14 AFS1500: T14	3-12
Advance v0.9 (continued)	In the "484-Pin FBGA" table, the function changed from V _{CC33ACAP} to V _{CC33A} for the following pins: AFS600: AB18 AFS1500: AB18	3-20
	In the "676-Pin FBGA" table, the function changed from V _{CC33ACAP} to V _{CC33A} for the following pins: AFS1500: AD20	3-28
Advance v0.8 (June 2007)	Figure 2-16 • Fusion Clocking Options and the "RC Oscillator" section were updated to change GND_OSC and VCC_OSC to GNDOSC and VCCOSC.	2-20, 2-21
	Figure 2-19 • Fusion CCC Options: Global Buffers with the PLL Macro was updated to change the positions of OADIVRST and OADIVHALF, and a note was added.	2-25
	The "Crystal Oscillator" section was updated to include information about controlling and enabling/disabling the crystal oscillator.	2-22
	Table 2-11 \cdot Electrical Characteristics of the Crystal Oscillator was updated to change the typical value of I _{DYNXTAL} for 0.032–0.2 MHz to 0.19.	2-24
	The "1.5 V Voltage Regulator" section was updated to add "or floating" in the paragraph stating that an external pull-down is required on TRST to power down the VR.	2-41
	The "1.5 V Voltage Regulator" section was updated to include information on powering down with the VR.	2-41