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#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

| Product Status                 | Active  |
|--------------------------------|---|
| Number of LABs/CLBs            | -   |
| Number of Logic Elements/Cells | -   |
| Total RAM Bits                 | 110592  |
| Number of I/O                  | 119   |
| Number of Gates                | 600000  |
| Voltage - Supply               | 1.425V ~ 1.575V   |
| Mounting Type                  | Surface Mount   |
| Operating Temperature          | -40°C ~ 100°C (TJ)  |
| Package / Case                 | 256-LBGA  |
| Supplier Device Package        | 256-FPBGA (17x17)   |
| Purchase URL                   | https://www.e-xfl.com/product-detail/microchip-technology/afs600-2fgg256i |
|                                |   |

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# **Fusion Device Architecture Overview**



Figure 1 • Fusion Device Architecture Overview (AFS600)

# Package I/Os: Single-/Double-Ended (Analog)

| Fusion Devices        | AFS090     | AFS250                | AFS600                | AFS1500                |
|-----------------------|------------|-----------------------|-----------------------|------------------------|
| ARM Cortex-M1 Devices |            | M1AFS250              | M1AFS600              | M1AFS1500              |
| Pigeon Point Devices  |            |                       | P1AFS600 <sup>1</sup> | P1AFS1500 <sup>1</sup> |
| MicroBlade Devices    |            | U1AFS250 <sup>2</sup> | U1AFS600 <sup>2</sup> | U1AFS1500 <sup>2</sup> |
| QN108 <sup>3</sup>    | 37/9 (16)  |                       |                       |                        |
| QN180 <sup>3</sup>    | 60/16 (20) | 65/15 (24)            |                       |                        |
| PQ208 <sup>4</sup>    |            | 93/26 (24)            | 95/46 (40)            |                        |
| FG256                 | 75/22 (20) | 114/37 (24)           | 119/58 (40)           | 119/58 (40)            |
| FG484                 |            |                       | 172/86 (40)           | 223/109 (40)           |
| FG676                 |            |                       |                       | 252/126 (40)           |
| Notes:                | •          | 1                     |                       | •                      |

1. Pigeon Point devices are only offered in FG484 and FG256.

2. MicroBlade devices are only offered in FG256.

3. Package not available.

4. Fusion devices in the same package are pin compatible with the exception of the PQ208 package (AFS250 and AFS600).





Figure 2-73 • Negative Current Monitor

#### Terminology

#### Accuracy

The accuracy of Fusion Current Monitor is  $\pm 2 \text{ mV}$  minimum plus 5% of the differential voltage at the input. The input accuracy can be translated to error at the ADC output by using EQ 4. The 10 V/V gain is the gain of the Current Monitor Circuit, as described in the "Current Monitor" section on page 2-86. For 8-bit mode, N = 8,  $V_{AREF} = 2.56$  V, zero differential voltage between AV and AC, the Error ( $E_{ADC}$ ) is equal to 2 LSBs.

$$E_{ADC} = (2mV + 0.05 |V_{AV} - V_{AC}|) \times (10V) / V \times \frac{2^N}{V_{AREF}}$$

EQ 4

where

N is the number of bits

 $V_{AREF}$  is the Reference voltage

 $V_{AV}$  is the voltage at AV pad

V<sub>AC</sub> is the voltage at AC pad



This process results in a binary approximation of VIN. Generally, there is a fixed interval T, the sampling period, between the samples. The inverse of the sampling period is often referred to as the sampling frequency  $f_S = 1 / T$ . The combined effect is illustrated in Figure 2-82.



#### Figure 2-82 • Conversion Example

Figure 2-82 demonstrates that if the signal changes faster than the sampling rate can accommodate, or if the actual value of VIN falls between counts in the result, this information is lost during the conversion. There are several techniques that can be used to address these issues.

First, the sampling rate must be chosen to provide enough samples to adequately represent the input signal. Based on the Nyquist-Shannon Sampling Theorem, the minimum sampling rate must be at least twice the frequency of the highest frequency component in the target signal (Nyquist Frequency). For example, to recreate the frequency content of an audio signal with up to 22 KHz bandwidth, the user must sample it at a minimum of 44 ksps. However, as shown in Figure 2-82, significant post-processing of the data is required to interpolate the value of the waveform during the time between each sample.

Similarly, to re-create the amplitude variation of a signal, the signal must be sampled with adequate resolution. Continuing with the audio example, the dynamic range of the human ear (the ratio of the amplitude of the threshold of hearing to the threshold of pain) is generally accepted to be 135 dB, and the dynamic range of a typical symphony orchestra performance is around 85 dB. Most commercial recording media provide about 96 dB of dynamic range using 16-bit sample resolution. But 16-bit fidelity does not necessarily mean that you need a 16-bit ADC. As long as the input is sampled at or above the Nyquist Frequency, post-processing techniques can be used to interpolate intermediate values and reconstruct the original input signal to within desired tolerances.

If sophisticated digital signal processing (DSP) capabilities are available, the best results are obtained by implementing a reconstruction filter, which is used to interpolate many intermediate values with higher resolution than the original data. Interpolating many intermediate values increases the effective number of samples, and higher resolution increases the effective number of bits in the sample. In many cases, however, it is not cost-effective or necessary to implement such a sophisticated reconstruction algorithm. For applications that do not require extremely fine reproduction of the input signal, alternative methods can enhance digital sampling results with relatively simple post-processing. The details of such techniques are out of the scope of this chapter; refer to the *Improving ADC Results through Oversampling and Post-Processing of Data* white paper for more information.



Device Architecture

#### Gain Error

The gain error of an ADC indicates how well the slope of an actual transfer function matches the slope of the ideal transfer function. Gain error is usually expressed in LSB or as a percent of full-scale (%FSR). Gain error is the full-scale error minus the offset error (Figure 2-84).



Figure 2-84 • Gain Error

#### Gain Error Drift

Gain-error drift is the variation in gain error due to a change in ambient temperature, typically expressed in ppm/°C.

# **Timing Characteristics**

# Table 2-55 • Analog Configuration Multiplexer (ACM) TimingCommercial Temperature Range Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

| Parameter               | Description  | -2    | -1    | Std.  | Units |
|-------------------------|--|-------|-------|-------|-------|
| t <sub>CLKQACM</sub>    | Clock-to-Q of the ACM                              | 19.73 | 22.48 | 26.42 | ns    |
| t <sub>SUDACM</sub>     | Data Setup time for the ACM                        | 4.39  | 5.00  | 5.88  | ns    |
| t <sub>HDACM</sub>      | Data Hold time for the ACM                         | 0.00  | 0.00  | 0.00  | ns    |
| t <sub>SUAACM</sub>     | Address Setup time for the ACM                     | 4.73  | 5.38  | 6.33  | ns    |
| t <sub>HAACM</sub>      | Address Hold time for the ACM                      | 0.00  | 0.00  | 0.00  | ns    |
| t <sub>SUEACM</sub>     | Enable Setup time for the ACM                      | 3.93  | 4.48  | 5.27  | ns    |
| t <sub>HEACM</sub>      | Enable Hold time for the ACM                       | 0.00  | 0.00  | 0.00  | ns    |
| t <sub>MPWARACM</sub>   | Asynchronous Reset Minimum Pulse Width for the ACM | 10.00 | 10.00 | 10.00 | ns    |
| t <sub>REMARACM</sub>   | Asynchronous Reset Removal time for the ACM        | 12.98 | 14.79 | 17.38 | ns    |
| t <sub>RECARACM</sub>   | Asynchronous Reset Recovery time for the ACM       | 12.98 | 14.79 | 17.38 | ns    |
| t <sub>MPWCLKACM</sub>  | Clock Minimum Pulse Width for the ACM              | 45.00 | 45.00 | 45.00 | ns    |
| t <sub>FMAXCLKACM</sub> | lock Maximum Frequency for the ACM                 | 10.00 | 10.00 | 10.00 | MHz   |

Table 2-57 details the settings available to control the prescaler values of the AV, AC, and AT pins. Note that the AT pin has a reduced number of available prescaler values.

| Control Lines<br>Bx[2:0] | Scaling<br>Factor, Pad to<br>ADC Input | LSB for an<br>8-Bit<br>Conversion <sup>1</sup><br>(mV) | LSB for a<br>10-Bit<br>Conversion <sup>1</sup><br>(mV) | LSB for a<br>12-Bit<br>Conversion <sup>1</sup><br>(mV) | Full-Scale<br>Voltage in<br>10-Bit<br>Mode <sup>2</sup> | Range Name |
|--------------------------|--|--|--|--|---|------------|
| 000 <sup>3</sup>         | 0.15625                                | 64   | 16   | 4  | 16.368 V  | 16 V       |
| 001                      | 0.3125                                 | 32   | 8  | 2  | 8.184 V   | 8 V        |
| 010 <sup>3</sup>         | 0.625                                  | 16   | 4  | 1  | 4.092 V   | 4 V        |
| 011                      | 1.25                                   | 8  | 2  | 0.5  | 2.046 V   | 2 V        |
| 100                      | 2.5                                    | 4  | 1  | 0.25   | 1.023 V   | 1 V        |
| 101                      | 5.0                                    | 2  | 0.5  | 0.125  | 0.5115 V  | 0.5 V      |
| 110                      | 10.0                                   | 1  | 0.25   | 0.0625   | 0.25575 V   | 0.25 V     |
| 111                      | 20.0                                   | 0.5  | 0.125  | 0.03125  | 0.127875 V  | 0.125 V    |

Table 2-57 • Prescaler Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)

Notes:

1. LSB voltage equivalences assume VAREF = 2.56 V.

2. Full Scale voltage for n-bit mode: ((2<sup>n</sup>) - 1) x (LSB for a n-bit Conversion)

3. These are the only valid ranges for the Temperature Monitor Block Prescaler.

Table 2-58 details the settings available to control the MUX within each of the AV, AC, and AT circuits. This MUX determines whether the signal routed to the ADC is the direct analog input, prescaled signal, or output of either the Current Monitor Block or the Temperature Monitor Block.

Table 2-58 • Analog Multiplexer Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)

| Control Lines Bx[4] | Control Lines Bx[3] | ADC Connected To                      |
|---------------------|---------------------|---------------------------------------|
| 0                   | 0                   | Prescaler                             |
| 0                   | 1                   | Direct input                          |
| 1                   | 0                   | Current amplifier temperature monitor |
| 1                   | 1                   | Not valid                             |

Table 2-59 details the settings available to control the Direct Analog Input switch for the AV, AC, and AT pins.

#### *Table 2-59* • Direct Analog Input Switch Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)

| Control Lines Bx[5] | Direct Input Switch |
|---------------------|---------------------|
| 0                   | Off                 |
| 1                   | On                  |

Table 2-60 details the settings available to control the polarity of the signals coming to the AV, AC, and AT pins. Note that the only valid setting for the AT pin is logic 0 to support positive voltages.

#### Table 2-60 • Voltage Polarity Control Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3)\*

| Control Lines Bx[6] | Input Signal Polarity |
|---------------------|-----------------------|
| 0                   | Positive              |
| 1                   | Negative              |

Note: \*The B3[6] signal for the AT pad should be kept at logic 0 to accept only positive voltages.



Temporary overshoots are allowed according to Table 3-4 on page 3-4.



Figure 2-103 • Solution 1

## Solution 2

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-4 on page 3-4. This is a long-term reliability requirement.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the external resistors and Zener, as shown in Figure 2-104. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.



Figure 2-104 • Solution 2



At the system level, the skew circuit can be used in applications where transmission activities on bidirectional data lines need to be coordinated. This circuit, when selected, provides a timing margin that can prevent bus contention and subsequent data loss or transmitter overstress due to transmitter-to-transmitter current shorts. Figure 2-110 presents an example of the skew circuit implementation in a bidirectional communication system. Figure 2-111 shows how bus contention is created, and Figure 2-112 on page 2-151 shows how it can be avoided with the skew circuit.







Figure 2-111 • Timing Diagram (bypasses skew circuit)

# **Overview of I/O Performance** Summary of I/O DC Input and Output Levels – Default I/O Software Settings

#### Table 2-86 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions Applicable to Pro I/Os

|                               |                    |              |           | VIL         | VIH           |            | VOL         | VOH         | IOL | IOH |
|-------------------------------|--------------------|--------------|-----------|-------------|---------------|------------|-------------|-------------|-----|-----|
| I/O Standard                  | Drive<br>Strength  | Slew<br>Rate | Min.<br>V | Max.<br>V   | Min.<br>V     | Max.<br>V  | Max.<br>V   | Min.<br>V   | mA  | mA  |
| 3.3 V LVTTL /<br>3.3 V LVCMOS | 12 mA              | High         | -0.3      | 0.8         | 2             | 3.6        | 0.4         | 2.4         | 12  | 12  |
| 2.5 V LVCMOS                  | 12 mA              | High         | -0.3      | 0.7         | 1.7           | 3.6        | 0.7         | 1.7         | 12  | 12  |
| 1.8 V LVCMOS                  | 12 mA              | High         | -0.3      | 0.35 * VCCI | 0.65 * VCCI   | 3.6        | 0.45        | VCCI - 0.45 | 12  | 12  |
| 1.5 V LVCMOS                  | 12 mA              | High         | -0.3      | 0.35 * VCCI | 0.65 * VCCI   | 3.6        | 0.25 * VCCI | 0.75 * VCCI | 12  | 12  |
| 3.3 V PCI                     |                    | •            | •         |             | Per PCI Spec  | ification  |             |             |     |     |
| 3.3 V PCI-X                   |                    |              |           |             | Per PCI-X Spe | cification |             |             |     |     |
| 3.3 V GTL                     | 20 mA <sup>2</sup> | High         | -0.3      | VREF-0.05   | VREF + 0.05   | 3.6        | 0.4         | -           | 20  | 20  |
| 2.5 V GTL                     | 20 mA <sup>2</sup> | High         | -0.3      | VREF-0.05   | VREF + 0.05   | 3.6        | 0.4         | -           | 20  | 20  |
| 3.3 V GTL+                    | 35 mA              | High         | -0.3      | VREF – 0.1  | VREF + 0.1    | 3.6        | 0.6         | -           | 35  | 35  |
| 2.5 V GTL+                    | 33 mA              | High         | -0.3      | VREF – 0.1  | VREF + 0.1    | 3.6        | 0.6         | -           | 33  | 33  |
| HSTL (I)                      | 8 mA               | High         | -0.3      | VREF – 0.1  | VREF + 0.1    | 3.6        | 0.4         | VCCI – 0.4  | 8   | 8   |
| HSTL (II)                     | 15 mA <sup>2</sup> | High         | -0.3      | VREF – 0.1  | VREF + 0.1    | 3.6        | 0.4         | VCCI – 0.4  | 15  | 15  |
| SSTL2 (I)                     | 15 mA              | High         | -0.3      | VREF – 0.2  | VREF + 0.2    | 3.6        | 0.54        | VCCI-0.62   | 15  | 15  |
| SSTL2 (II)                    | 18 mA              | High         | -0.3      | VREF – 0.2  | VREF + 0.2    | 3.6        | 0.35        | VCCI-0.43   | 18  | 18  |
| SSTL3 (I)                     | 14 mA              | High         | -0.3      | VREF - 0.2  | VREF + 0.2    | 3.6        | 0.7         | VCCI – 1.1  | 14  | 14  |
| SSTL3 (II)                    | 21 mA              | High         | -0.3      | VREF – 0.2  | VREF + 0.2    | 3.6        | 0.5         | VCCI – 0.9  | 21  | 21  |

#### Notes:

1. Currents are measured at 85°C junction temperature.

2. Output drive strength is below JEDEC specification.

3. Output slew rate can be extracted by the IBIS models.

#### Table 2-87 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions Applicable to Advanced I/Os

|                               |                   |              | VIL       |             | VIH           | VIH        |             | VOH         | IOL | ЮН |
|-------------------------------|-------------------|--------------|-----------|-------------|---------------|------------|-------------|-------------|-----|----|
| I/O Standard                  | Drive<br>Strength | Slew<br>Rate | Min.<br>V | Max.<br>V   | Min.<br>V     | Max.<br>V  | Max.<br>V   | Min.<br>V   | mA  | mA |
| 3.3 V LVTTL /<br>3.3 V LVCMOS | 12 mA             | High         | -0.3      | 0.8         | 2             | 3.6        | 0.4         | 2.4         | 12  | 12 |
| 2.5 V LVCMOS                  | 12 mA             | High         | -0.3      | 0.7         | 1.7           | 2.7        | 0.7         | 1.7         | 12  | 12 |
| 1.8 V LVCMOS                  | 12 mA             | High         | -0.3      | 0.35 * VCCI | 0.65 * VCCI   | 1.9        | 0.45        | VCCI-0.45   | 12  | 12 |
| 1.5 V LVCMOS                  | 12 mA             | High         | -0.3      | 0.35 * VCCI | 0.65 * VCCI   | 1.575      | 0.25 * VCCI | 0.75 * VCCI | 12  | 12 |
| 3.3 V PCI                     |                   |              |           |             | Per PCI speci | fications  | 3           |             |     |    |
| 3.3 V PCI-X                   |                   |              |           | Р           | er PCI-X spec | cificatior | าร          |             |     |    |

*Note:* Currents are measured at 85°C junction temperature.



| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | C <sub>LOAD</sub> (pF) |
|---------------|----------------|----------------------|-----------------|------------------------|
| 0             | 3.3            | 1.4                  | -               | 35                     |

Note: \*Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

#### Timing Characteristics

### Table 2-104 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew

Commercial Temperature Range Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Pro I/Os

| Drive<br>Strength | Speed<br>Grade | t <sub>DOUT</sub> | t <sub>DP</sub> | t <sub>DIN</sub> | t <sub>PY</sub> | t <sub>PYS</sub> | t <sub>EOUT</sub> | t <sub>ZL</sub> | t <sub>zH</sub> | t <sub>LZ</sub> | t <sub>HZ</sub> | t <sub>zLS</sub> | t <sub>zHS</sub> | Units |
|-------------------|----------------|-------------------|-----------------|------------------|-----------------|------------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| 4 mA              | Std.           | 0.66              | 11.01           | 0.04             | 1.20            | 1.57             | 0.43              | 11.21           | 9.05            | 2.69            | 2.44            | 13.45            | 11.29            | ns    |
|                   | -1             | 0.56              | 9.36            | 0.04             | 1.02            | 1.33             | 0.36              | 9.54            | 7.70            | 2.29            | 2.08            | 11.44            | 9.60             | ns    |
|                   | -2             | 0.49              | 8.22            | 0.03             | 0.90            | 1.17             | 0.32              | 8.37            | 6.76            | 2.01            | 1.82            | 10.04            | 8.43             | ns    |
| 8 mA              | Std.           | 0.66              | 7.86            | 0.04             | 1.20            | 1.57             | 0.43              | 8.01            | 6.44            | 3.04            | 3.06            | 10.24            | 8.68             | ns    |
|                   | -1             | 0.56              | 6.69            | 0.04             | 1.02            | 1.33             | 0.36              | 6.81            | 5.48            | 2.58            | 2.61            | 8.71             | 7.38             | ns    |
|                   | -2             | 0.49              | 5.87            | 0.03             | 0.90            | 1.17             | 0.32              | 5.98            | 4.81            | 2.27            | 2.29            | 7.65             | 6.48             | ns    |
| 12 mA             | Std.           | 0.66              | 6.03            | 0.04             | 1.20            | 1.57             | 0.43              | 6.14            | 5.02            | 3.28            | 3.47            | 8.37             | 7.26             | ns    |
|                   | -1             | 0.56              | 5.13            | 0.04             | 1.02            | 1.33             | 0.36              | 5.22            | 4.27            | 2.79            | 2.95            | 7.12             | 6.17             | ns    |
|                   | -2             | 0.49              | 4.50            | 0.03             | 0.90            | 1.17             | 0.32              | 4.58            | 3.75            | 2.45            | 2.59            | 6.25             | 5.42             | ns    |
| 16 mA             | Std.           | 0.66              | 5.62            | 0.04             | 1.20            | 1.57             | 0.43              | 5.72            | 4.72            | 3.32            | 3.58            | 7.96             | 6.96             | ns    |
|                   | -1             | 0.56              | 4.78            | 0.04             | 1.02            | 1.33             | 0.36              | 4.87            | 4.02            | 2.83            | 3.04            | 6.77             | 5.92             | ns    |
|                   | -2             | 0.49              | 4.20            | 0.03             | 0.90            | 1.17             | 0.32              | 4.27            | 3.53            | 2.48            | 2.67            | 5.94             | 5.20             | ns    |
| 24 mA             | Std.           | 0.66              | 5.24            | 0.04             | 1.20            | 1.57             | 0.43              | 5.34            | 4.69            | 3.39            | 3.96            | 7.58             | 6.93             | ns    |
|                   | -1             | 0.56              | 4.46            | 0.04             | 1.02            | 1.33             | 0.36              | 4.54            | 3.99            | 2.88            | 3.37            | 6.44             | 5.89             | ns    |
|                   | -2             | 0.49              | 3.92            | 0.03             | 0.90            | 1.17             | 0.32              | 3.99            | 3.50            | 2.53            | 2.96            | 5.66             | 5.17             | ns    |

#### Timing Characteristics

Table 2-120 • 1.8 V LVCMOS Low Slew

Commercial Temperature Range Conditions:  $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V Applicable to Pro I/Os

| Drive<br>Strength | Speed<br>Grade | t <sub>DOUT</sub> | t <sub>DP</sub> | t <sub>DIN</sub> | t <sub>PY</sub> | t <sub>PYS</sub> | t <sub>EOUT</sub> | t <sub>ZL</sub> | t <sub>zH</sub> | t <sub>LZ</sub> | t <sub>HZ</sub> | t <sub>zLS</sub> | t <sub>zHS</sub> | Units |
|-------------------|----------------|-------------------|-----------------|------------------|-----------------|------------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| 2 mA              | Std.           | 0.66              | 15.84           | 0.04             | 1.45            | 1.91             | 0.43              | 15.65           | 15.84           | 2.78            | 1.58            | 17.89            | 18.07            | ns    |
|                   | -1             | 0.56              | 13.47           | 0.04             | 1.23            | 1.62             | 0.36              | 13.31           | 13.47           | 2.37            | 1.35            | 15.22            | 15.37            | ns    |
|                   | -2             | 0.49              | 11.83           | 0.03             | 1.08            | 1.42             | 0.32              | 11.69           | 11.83           | 2.08            | 1.18            | 13.36            | 13.50            | ns    |
| 4 mA              | Std.           | 0.66              | 11.39           | 0.04             | 1.45            | 1.91             | 0.43              | 11.60           | 10.76           | 3.26            | 2.77            | 13.84            | 12.99            | ns    |
|                   | -1             | 0.56              | 9.69            | 0.04             | 1.23            | 1.62             | 0.36              | 9.87            | 9.15            | 2.77            | 2.36            | 11.77            | 11.05            | ns    |
|                   | -2             | 0.49              | 8.51            | 0.03             | 1.08            | 1.42             | 0.32              | 8.66            | 8.03            | 2.43            | 2.07            | 10.33            | 9.70             | ns    |
| 8 mA              | Std.           | 0.66              | 8.97            | 0.04             | 1.45            | 1.91             | 0.43              | 9.14            | 8.10            | 3.57            | 3.36            | 11.37            | 10.33            | ns    |
|                   | -1             | 0.56              | 7.63            | 0.04             | 1.23            | 1.62             | 0.36              | 7.77            | 6.89            | 3.04            | 2.86            | 9.67             | 8.79             | ns    |
|                   | -2             | 0.49              | 6.70            | 0.03             | 1.08            | 1.42             | 0.32              | 6.82            | 6.05            | 2.66            | 2.51            | 8.49             | 7.72             | ns    |
| 12 mA             | Std.           | 0.66              | 8.35            | 0.04             | 1.45            | 1.91             | 0.43              | 8.50            | 7.59            | 3.64            | 3.52            | 10.74            | 9.82             | ns    |
|                   | -1             | 0.56              | 7.10            | 0.04             | 1.23            | 1.62             | 0.36              | 7.23            | 6.45            | 3.10            | 3.00            | 9.14             | 8.35             | ns    |
|                   | -2             | 0.49              | 6.24            | 0.03             | 1.08            | 1.42             | 0.32              | 6.35            | 5.66            | 2.72            | 2.63            | 8.02             | 7.33             | ns    |
| 16 mA             | Std.           | 0.66              | 7.94            | 0.04             | 1.45            | 1.91             | 0.43              | 8.09            | 7.56            | 3.74            | 4.11            | 10.32            | 9.80             | ns    |
|                   | -1             | 0.56              | 6.75            | 0.04             | 1.23            | 1.62             | 0.36              | 6.88            | 6.43            | 3.18            | 3.49            | 8.78             | 8.33             | ns    |
|                   | -2             | 0.49              | 5.93            | 0.03             | 1.08            | 1.42             | 0.32              | 6.04            | 5.65            | 2.79            | 3.07            | 7.71             | 7.32             | ns    |



# Voltage Referenced I/O Characteristics

#### 3.3 V GTL

Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

| 3.3 V GTL          |           | VIL         | VIF         | I         | VOL       | VOH       | IOL | IOH | IOSL                    | IOSH                    | IIL <sup>1</sup> | IIH <sup>2</sup> |
|--------------------|-----------|-------------|-------------|-----------|-----------|-----------|-----|-----|-------------------------|-------------------------|------------------|------------------|
| Drive<br>Strength  | Min.<br>V | Max.<br>V   | Min.<br>V   | Max.<br>V | Max.<br>V | Min.<br>V | mA  | mA  | Max.<br>mA <sup>3</sup> | Max.<br>mA <sup>3</sup> | μA <sup>4</sup>  | μA <sup>4</sup>  |
| 20 mA <sup>3</sup> | -0.3      | VREF – 0.05 | VREF + 0.05 | 3.6       | 0.4       | _         | 20  | 20  | 181                     | 268                     | 10               | 10               |

Table 2-138 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.



#### Figure 2-124 • AC Loading

#### Table 2-139 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C <sub>LOAD</sub> (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF – 0.05   | VREF + 0.05    | 0.8                  | 0.8             | 1.2            | 10                     |

Note: \*Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

#### Timing Characteristics

Table 2-140 • 3.3 V GTL

```
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 0.8 V
```

| Speed<br>Grade | t <sub>DOUT</sub> | t <sub>DP</sub> | t <sub>DIN</sub> | t <sub>PY</sub> | t <sub>EOUT</sub> | t <sub>ZL</sub> | t <sub>zH</sub> | t <sub>LZ</sub> | t <sub>HZ</sub> | t <sub>ZLS</sub> | t <sub>zHS</sub> | Units |
|----------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std.           | 0.66              | 2.08            | 0.04             | 2.93            | 0.43              | 2.04            | 2.08            |                 |                 | 4.27             | 4.31             | ns    |
| -1             | 0.56              | 1.77            | 0.04             | 2.50            | 0.36              | 1.73            | 1.77            |                 |                 | 3.63             | 3.67             | ns    |
| -2             | 0.49              | 1.55            | 0.03             | 2.19            | 0.32              | 1.52            | 1.55            |                 |                 | 3.19             | 3.22             | ns    |

#### SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

| SSTL3 Class II |           | VIL        | VIH        |           | VOL       | VOH        | IOL | IOH | IOSL                    | IOSH                    | IIL <sup>1</sup> | IIH <sup>2</sup> |
|----------------|-----------|------------|------------|-----------|-----------|------------|-----|-----|-------------------------|-------------------------|------------------|------------------|
| Drive Strength | Min.<br>V | Max.<br>V  | Min.<br>V  | Max.<br>V | Max.<br>V | Min.<br>V  | mA  | mA  | Max.<br>mA <sup>3</sup> | Max.<br>mA <sup>3</sup> | μA <sup>4</sup>  | μA <sup>4</sup>  |
| 21 mA          | -0.3      | VREF – 0.2 | VREF + 0.2 | 3.6       | 0.5       | VCCI – 0.9 | 21  | 21  | 109                     | 103                     | 10               | 10               |

Table 2-165 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.



#### Figure 2-133 • AC Loading

#### Table 2-166 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | VREF (typ.) (V) | VTT (typ.) (V) | C <sub>LOAD</sub> (pF) |
|---------------|----------------|----------------------|-----------------|----------------|------------------------|
| VREF – 0.2    | VREF + 0.2     | 1.5                  | 1.5             | 1.485          | 30                     |

Note: \*Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

#### Timing Characteristics

Table 2-167 • SSTL3- Class II Commercial Temperature Range Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.5 V

| Speed<br>Grade | t <sub>DOUT</sub> | t <sub>DP</sub> | t <sub>DIN</sub> | t <sub>PY</sub> | t <sub>EOUT</sub> | t <sub>ZL</sub> | t <sub>zH</sub> | t <sub>LZ</sub> | t <sub>HZ</sub> | t <sub>ZLS</sub> | t <sub>zHS</sub> | Units |
|----------------|-------------------|-----------------|------------------|-----------------|-------------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------|
| Std.           | 0.66              | 2.07            | 0.04             | 1.25            | 0.43              | 2.10            | 1.67            |                 |                 | 4.34             | 3.91             | ns    |
| -1             | 0.56              | 1.76            | 0.04             | 1.06            | 0.36              | 1.79            | 1.42            |                 |                 | 3.69             | 3.32             | ns    |
| -2             | 0.49              | 1.54            | 0.03             | 0.93            | 0.32              | 1.57            | 1.25            |                 |                 | 3.24             | 2.92             | ns    |



#### Output Enable Register



#### **Timing Characteristics**

# Table 2-178 • Output Enable Register Propagation DelaysCommercial Temperature Range Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

| Parameter             | Description  | -2   | -1   | Std. | Units |
|-----------------------|--|------|------|------|-------|
| t <sub>OECLKQ</sub>   | Clock-to-Q of the Output Enable Register                               | 0.44 | 0.51 | 0.59 | ns    |
| t <sub>OESUD</sub>    | Data Setup Time for the Output Enable Register                         | 0.31 | 0.36 | 0.42 | ns    |
| t <sub>OEHD</sub>     | Data Hold Time for the Output Enable Register                          | 0.00 | 0.00 | 0.00 | ns    |
| t <sub>OESUE</sub>    | Enable Setup Time for the Output Enable Register                       | 0.44 | 0.50 | 0.58 | ns    |
| t <sub>OEHE</sub>     | Enable Hold Time for the Output Enable Register                        | 0.00 | 0.00 | 0.00 | ns    |
| t <sub>OECLR2Q</sub>  | Asynchronous Clear-to-Q of the Output Enable Register                  | 0.67 | 0.76 | 0.89 | ns    |
| t <sub>OEPRE2Q</sub>  | Asynchronous Preset-to-Q of the Output Enable Register                 | 0.67 | 0.76 | 0.89 | ns    |
| t <sub>OEREMCLR</sub> | Asynchronous Clear Removal Time for the Output Enable Register         | 0.00 | 0.00 | 0.00 | ns    |
| t <sub>OERECCLR</sub> | Asynchronous Clear Recovery Time for the Output Enable Register        | 0.22 | 0.25 | 0.30 | ns    |
| t <sub>OEREMPRE</sub> | Asynchronous Preset Removal Time for the Output Enable Register        | 0.00 | 0.00 | 0.00 | ns    |
| t <sub>OERECPRE</sub> | Asynchronous Preset Recovery Time for the Output Enable Register       | 0.22 | 0.25 | 0.30 | ns    |
| t <sub>OEWCLR</sub>   | Asynchronous Clear Minimum Pulse Width for the Output Enable Register  | 0.22 | 0.25 | 0.30 | ns    |
| t <sub>OEWPRE</sub>   | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.22 | 0.25 | 0.30 | ns    |
| t <sub>OECKMPWH</sub> | Clock Minimum Pulse Width High for the Output Enable Register          | 0.36 | 0.41 | 0.48 | ns    |
| t <sub>OECKMPWL</sub> | Clock Minimum Pulse Width Low for the Output Enable Register           | 0.32 | 0.37 | 0.43 | ns    |

## Theta-JA

Junction-to-ambient thermal resistance ( $\theta_{JA}$ ) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the AFS600-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

Maximum Power Allowed = 
$$\frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

where

 $\theta_{JA}$  = 19.00°C/W (taken from Table 3-6 on page 3-7).

 $T_A = 75.00^{\circ}C$ 

Maximum Power Allowed = 
$$\frac{100.00^{\circ}C - 75.00^{\circ}C}{19.00^{\circ}C/W} = 1.3 W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

## Theta-JB

Junction-to-board thermal resistance ( $\theta_{JB}$ ) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

## Theta-JC

Junction-to-case thermal resistance ( $\theta_{JC}$ ) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

## Calculation for Heat Sink

For example, in a design implemented in an AFS600-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent  $T_a$  and  $T_j$  are given as follows:

 $T_{J} = 100.00^{\circ}C$ 

 $T_A = 70.00^{\circ}C$ 

From the datasheet:

 $\theta_{JA} = 17.00^{\circ}C/W$  $\theta_{JC} = 8.28^{\circ}C/W$ 

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100^{\circ}C - 70^{\circ}C}{17.00 \text{ W}} = 1.76 \text{ W}$$

EQ 6

# **Calculating Power Dissipation**

# **Quiescent Supply Current**

### Table 3-8 • AFS1500 Quiescent Supply Current Characteristics

| Parameter          | Description             | Conditions  | Temp.                  | Min. | Тур. | Max. | Unit |
|--------------------|-------------------------|---|------------------------|------|------|------|------|
| ICC <sup>1</sup>   | 1.5 V quiescent current | Operational standby <sup>4</sup> ,                                  | T <sub>J</sub> = 25°C  |      | 20   | 40   | mA   |
|                    |                         | VCC = 1.575 V   | T <sub>J</sub> = 85°C  |      | 32   | 65   | mA   |
|                    |                         |   | T <sub>J</sub> = 100°C |      | 59   | 120  | mA   |
|                    |                         | Standby mode <sup>5</sup> or Sleep mode <sup>6</sup> ,<br>VCC = 0 V |                        |      | 0    | 0    | μA   |
| ICC33 <sup>2</sup> | 3.3 V analog supplies   | Operational standby <sup>4</sup> ,                                  | T <sub>J</sub> = 25°C  |      | 9.8  | 13   | mA   |
|                    | current                 | VCC33 = 3.63 V  | T <sub>J</sub> = 85°C  |      | 10.7 | 14   | mA   |
|                    |                         |   | T <sub>J</sub> = 100°C |      | 10.8 | 15   | mA   |
|                    |                         | Operational standby, only Analog                                    | T <sub>J</sub> = 25°C  |      | 0.31 | 2    | mA   |
|                    |                         | Quad and $-3.3$ V output ON,<br>VCC33 = 3.63 V                      | T <sub>J</sub> = 85°C  |      | 0.35 | 2    | mA   |
|                    |                         |   | T <sub>J</sub> = 100°C |      | 0.45 | 2    | mA   |
|                    |                         | Standby mode <sup>5</sup> , VCC33 = 3.63 V                          | T <sub>J</sub> = 25°C  |      | 2.9  | 3.6  | mA   |
|                    |                         |   | T <sub>J</sub> = 85°C  |      | 2.9  | 4    | mA   |
|                    |                         |   | T <sub>J</sub> = 100°C |      | 3.3  | 6    | mA   |
|                    |                         | Sleep mode <sup>6</sup> , VCC33 = 3.63 V                            | T <sub>J</sub> = 25°C  |      | 17   | 19   | μA   |
|                    |                         |   | T <sub>J</sub> = 85°C  |      | 18   | 20   | μA   |
|                    |                         |   | T <sub>J</sub> = 100°C |      | 24   | 25   | μA   |
| ICCI <sup>3</sup>  | I/O quiescent current   | Operational standby <sup>4</sup> ,                                  | T <sub>J</sub> = 25°C  |      | 417  | 649  | μA   |
|                    |                         | Standby mode, and Sleep Mode <sup>o</sup> , VCCIx = 3.63 V          | T <sub>J</sub> = 85°C  |      | 417  | 649  | μA   |
|                    |                         |   | T <sub>J</sub> = 100°C |      | 417  | 649  | μA   |

Notes:

1. ICC is the 1.5 V power supplies, ICC and ICC15A.

2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.

3. ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.

4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.

5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.

6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.



DC and Power Characteristics

| Table 3-10 • AFS250 Q | Quiescent Supply Current | Characteristics (continued) |
|-----------------------|--------------------------|-----------------------------|
|-----------------------|--------------------------|-----------------------------|

| Parameter | Description                 | Conditions  | Temp.                  | Min | Тур | Max | Unit |
|-----------|-----------------------------|---|------------------------|-----|-----|-----|------|
| IPP       | Programming supply          | Non-programming mode,   | T <sub>J</sub> = 25°C  |     | 37  | 80  | μA   |
|           | current                     | VPUMP = 3.63 V  | T <sub>J</sub> = 85°C  |     | 37  | 80  | μA   |
|           |                             |   | T <sub>J</sub> = 100°C |     | 80  | 100 | μA   |
|           |                             | Standby mode <sup>5</sup> or Sleep<br>mode <sup>6</sup> , VPUMP = 0 V |                        |     | 0   | 0   | μA   |
| ICCNVM    | Embedded NVM current        | Reset asserted,   | T <sub>J</sub> = 25°C  |     | 10  | 40  | μA   |
|           |                             | VCCNVM = 1.575 V  | T <sub>J</sub> = 85°C  |     | 14  | 40  | μA   |
|           |                             |   | T <sub>J</sub> = 100°C |     | 14  | 40  | μA   |
| ICCPLL    | 1.5 V PLL quiescent current | Operational standby,  | T <sub>J</sub> = 25°C  |     | 65  | 100 | μA   |
|           |                             | VCCPLL = 1.575 V  | T <sub>J</sub> = 85°C  |     | 65  | 100 | μA   |
|           |                             |   | T <sub>J</sub> = 100°C |     | 65  | 100 | μA   |

Notes:

- 1. ICC is the 1.5 V power supplies, ICC, ICCPLL, ICC15A, ICCNVM.
- 2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.
- 3. ICCI includes all ICCI0, ICCI1, and ICCI2.
- 4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.
- 5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.
- 6. Sleep Mode, VCC = VJTA G = VPUMP = 0 V.

# Example of Power Calculation

This example considers a shift register with 5,000 storage tiles, including a counter and memory that stores analog information. The shift register is clocked at 50 MHz and stores and reads information from a RAM.

The device used is a commercial AFS600 device operating in typical conditions.

The calculation below uses the power calculation methodology previously presented and shows how to determine the dynamic and static power consumption of resources used in the application.

Also included in the example is the calculation of power consumption in operating, standby, and sleep modes to illustrate the benefit of power-saving modes.

#### Global Clock Contribution—P<sub>CLOCK</sub>

 $F_{CLK}$  = 50 MHz Number of sequential VersaTiles: N<sub>S-CELL</sub> = 5,000 Estimated number of Spines: N<sub>SPINES</sub> = 5 Estimated number of Rows: N<sub>ROW</sub> = 313

#### **Operating Mode**

$$\begin{split} & \mathsf{P}_{\mathsf{CLOCK}} = (\mathsf{PAC1} + \mathsf{N}_{\mathsf{SPINE}} * \mathsf{PAC2} + \mathsf{N}_{\mathsf{ROW}} * \mathsf{PAC3} + \mathsf{N}_{\mathsf{S}\text{-}\mathsf{CELL}} * \mathsf{PAC4}) * \mathsf{F}_{\mathsf{CLK}} \\ & \mathsf{P}_{\mathsf{CLOCK}} = (0.0128 + 5 * 0.0019 + 313 * 0.00081 + 5,000 * 0.00011) * 50 \\ & \mathsf{P}_{\mathsf{CLOCK}} = 41.28 \ \mathsf{mW} \end{split}$$

#### Standby Mode and Sleep Mode

 $P_{CLOCK} = 0 W$ 

Logic—Sequential Cells, Combinational Cells, and Routing Net Contributions— $P_{S-CELL}$ ,  $P_{C-CELL}$ , and  $P_{NET}$ 

 $\label{eq:F_CLK} \ensuremath{\mathsf{F_{CLK}}}\xspace = 50 \ensuremath{\,\mathsf{MHz}}\xspace \\ \ensuremath{\mathsf{Number}}\xspace of sequential VersaTiles: \ensuremath{\mathsf{N}_{S-CELL}}\xspace = 5,000 \\ \ensuremath{\mathsf{Number}}\xspace of versaTiles: \ensuremath{\mathsf{N}_{C-CELL}}\xspace = 6,000 \\ \ensuremath{\mathsf{Estimated}}\xspace toggle rate of VersaTile outputs: \ensuremath{\alpha_1}\xspace = 0.1 \ensuremath{\,(10\%)}\xspace \ensuremath{}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{}\xspace \ensuremath{}\xspace \ensuremath{\mathsf{R}}\xspace \ensuremath{}\xspace \ensuremath{$ 

#### **Operating Mode**

$$\begin{split} \mathsf{P}_{S\text{-}CELL} &= \mathsf{N}_{S\text{-}CELL} * (\mathsf{P}_{\mathsf{AC5}}\text{+} (\alpha_1 \, / \, 2) * \mathsf{PAC6}) * \mathsf{F}_{\mathsf{CLK}} \\ \mathsf{P}_{S\text{-}CELL} &= 5,000 * (0.00007 + (0.1 \, / \, 2) * 0.00029) * 50 \\ \mathsf{P}_{S\text{-}CELL} &= 21.13 \text{ mW} \end{split}$$

 $P_{C-CELL} = N_{C-CELL}^* (\alpha_1 / 2) * PAC7 * F_{CLK}$  $P_{C-CELL} = 6,000 * (0.1 / 2) * 0.00029 * 50$  $P_{C-CELL} = 4.35 \text{ mW}$ 

$$\begin{split} \mathsf{P}_{\mathsf{NET}} &= (\mathsf{N}_{\mathsf{S}\text{-}\mathsf{CELL}} + \mathsf{N}_{\mathsf{C}\text{-}\mathsf{CELL}}) * (\alpha_1 \,/\, 2) * \mathsf{PAC8} * \mathsf{F}_{\mathsf{CLK}} \\ \mathsf{P}_{\mathsf{NET}} &= (5,000 + 6,000) * (0.1 \,/\, 2) * 0.0007 * 50 \\ \mathsf{P}_{\mathsf{NET}} &= 19.25 \text{ mW} \end{split}$$

 $P_{LOGIC} = P_{S-CELL} + P_{C-CELL} + P_{NET}$  $P_{LOGIC} = 21.13 \text{ mW} + 4.35 \text{ mW} + 19.25 \text{ mW}$  $P_{LOGIC} = 44.73 \text{ mW}$ 

Standby Mode and Sleep Mode

Fusion Family of Mixed Signal FPGAs

|               | PQ208           |                 | PQ208         |                 |                 |  |  |  |
|---------------|-----------------|-----------------|---------------|-----------------|-----------------|--|--|--|
| Pin<br>Number | AFS250 Function | AFS600 Function | Pin<br>Number | AFS250 Function | AFS600 Function |  |  |  |
| 74            | AV2             | AV4             | 111           | VCCNVM          | VCCNVM          |  |  |  |
| 75            | AC2             | AC4             | 112           | VCC             | VCC             |  |  |  |
| 76            | AG2             | AG4             | 112           | VCC             | VCC             |  |  |  |
| 77            | AT2             | AT4             | 113           | VPUMP           | VPUMP           |  |  |  |
| 78            | ATRTN1          | ATRTN2          | 114           | GNDQ            | NC              |  |  |  |
| 79            | AT3             | AT5             | 115           | VCCIB1          | ТСК             |  |  |  |
| 80            | AG3             | AG5             | 116           | ТСК             | TDI             |  |  |  |
| 81            | AC3             | AC5             | 117           | TDI             | TMS             |  |  |  |
| 82            | AV3             | AV5             | 118           | TMS             | TDO             |  |  |  |
| 83            | AV4             | AV6             | 119           | TDO             | TRST            |  |  |  |
| 84            | AC4             | AC6             | 120           | TRST            | VJTAG           |  |  |  |
| 85            | AG4             | AG6             | 121           | VJTAG           | IO57NDB2V0      |  |  |  |
| 86            | AT4             | AT6             | 122           | IO57NDB1V0      | GDC2/IO57PDB2V0 |  |  |  |
| 87            | ATRTN2          | ATRTN3          | 123           | GDC2/IO57PDB1V0 | IO56NDB2V0      |  |  |  |
| 88            | AT5             | AT7             | 124           | IO56NDB1V0      | GDB2/IO56PDB2V0 |  |  |  |
| 89            | AG5             | AG7             | 125           | GDB2/IO56PDB1V0 | IO55NDB2V0      |  |  |  |
| 90            | AC5             | AC7             | 126           | VCCIB1          | GDA2/IO55PDB2V0 |  |  |  |
| 91            | AV5             | AV7             | 127           | GND             | GDA0/IO54NDB2V0 |  |  |  |
| 92            | NC              | AV8             | 128           | IO55NDB1V0      | GDA1/IO54PDB2V0 |  |  |  |
| 93            | NC              | AC8             | 129           | GDA2/IO55PDB1V0 | VCCIB2          |  |  |  |
| 94            | NC              | AG8             | 130           | GDA0/IO54NDB1V0 | GND             |  |  |  |
| 95            | NC              | AT8             | 131           | GDA1/IO54PDB1V0 | VCC             |  |  |  |
| 96            | NC              | ATRTN4          | 132           | GDB0/IO53NDB1V0 | GCA0/IO45NDB2V0 |  |  |  |
| 97            | NC              | AT9             | 133           | GDB1/IO53PDB1V0 | GCA1/IO45PDB2V0 |  |  |  |
| 98            | NC              | AG9             | 134           | GDC0/IO52NDB1V0 | GCB0/IO44NDB2V0 |  |  |  |
| 99            | NC              | AC9             | 135           | GDC1/IO52PDB1V0 | GCB1/IO44PDB2V0 |  |  |  |
| 100           | NC              | AV9             | 136           | IO51NSB1V0      | GCC0/IO43NDB2V  |  |  |  |
| 101           | GNDAQ           | GNDAQ           |               |                 | 0               |  |  |  |
| 102           | VCC33A          | VCC33A          | 137           | VCCIB1          | GCC1/IO43PDB2V0 |  |  |  |
| 103           | ADCGNDREF       | ADCGNDREF       | 138           | GND             | IO42NDB2V0      |  |  |  |
| 104           | VAREF           | VAREF           | 139           | VCC             | IO42PDB2V0      |  |  |  |
| 105           | PUB             | PUB             | 140           | IO50NDB1V0      | IO41NDB2V0      |  |  |  |
| 106           | VCC33A          | VCC33A          | 141           | IO50PDB1V0      | GCC2/IO41PDB2V0 |  |  |  |
| 107           | GNDA            | GNDA            | 142           | GCA0/IO49NDB1V0 | VCCIB2          |  |  |  |
| 108           | PTEM            | PTEM            | 143           | GCA1/IO49PDB1V0 | GND             |  |  |  |
| 109           | PTBASE          | PTBASE          | 144           | GCB0/IO48NDB1V0 | VCC             |  |  |  |
| 110           | GNDNVM          | GNDNVM          | 145           | GCB1/IO48PDB1V0 | IO40NDB2V0      |  |  |  |
|               |                 | L]              | 146           | GCC0/IO47NDB1V0 | GCB2/IO40PDB2V0 |  |  |  |

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Package Pin Assignments

| FG676      |                  | FG676      |                  | FG676      |                  |
|------------|------------------|------------|------------------|------------|------------------|
| Pin Number | AFS1500 Function | Pin Number | AFS1500 Function | Pin Number | AFS1500 Function |
| L17        | VCCIB2           | N1         | NC               | P11        | VCC              |
| L18        | GCB2/IO60PDB2V0  | N2         | NC               | P12        | GND              |
| L19        | IO58NDB2V0       | N3         | IO108NDB4V0      | P13        | VCC              |
| L20        | IO57NDB2V0       | N4         | VCCOSC           | P14        | GND              |
| L21        | IO59NDB2V0       | N5         | VCCIB4           | P15        | VCC              |
| L22        | GCC2/IO61PDB2V0  | N6         | XTAL2            | P16        | GND              |
| L23        | IO55PPB2V0       | N7         | GFC1/IO107PDB4V0 | P17        | VCCIB2           |
| L24        | IO56PDB2V0       | N8         | VCCIB4           | P18        | IO70NDB2V0       |
| L25        | IO55NPB2V0       | N9         | GFB1/IO106PDB4V0 | P19        | VCCIB2           |
| L26        | GND              | N10        | VCCIB4           | P20        | IO69NDB2V0       |
| M1         | NC               | N11        | GND              | P21        | GCA0/IO64NDB2V0  |
| M2         | VCCIB4           | N12        | VCC              | P22        | VCCIB2           |
| M3         | GFC2/IO108PDB4V0 | N13        | GND              | P23        | GCB0/IO63NDB2V0  |
| M4         | GND              | N14        | VCC              | P24        | GCB1/IO63PDB2V0  |
| M5         | IO109NDB4V0      | N15        | GND              | P25        | IO66NDB2V0       |
| M6         | IO110NDB4V0      | N16        | VCC              | P26        | IO67PDB2V0       |
| M7         | GND              | N17        | VCCIB2           | R1         | NC               |
| M8         | IO104NDB4V0      | N18        | IO70PDB2V0       | R2         | VCCIB4           |
| M9         | IO111NDB4V0      | N19        | VCCIB2           | R3         | IO103NDB4V0      |
| M10        | GND              | N20        | IO69PDB2V0       | R4         | GND              |
| M11        | VCC              | N21        | GCA1/IO64PDB2V0  | R5         | IO101PDB4V0      |
| M12        | GND              | N22        | VCCIB2           | R6         | IO100NPB4V0      |
| M13        | VCC              | N23        | GCC0/IO62NDB2V0  | R7         | GND              |
| M14        | GND              | N24        | GCC1/IO62PDB2V0  | R8         | IO99PDB4V0       |
| M15        | VCC              | N25        | IO66PDB2V0       | R9         | IO97PDB4V0       |
| M16        | GND              | N26        | IO65NDB2V0       | R10        | GND              |
| M17        | GND              | P1         | NC               | R11        | GND              |
| M18        | IO60NDB2V0       | P2         | NC               | R12        | VCC              |
| M19        | IO58PDB2V0       | P3         | IO103PDB4V0      | R13        | GND              |
| M20        | GND              | P4         | XTAL1            | R14        | VCC              |
| M21        | IO68NPB2V0       | P5         | VCCIB4           | R15        | GND              |
| M22        | IO61NDB2V0       | P6         | GNDOSC           | R16        | VCC              |
| M23        | GND              | P7         | GFC0/IO107NDB4V0 | R17        | GND              |
| M24        | IO56NDB2V0       | P8         | VCCIB4           | R18        | GDB2/IO83PDB2V0  |
| M25        | VCCIB2           | P9         | GFB0/IO106NDB4V0 | R19        | IO78PDB2V0       |
| M26        | IO65PDB2V0       | P10        | VCCIB4           | R20        | GND              |